

CPE 100

# Digital logic DESIGN

Lecture 10

2/24/2021

2.14b

$$y = \overline{ABC} + A\overline{B}$$

$$\overline{A} + \overline{B} + \overline{C} = \overline{ABC}$$

$$= \overline{A} + \overline{B} + \overline{C} + A\overline{B} \quad \equiv \text{OR gate}$$

$$\overline{A} + A\overline{B} + \overline{B} + \overline{C}$$

$$\overline{A} + \overline{B} + \overline{C} \quad \equiv \text{CMOSedu.com}$$

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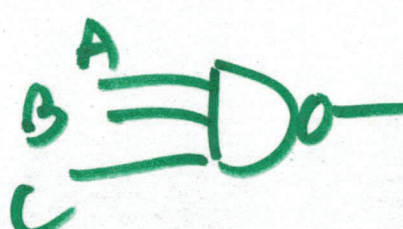


$$y = \overline{A}Bc + A\overline{B}\overline{c}$$

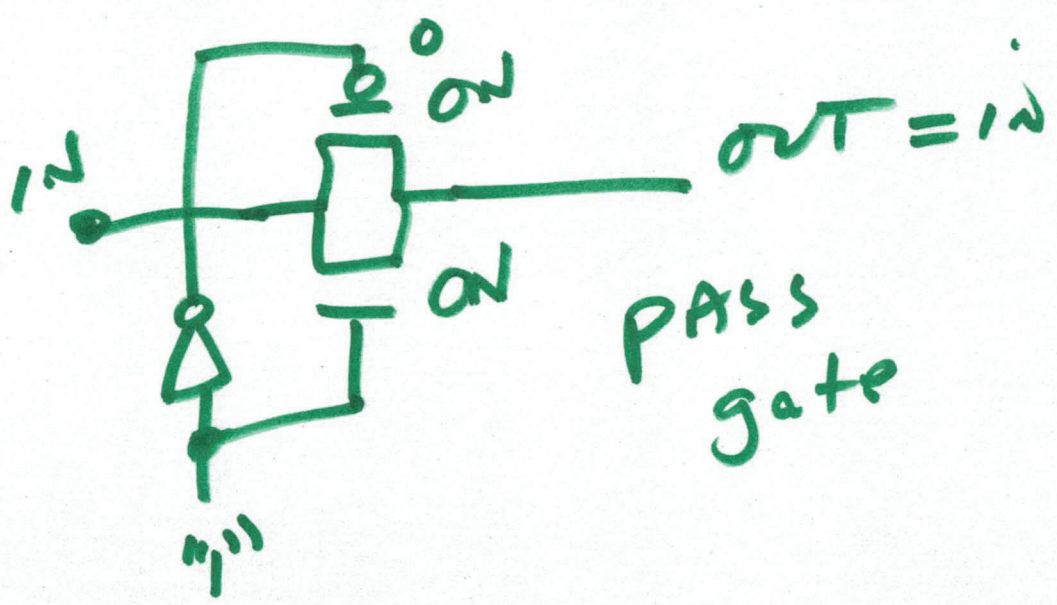
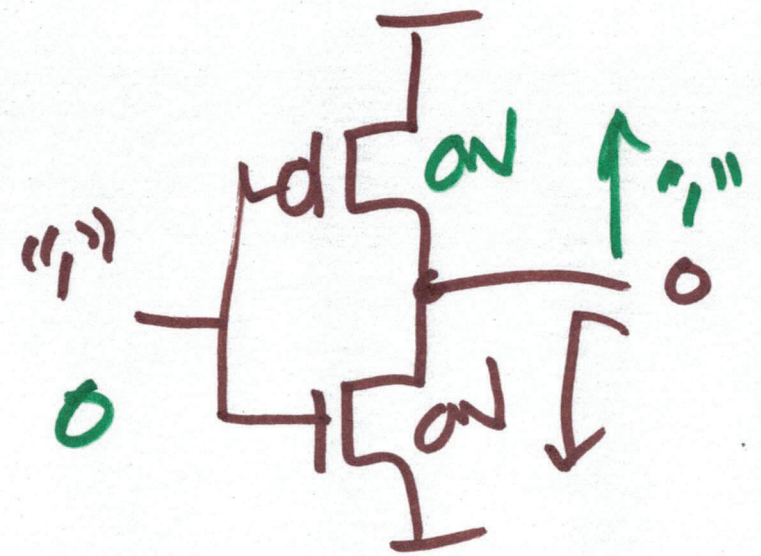
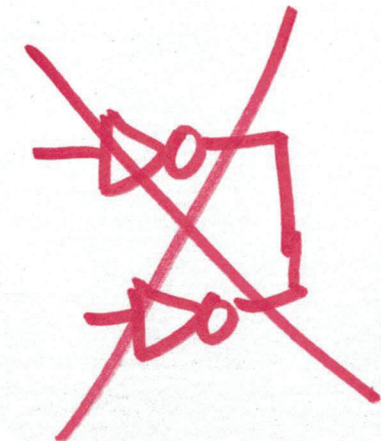
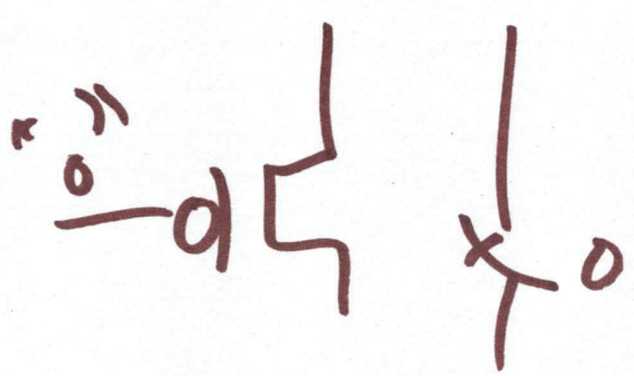
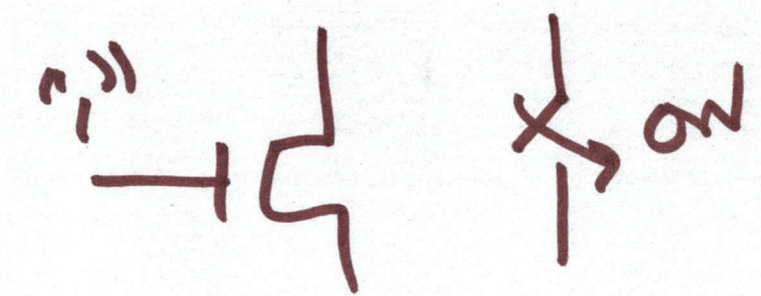
	AB			
	00	01	11	10
C				
0	0	0	0	
1	0	0	0	

	AB			
	00	01	11	10
C				
0	1	1	1	1
1	1	1	0	1

$$\overline{c} + \overline{a} + \overline{b}$$

$$\overline{A}Bc = \overline{A} + \overline{B} + \overline{C}$$


2



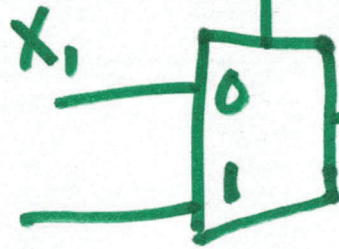


# 2-to-1 multiplexer

(MUX)

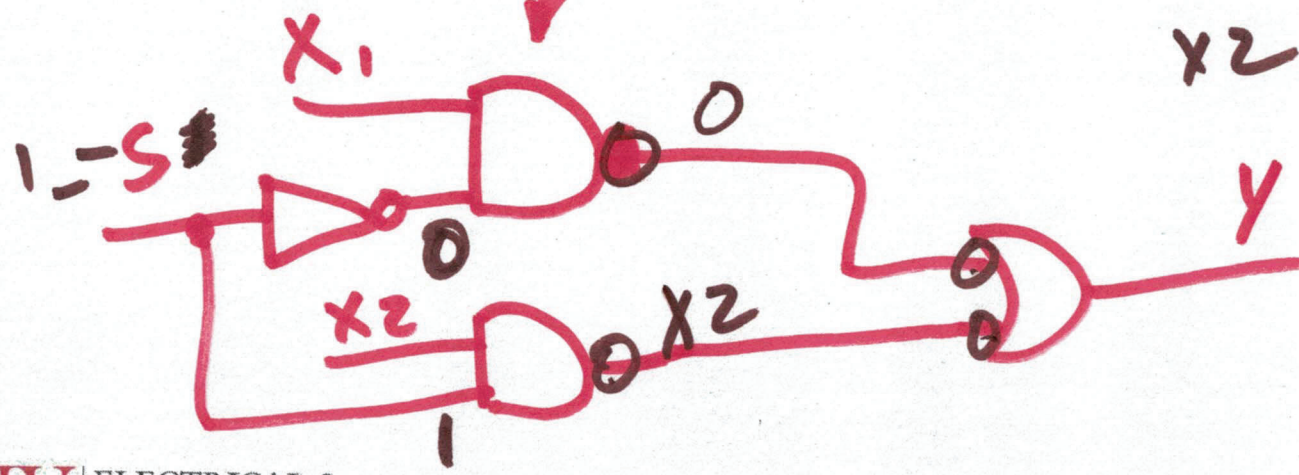
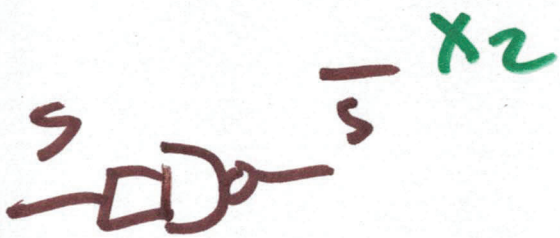
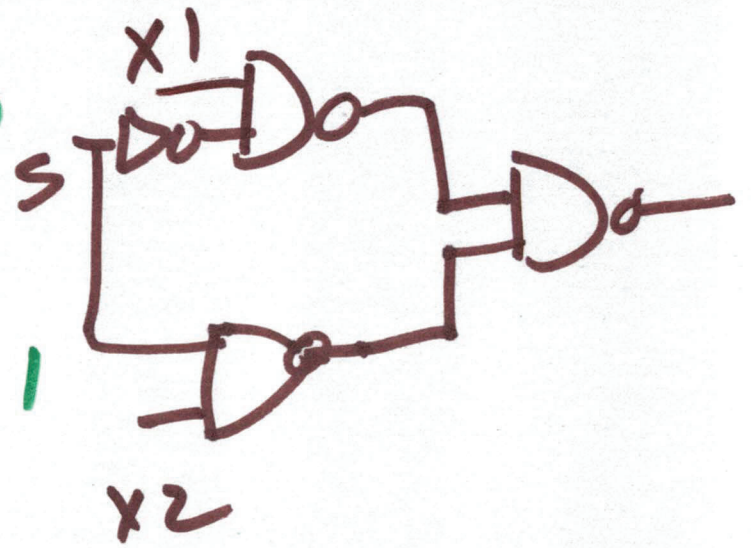
select

$$y = X_1 \cdot \bar{s} + X_2 \cdot s$$



$$y = \begin{cases} X_1 & s=0 \end{cases}$$

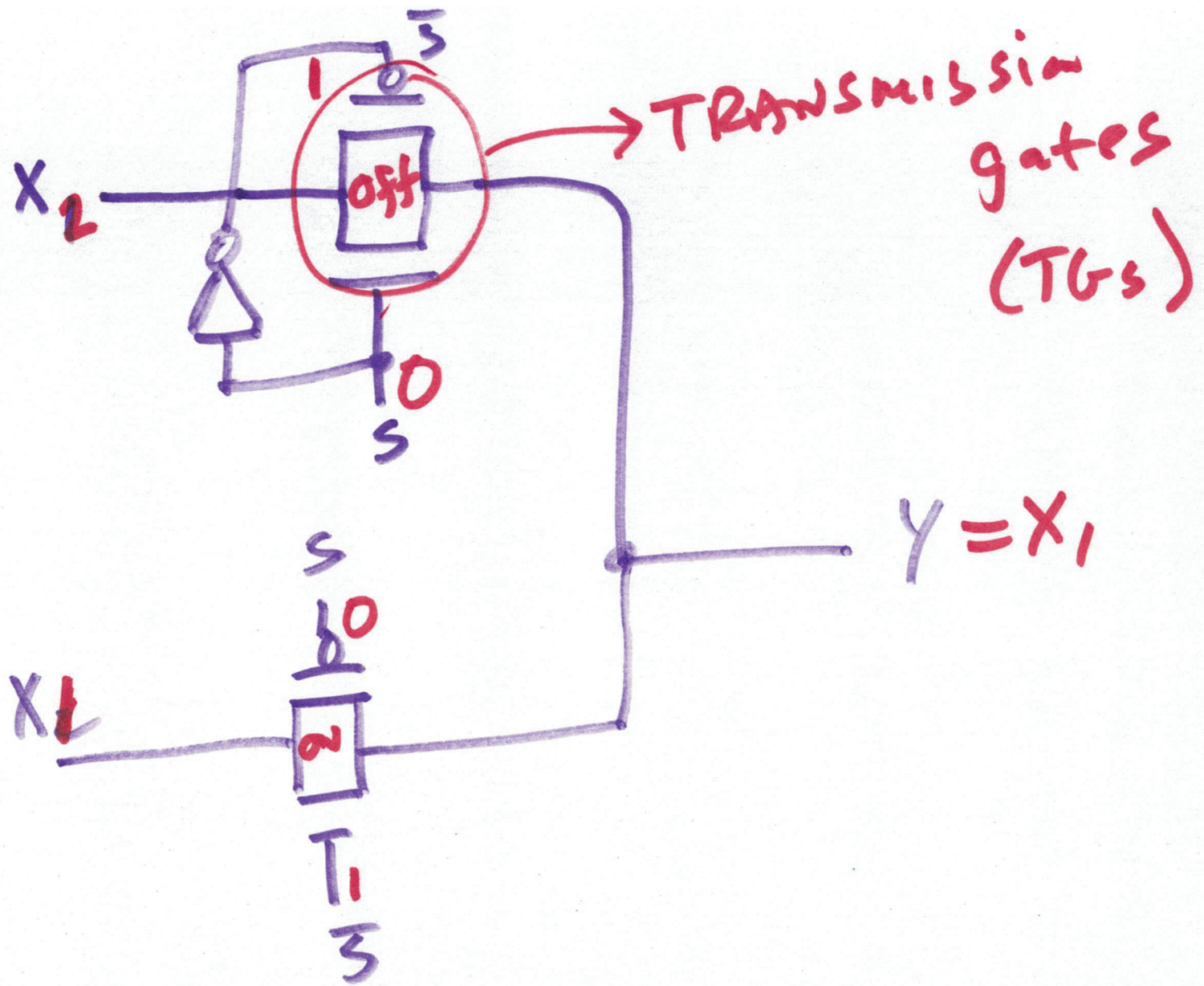
$$y = \begin{cases} X_2 & s=1 \end{cases}$$



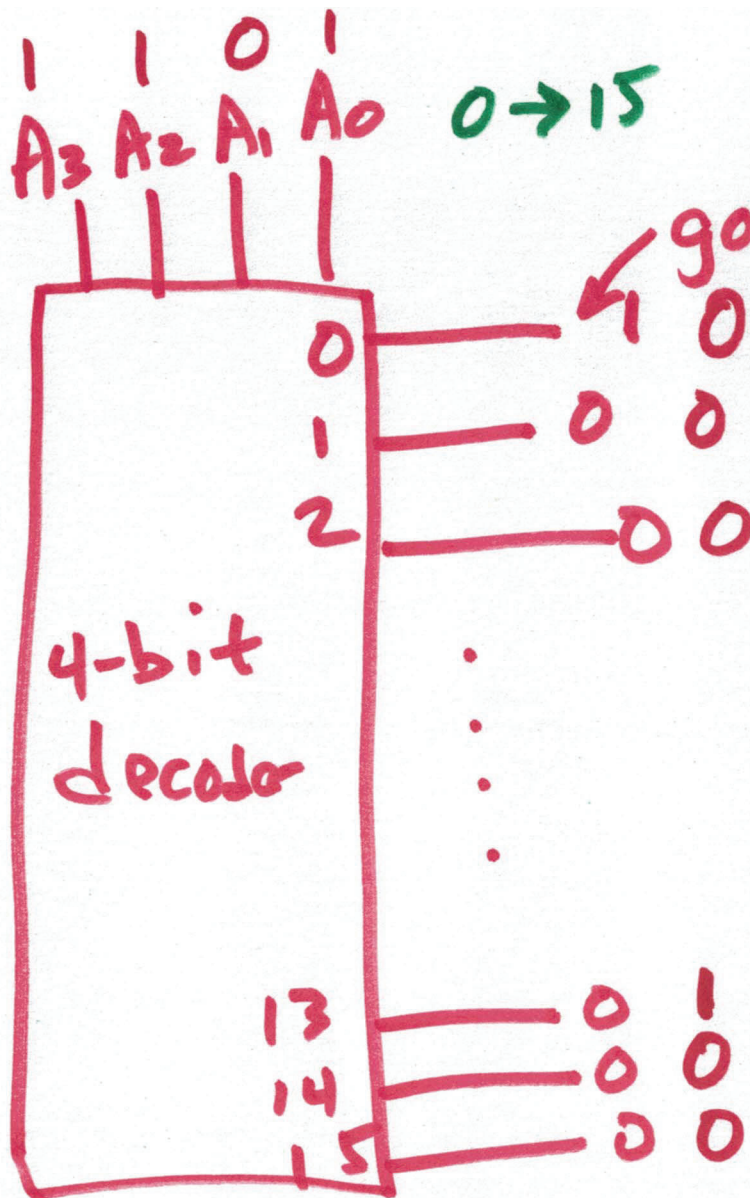
$$y = X_2 + 0 = X_2$$

4)





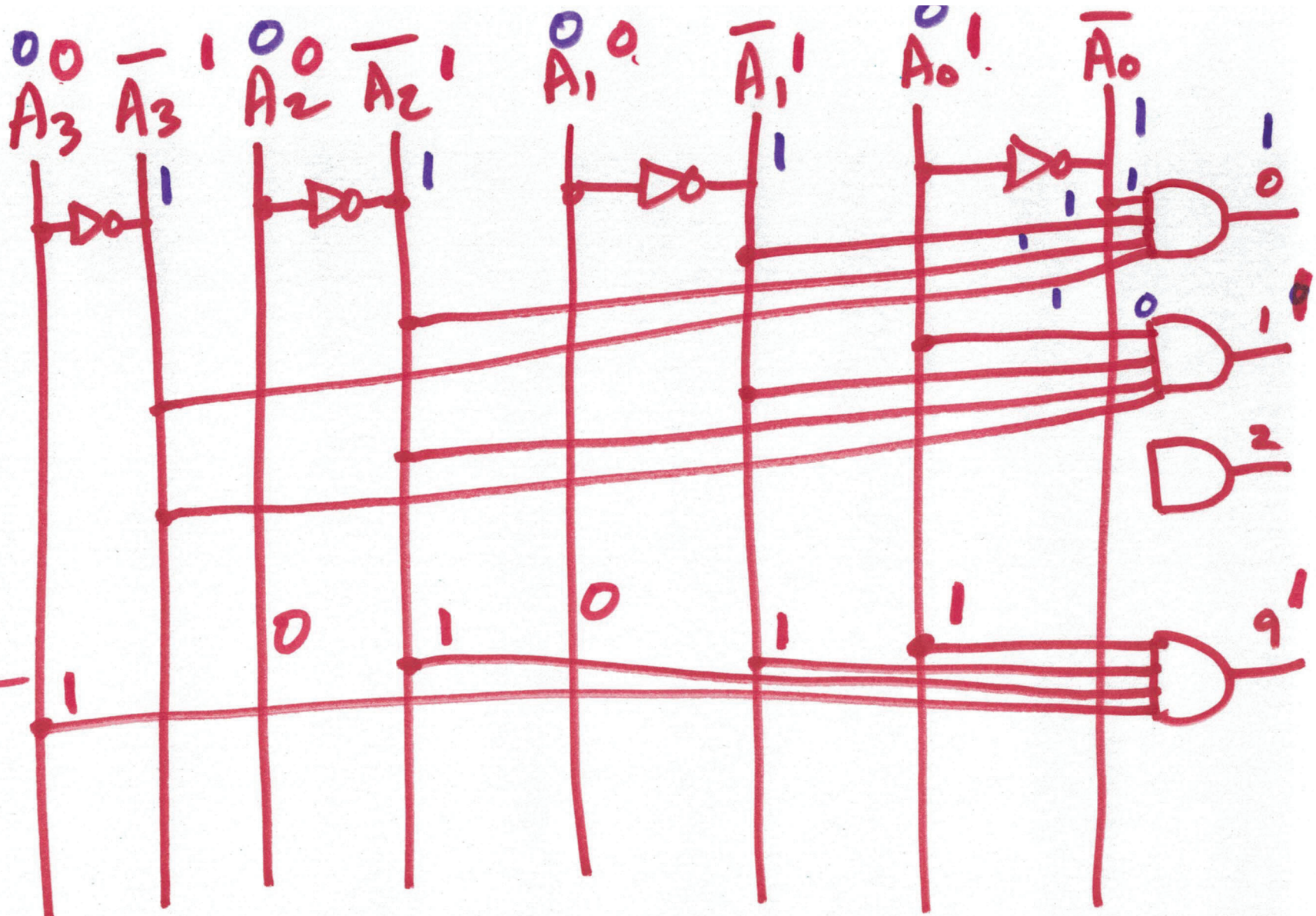
5)



0000  
 1111  $\downarrow$  15

61





$00$   $\bar{1}$   $00$   $\bar{1}$   $0$   $\bar{1}$   $0$   $\bar{1}$   
 $A_3$   $A_3$   $A_2$   $A_2$   $A_1$   $A_1$   $A_0$   $A_0$

1 0 0 1