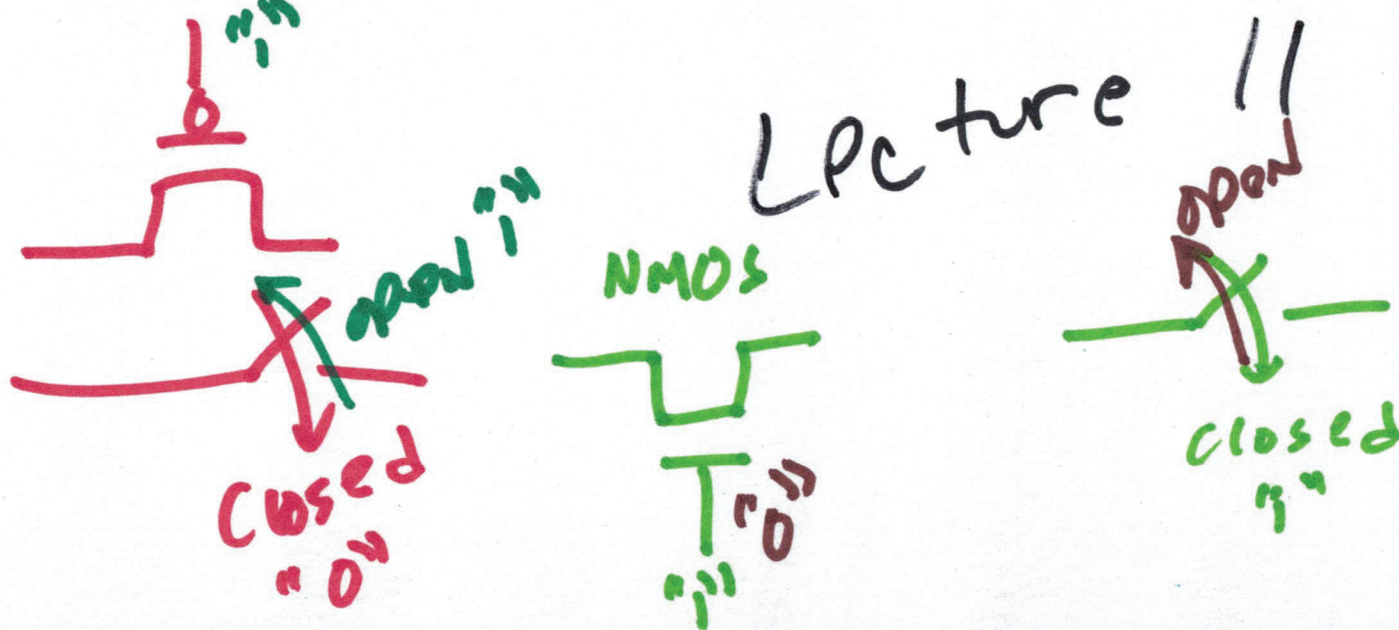


CPE 100

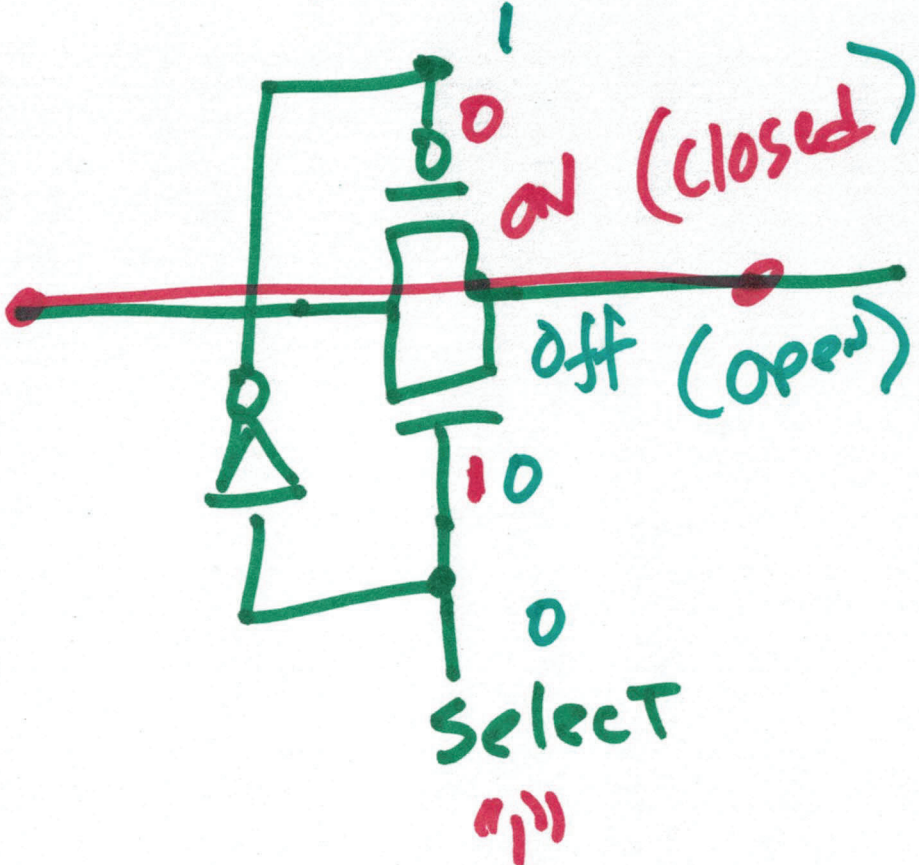
Digital Logic Design

MARCH 1, 2021

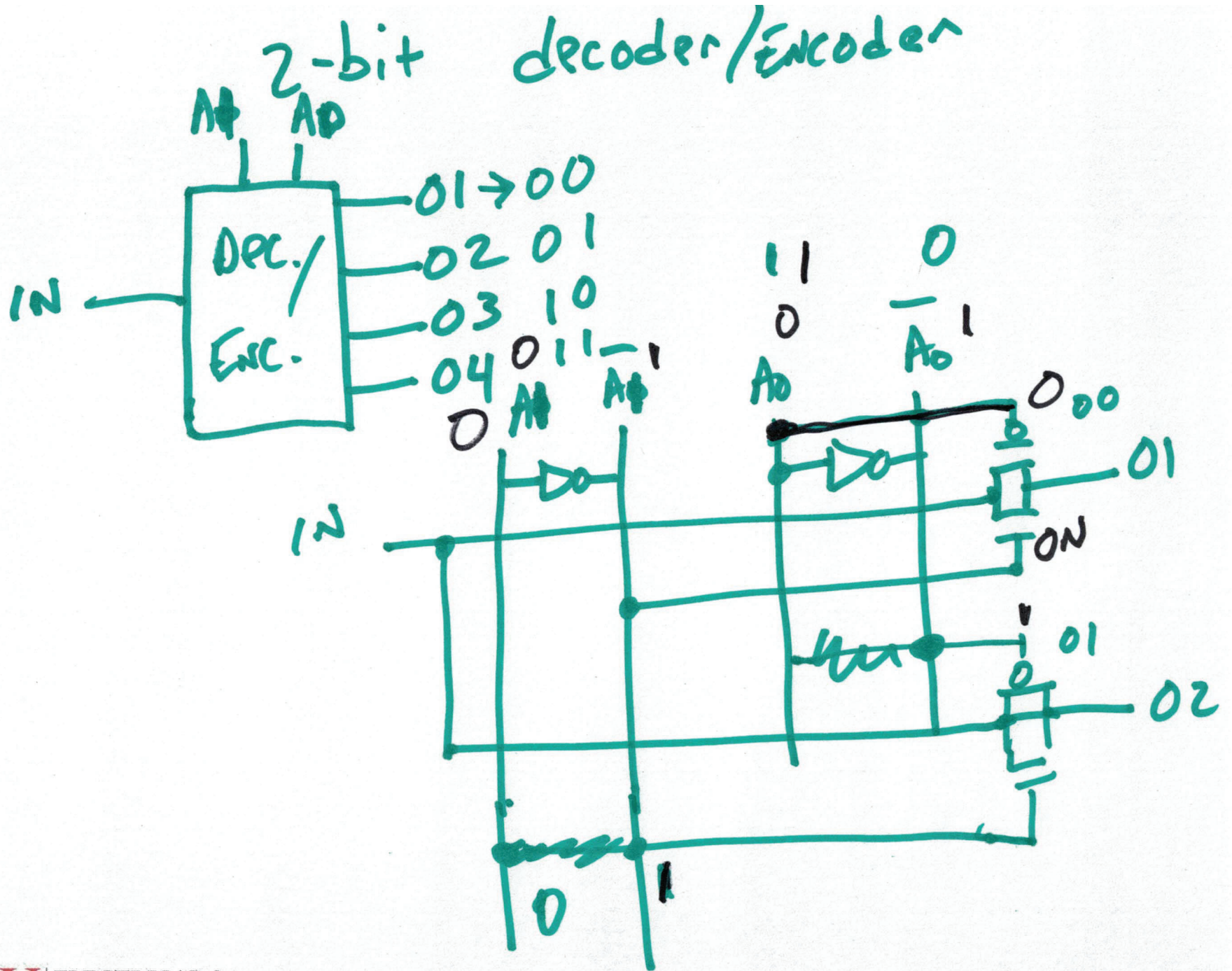


Lecture 11

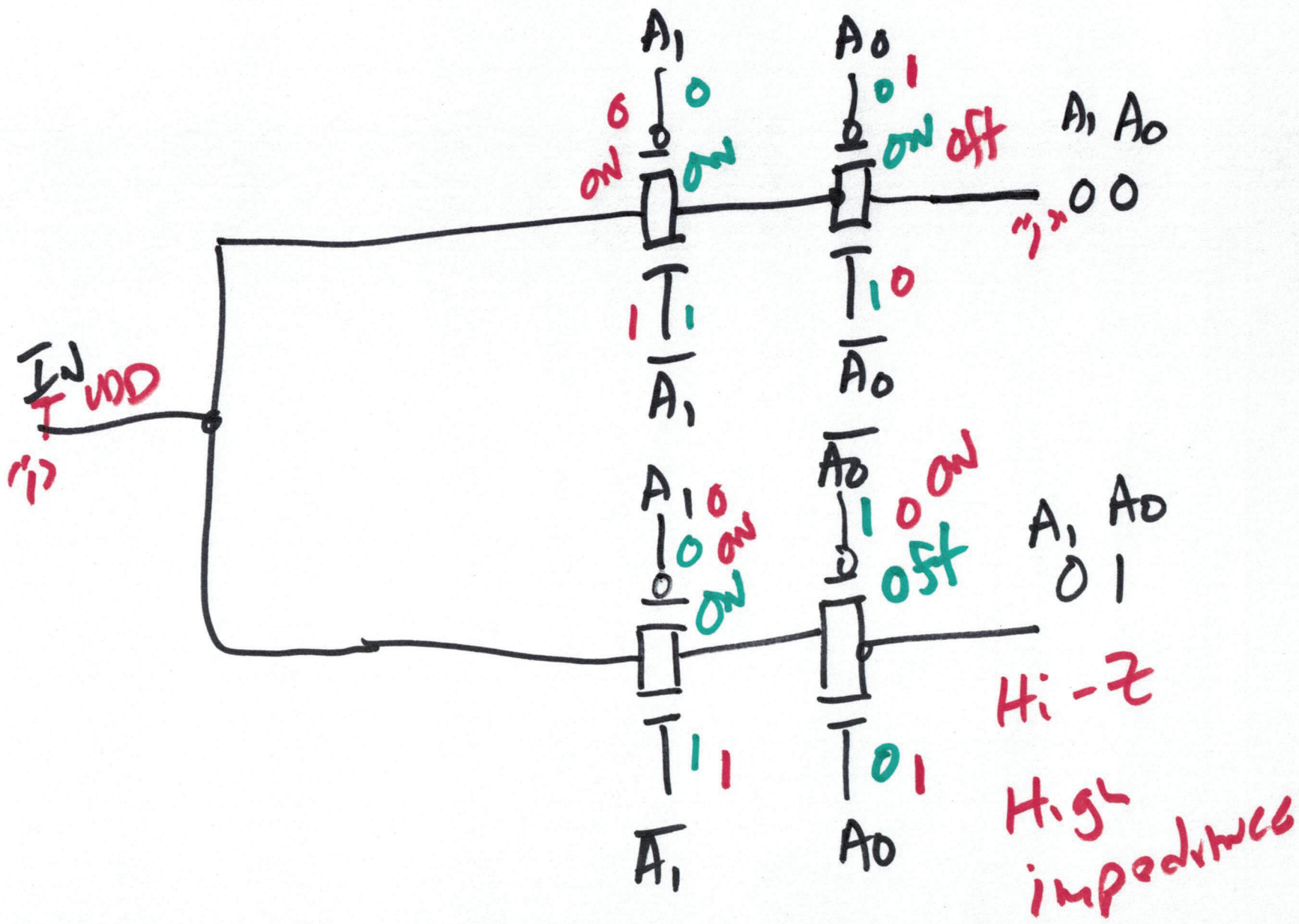
TRANSMISSION Gate



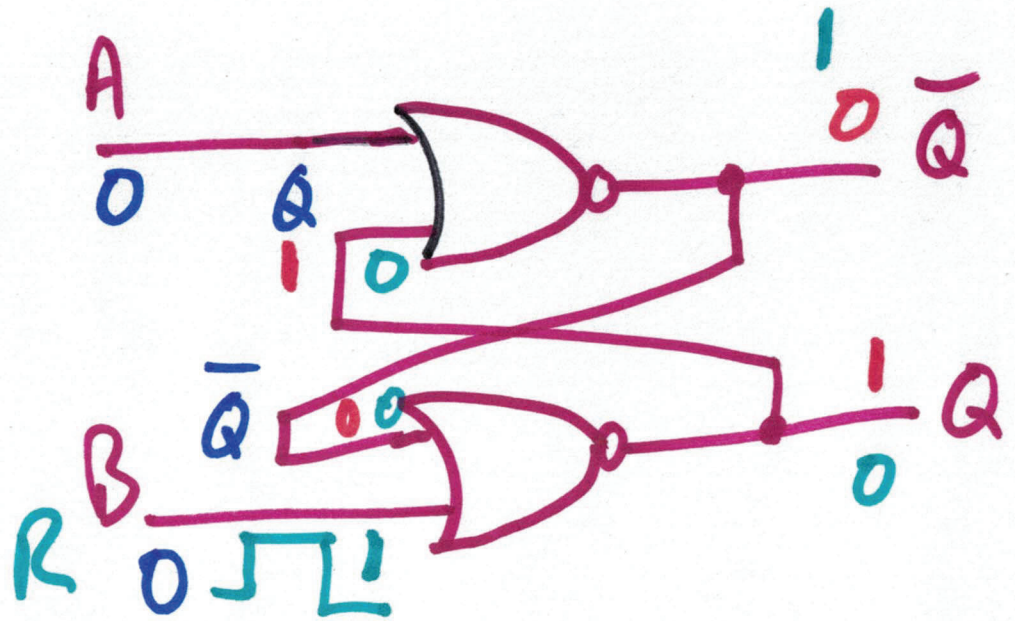
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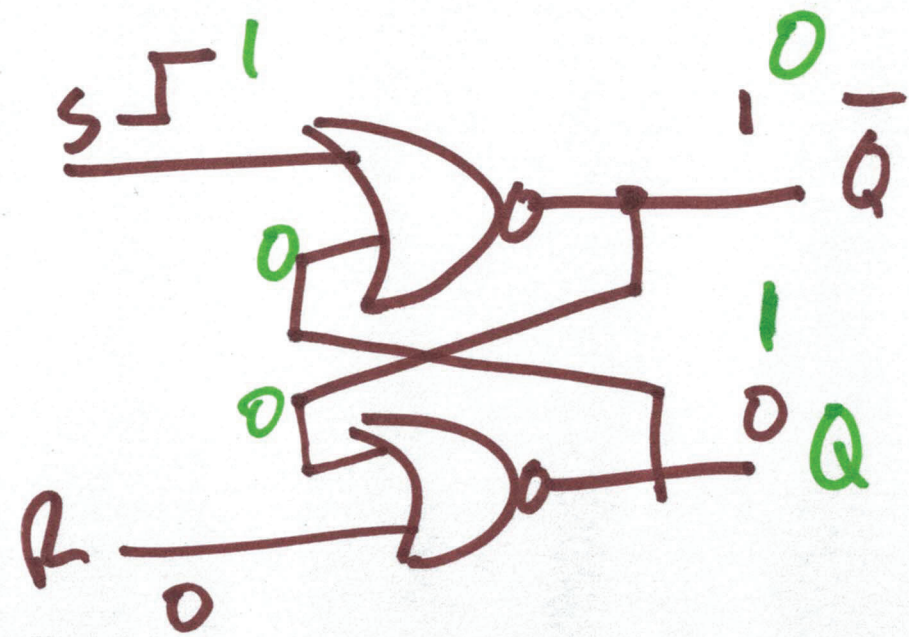
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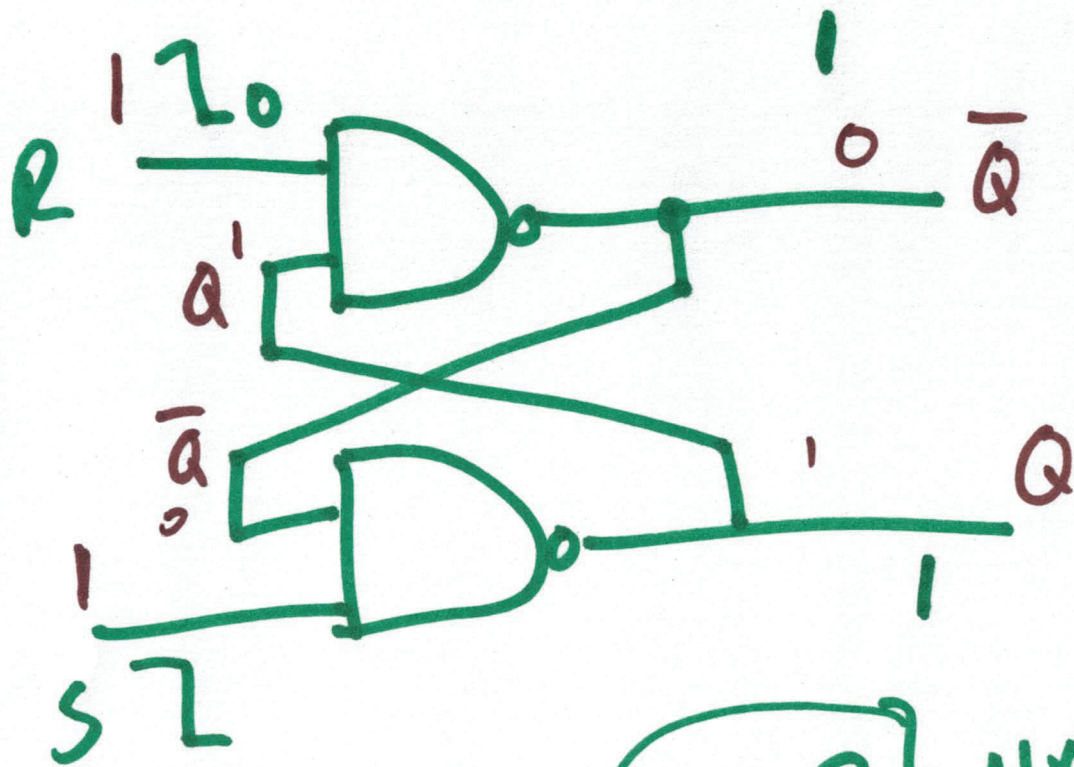


SR Latch



A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0





A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

SR NAND
Latch