CpE 100 Digital Logic Design

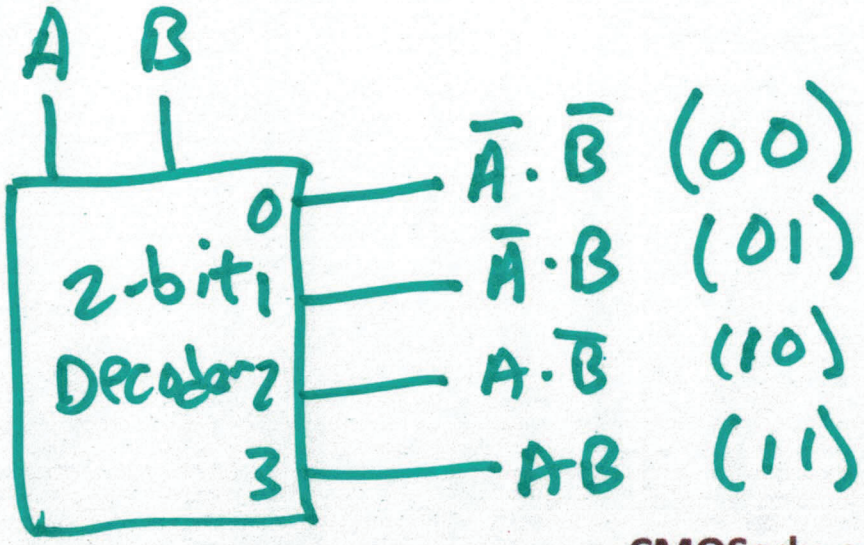
MARch 3, 2021

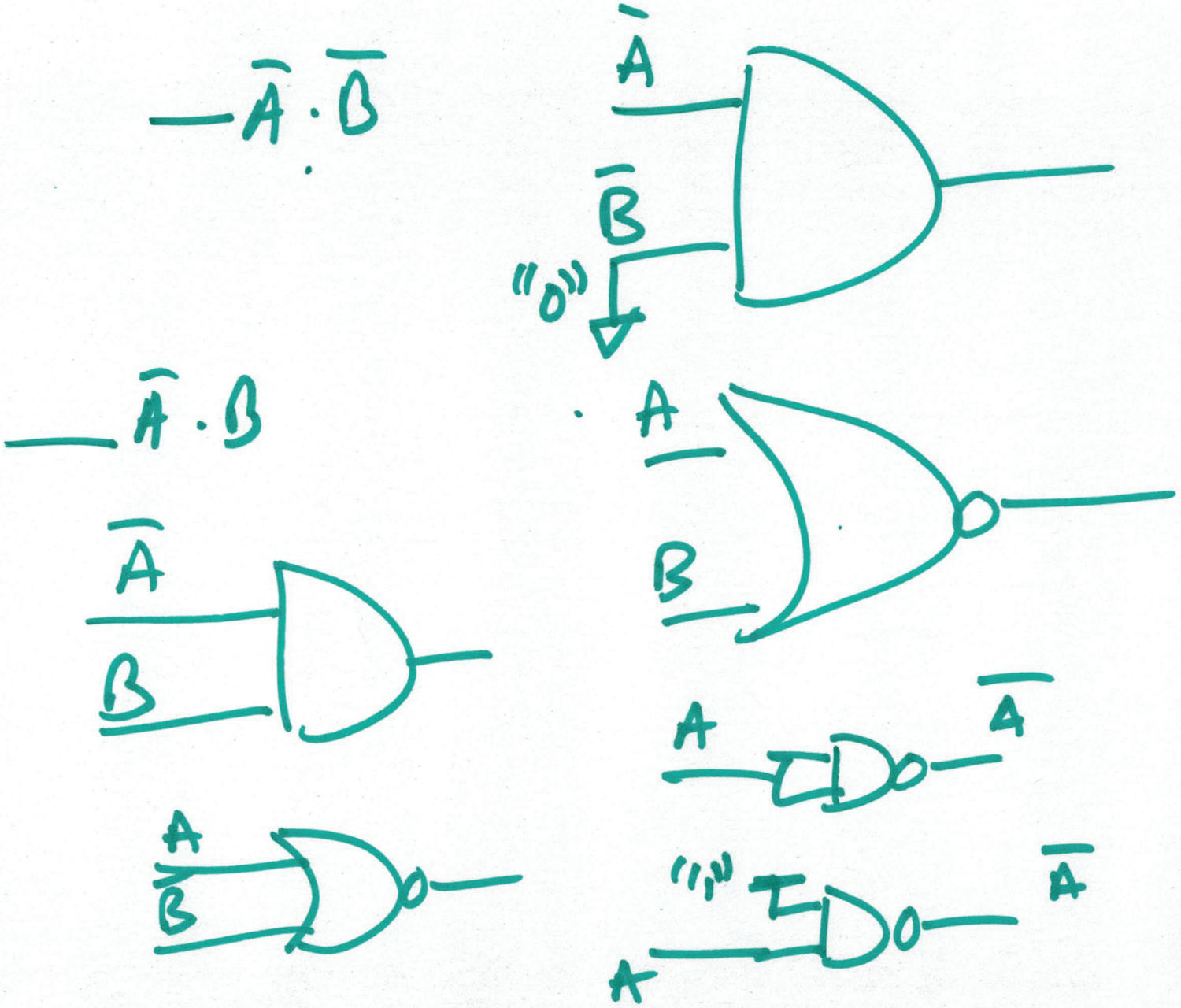
1080

1080

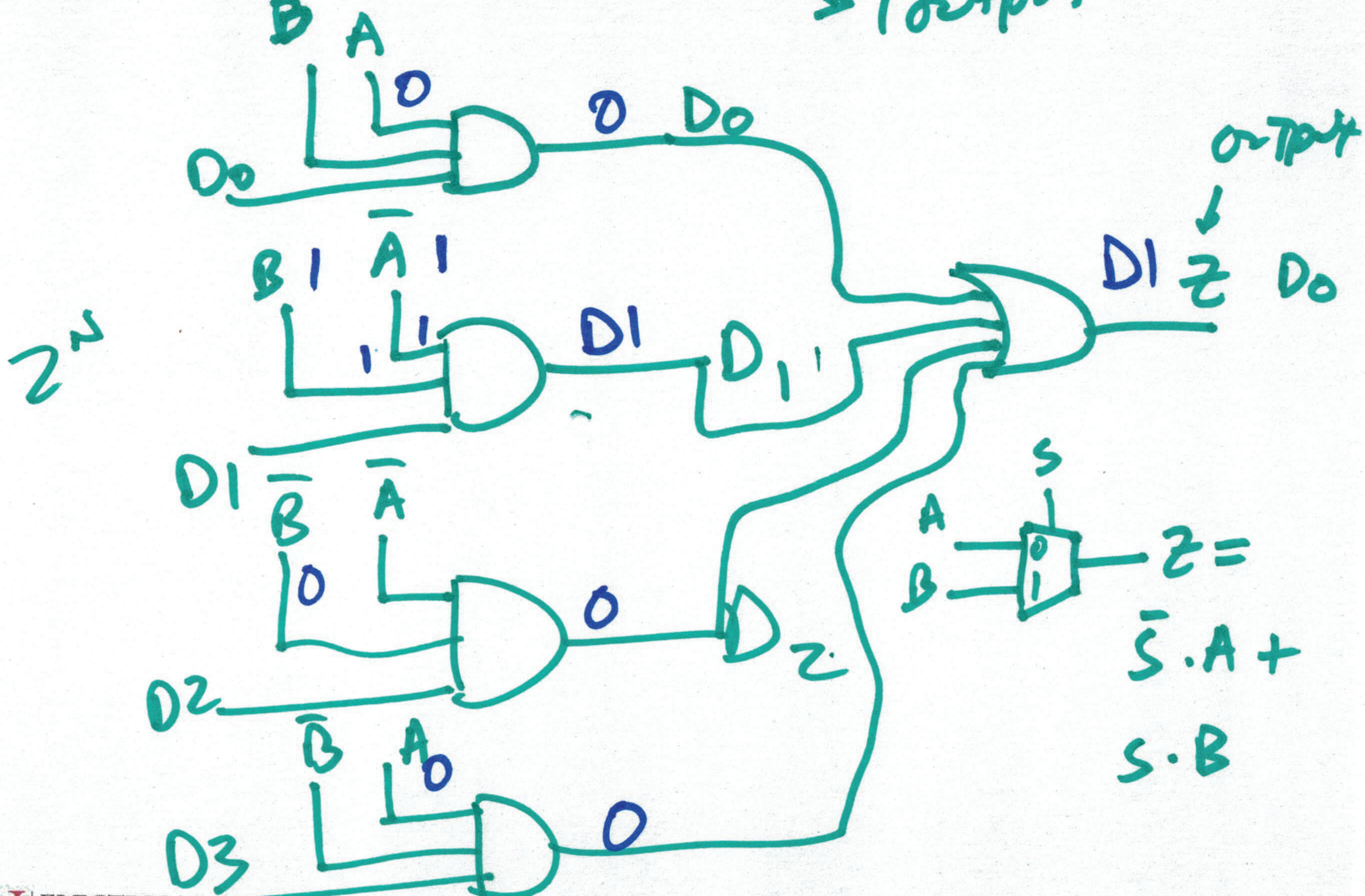
Lecture 12

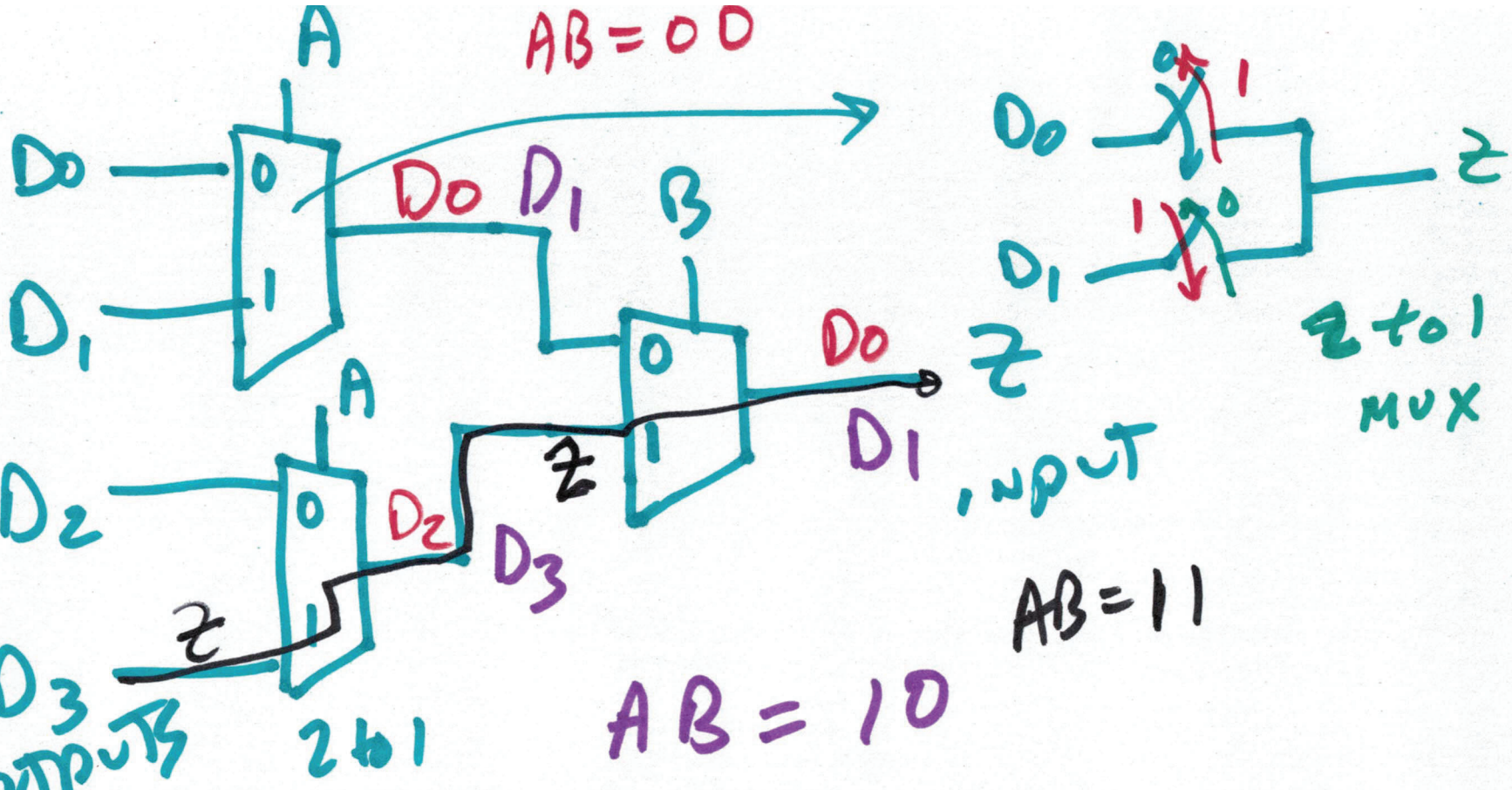
Decoder




$\overline{A} \cdot \overline{B}$
$\overline{A}$
$\overline{B}$
"0"
$\overline{A} \cdot B$
A
B
$\overline{A}$
B
A
$\overline{A}$
A
B
"1"
A
$\overline{A}$

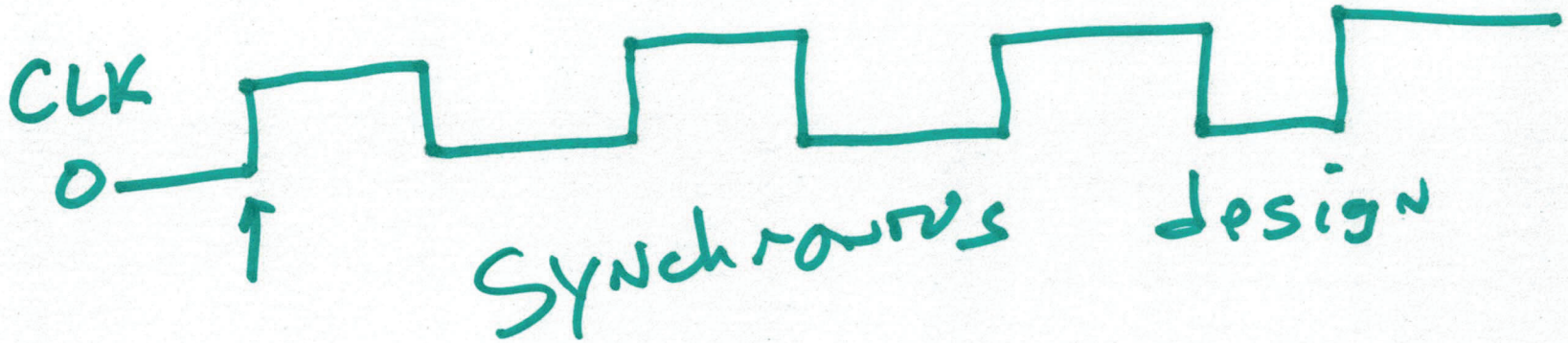
B=1 A=0 2-bit selector (multiplexor) → 1 output

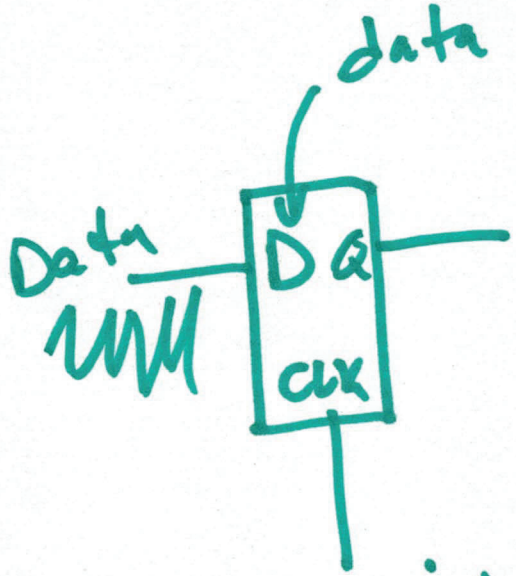




Multiplexer (many to 1)

Demultiplex (1 to many)





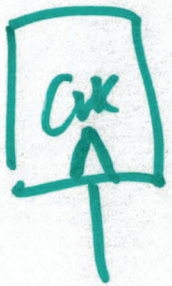
Data Flip Flop

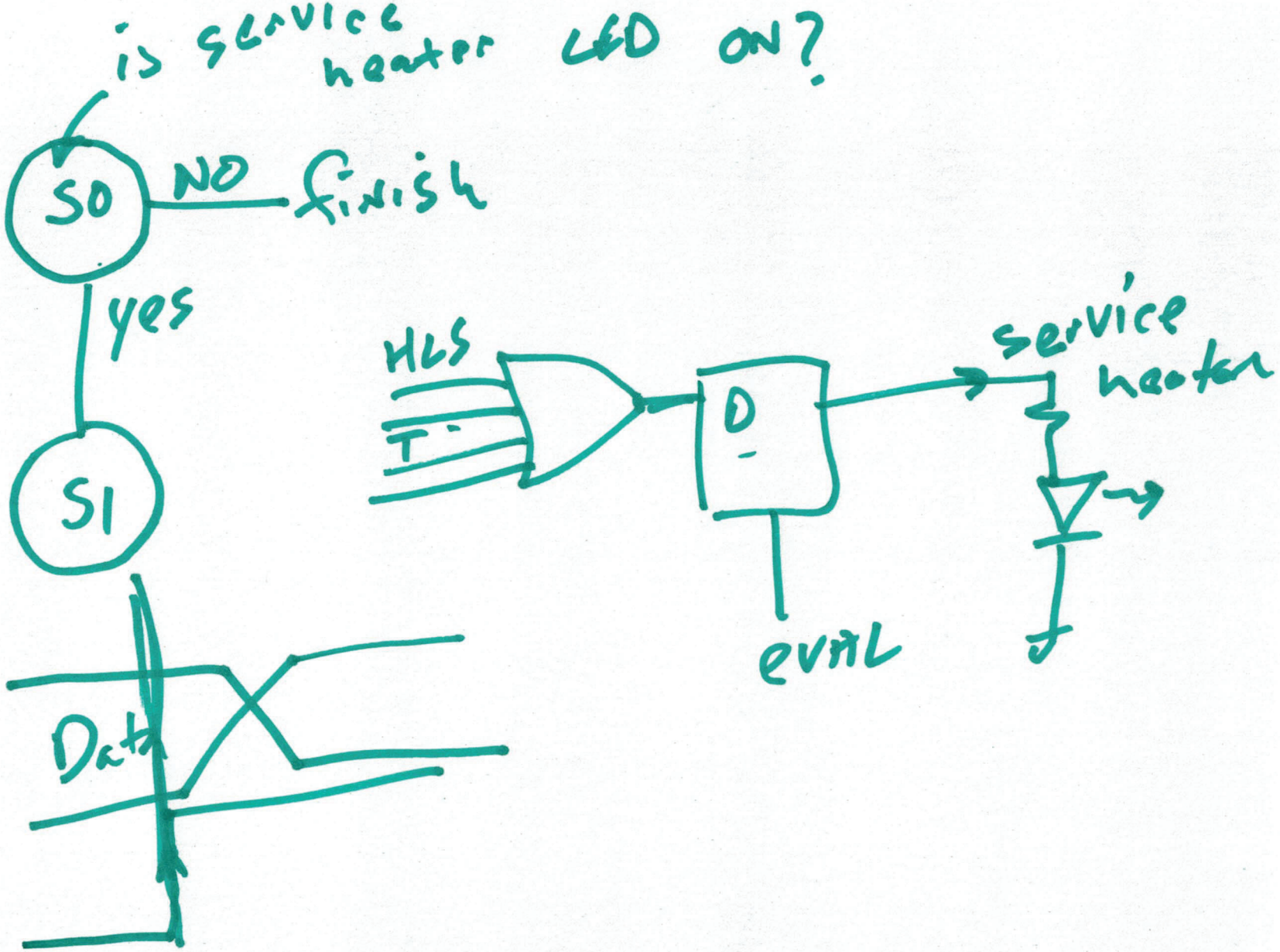
DFF

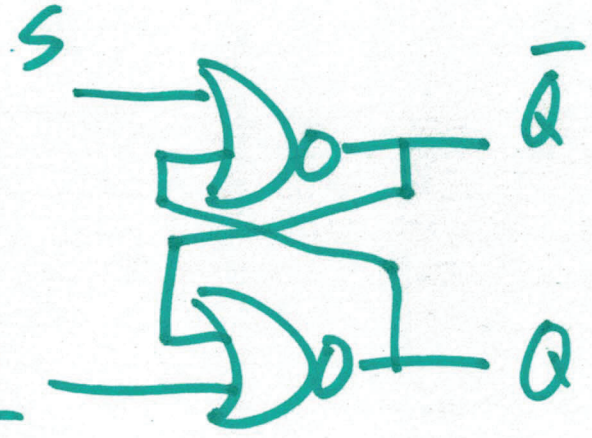
↓

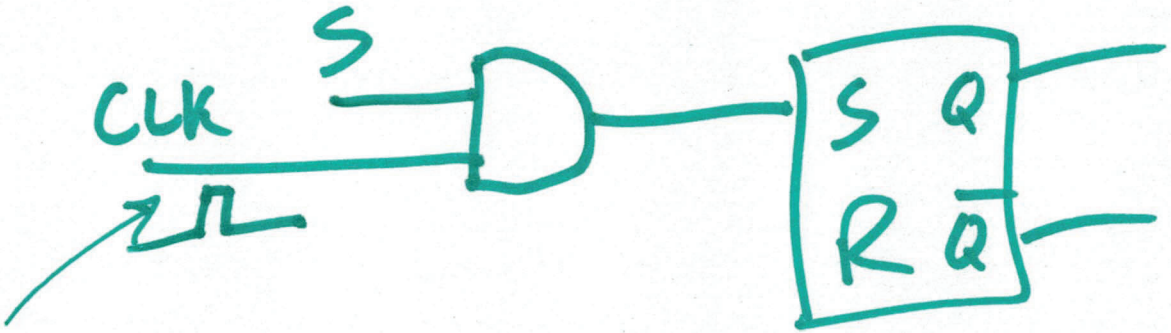
Register

positive edge triggered Flip-Flop




is service heater LED ON?
S0
NO
finish
yes
S1
Data
HLS
T-
D
evtL
service heater


S
$\bar{Q}$
R
Q


CLK
S
S Q
R $\bar{Q}$