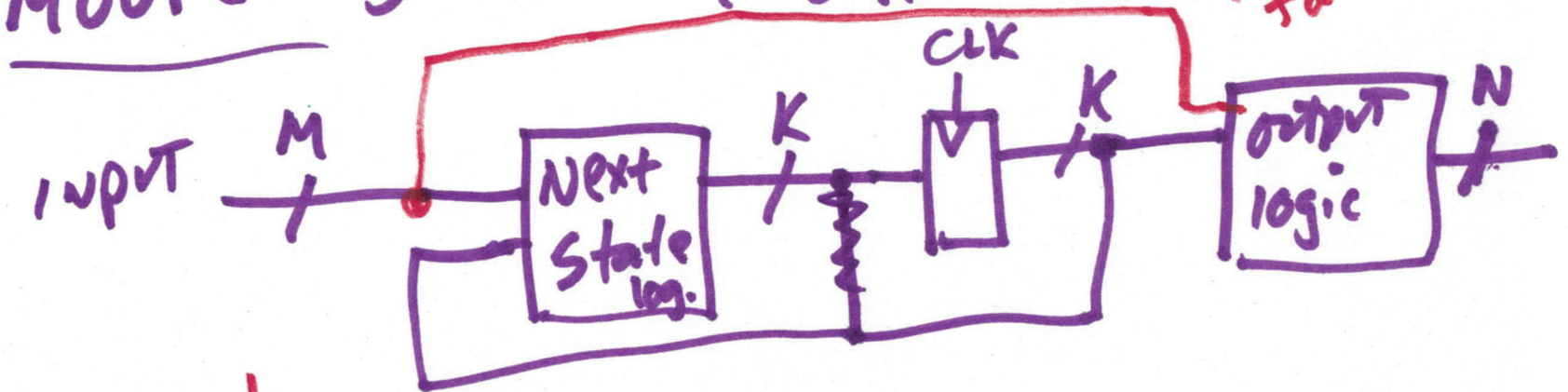


CpE 100 Digital logic Design

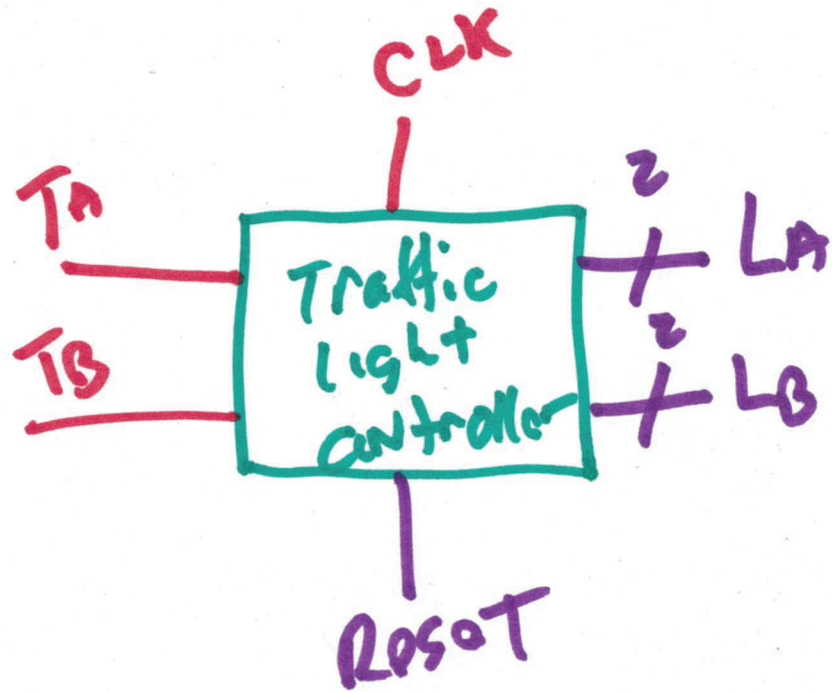
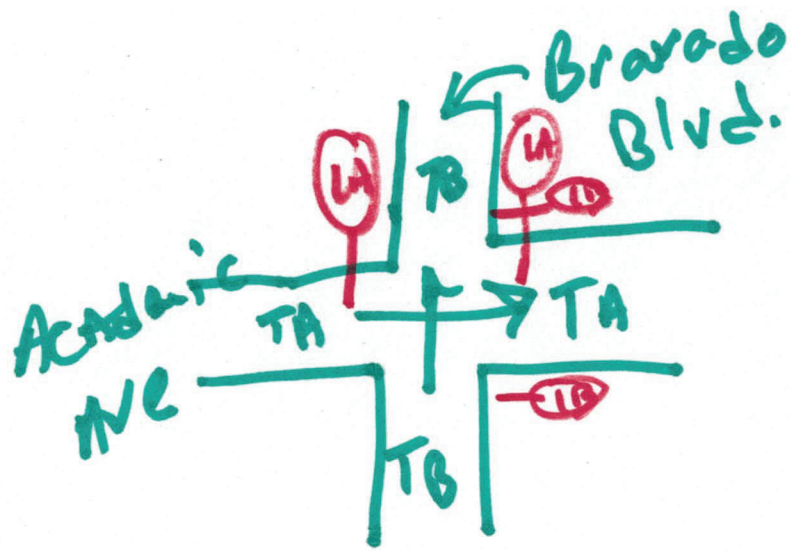
MARCH 24, 2021

Moore state machine



mealy state machine

1)



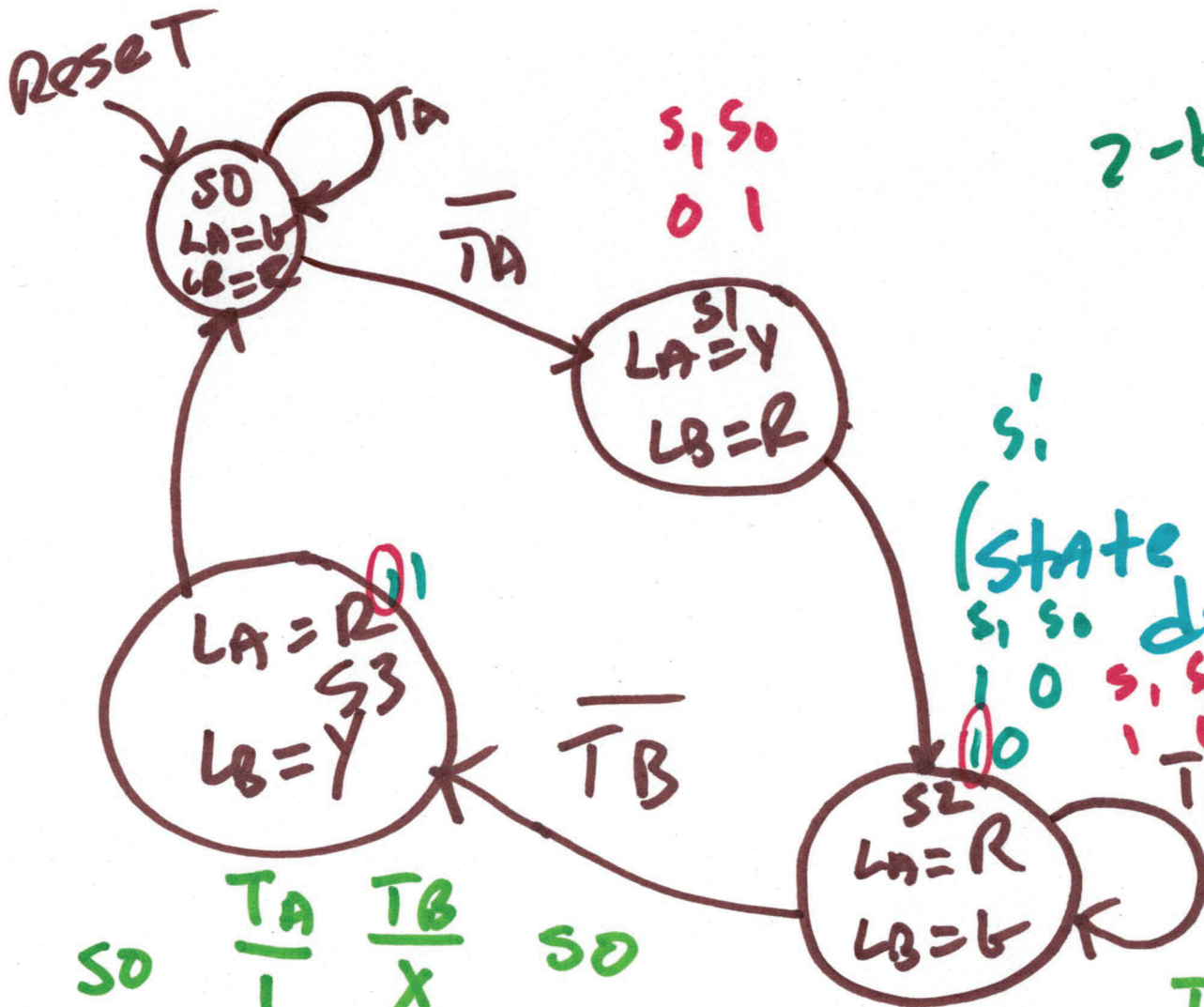
$TA = \text{true}$ then
 \downarrow traffic in the direction
 $TA = 1$
 $TA = 0$ (false) (nobody waiting)

$TB = \text{true}$ (1) people WANT to cross

$TB = 0$ (false) nobody

$f = \frac{1}{5} = 0.2 \text{ Hz}$ there

2)



2-bits
 $2^2 = 4$
 $2^2 - 1 = 3$

state diagram

FSM

S0	\overline{TA}	\overline{TB}	S0
S0	0	X	S1
S1	X	X	S2

S2	\overline{TA}	\overline{TB}	S2
S2	X	1	S3
S3	X	0	S0

3)

TABLE 3.2

State

S0

S1

S2

S3

ENCODING S_{1:0}

00

01

10

11

→ S1 S0



L1 L0

OUTPUTS

Green

Yellow

Red

ENCODING, L_{1:0}

00 ←

01

10

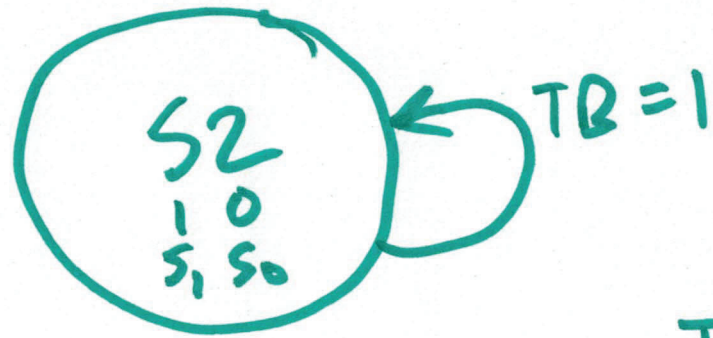
4)

State	S_1	S_0	L_{A1}^{LA}	L_{A0}	L_{B1}	L_{B0}^{LB}
S_0	0	0	0	0 (green)	1	0 (red)
S_1	0	1	0	1 (yell)	1	0 (red)
S_2	1	0	1	0 (red)	0	0 (green)
S_3	1	1	1	0 (red)	0	1 (yell)

$S_1 = 0 \quad S_0 = 0$

$$S_1' = \overline{S_1} S_0 + S_1 \overline{S_0} \overline{T_B} + S_1 \overline{S_0} T_B$$

$$S_0' = \overline{S_1} \overline{S_0} \overline{T_A} + S_1 \overline{S_0} \overline{T_B}$$



$$TB \cdot S_1 \cdot \bar{S}_0 \Rightarrow S_1 = 1$$