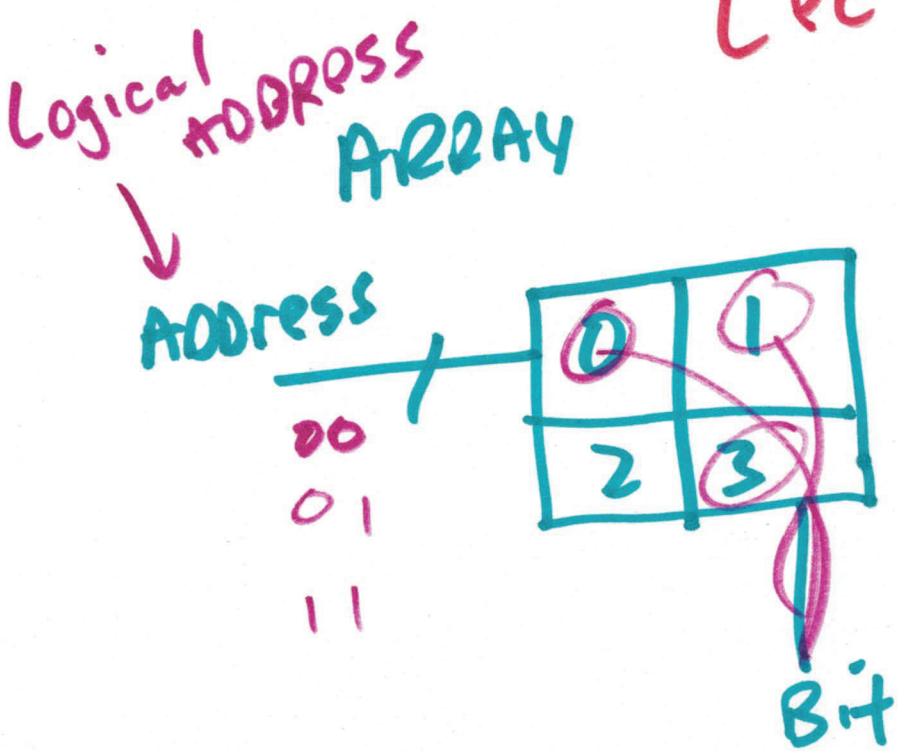
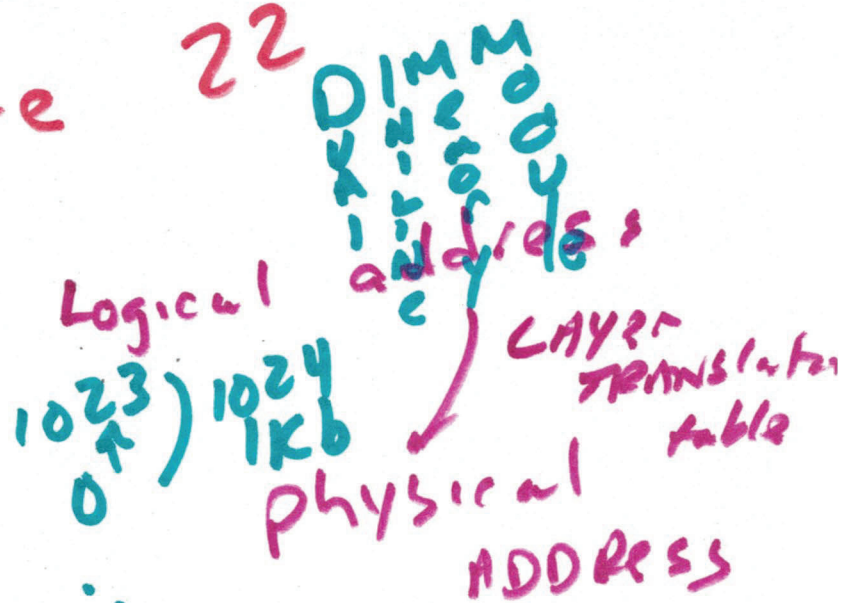
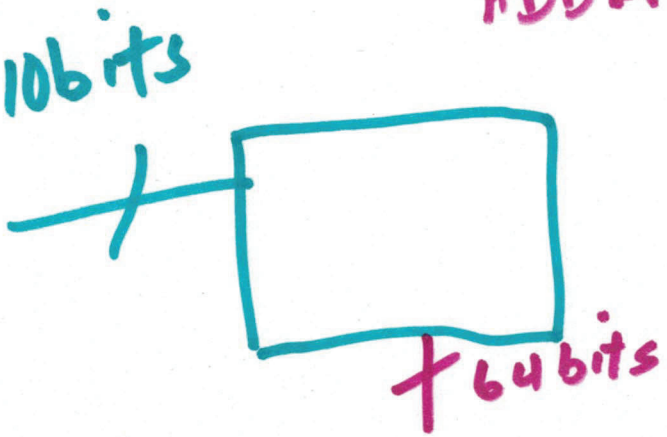
CPE 100 Digital logic Design

April 19, 2021

Lecture 22







Register file (RF)

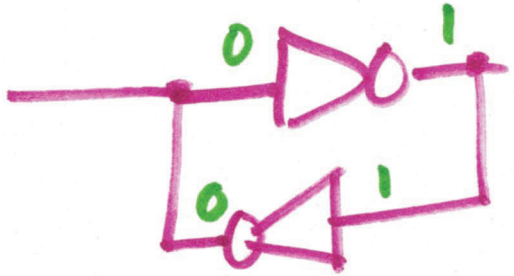
made using

Static RAM Access Memory (SRAM)

1-bit

~~Non-Volatile memory~~

~~NVM~~ Static



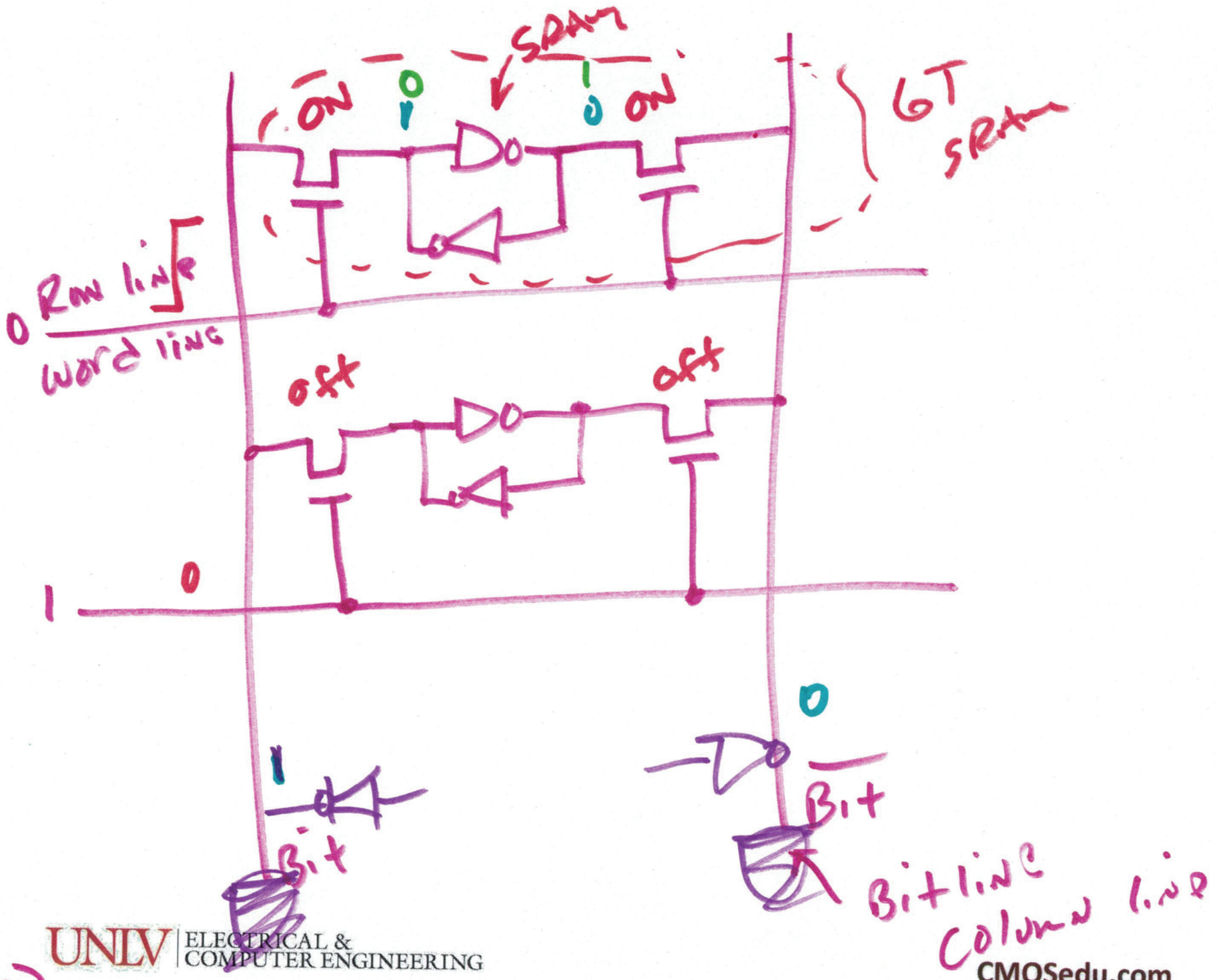
Power is applied it remembers

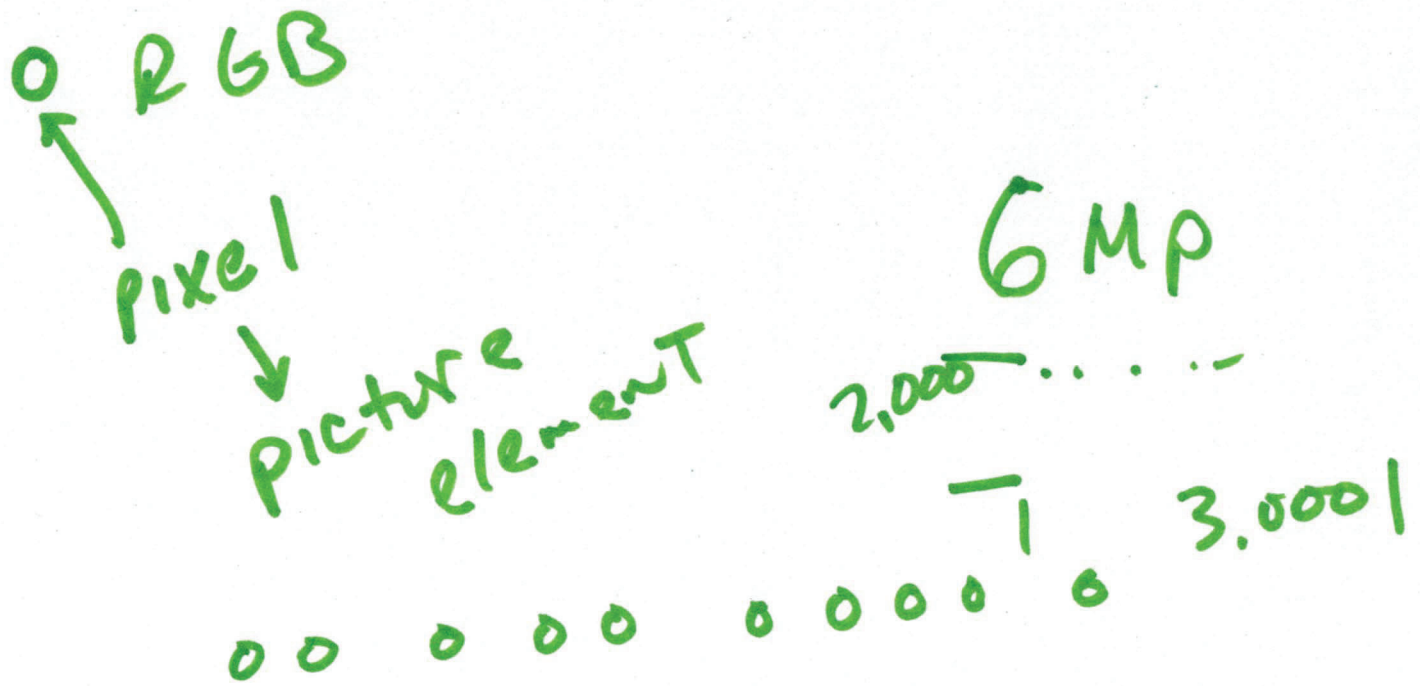
NVM

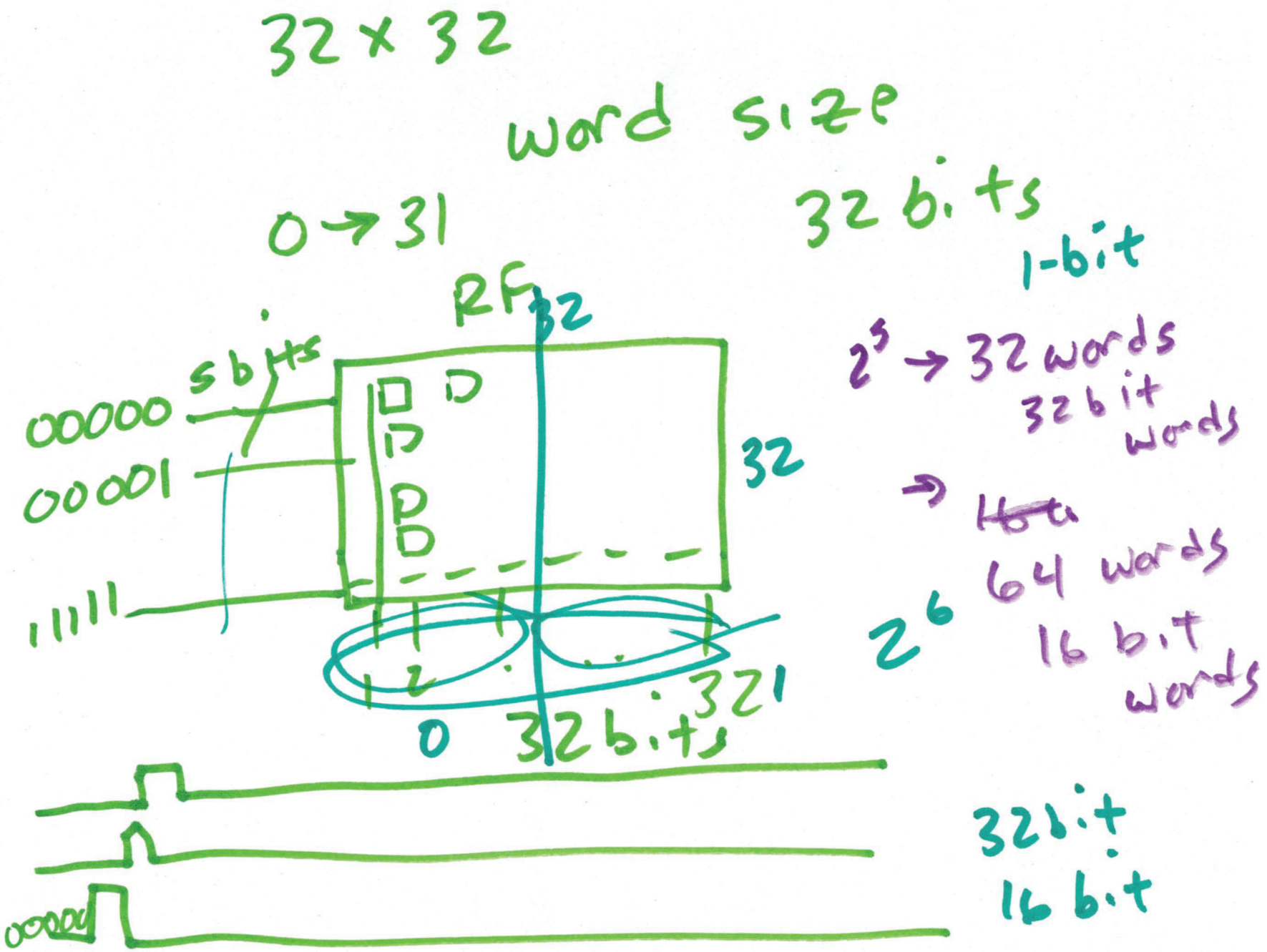
NVM is when Power is Removed it remembers

NVM ~ HDD

Flash solid state drive


SRAM
ON
0
1
1
ON
6T
SRAM
0 Row line
word line
off
off
1
0
1
Bit
0
Bit
Bit line
Column line


RGB
pixel
picture
element
6MP
2,000
3,000



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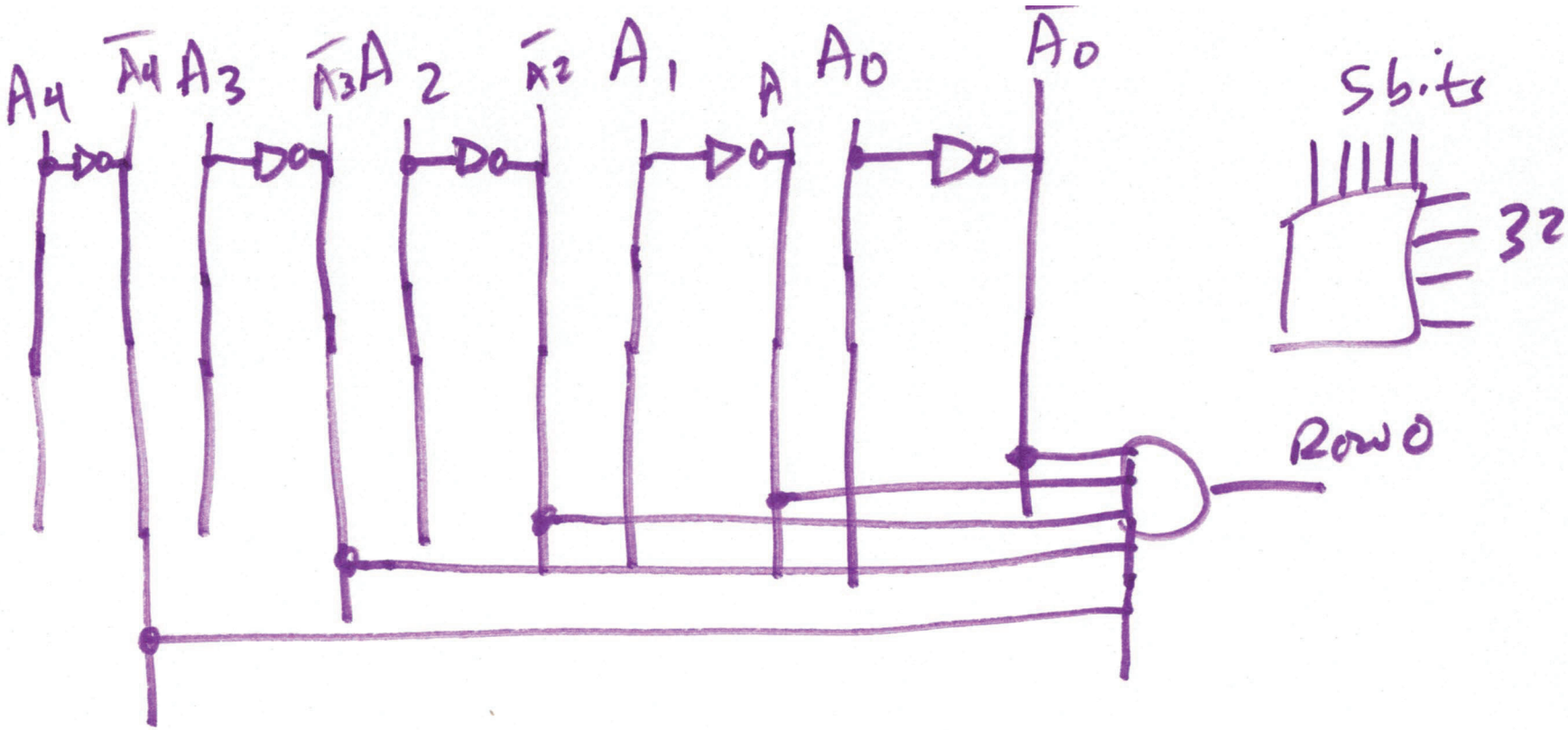
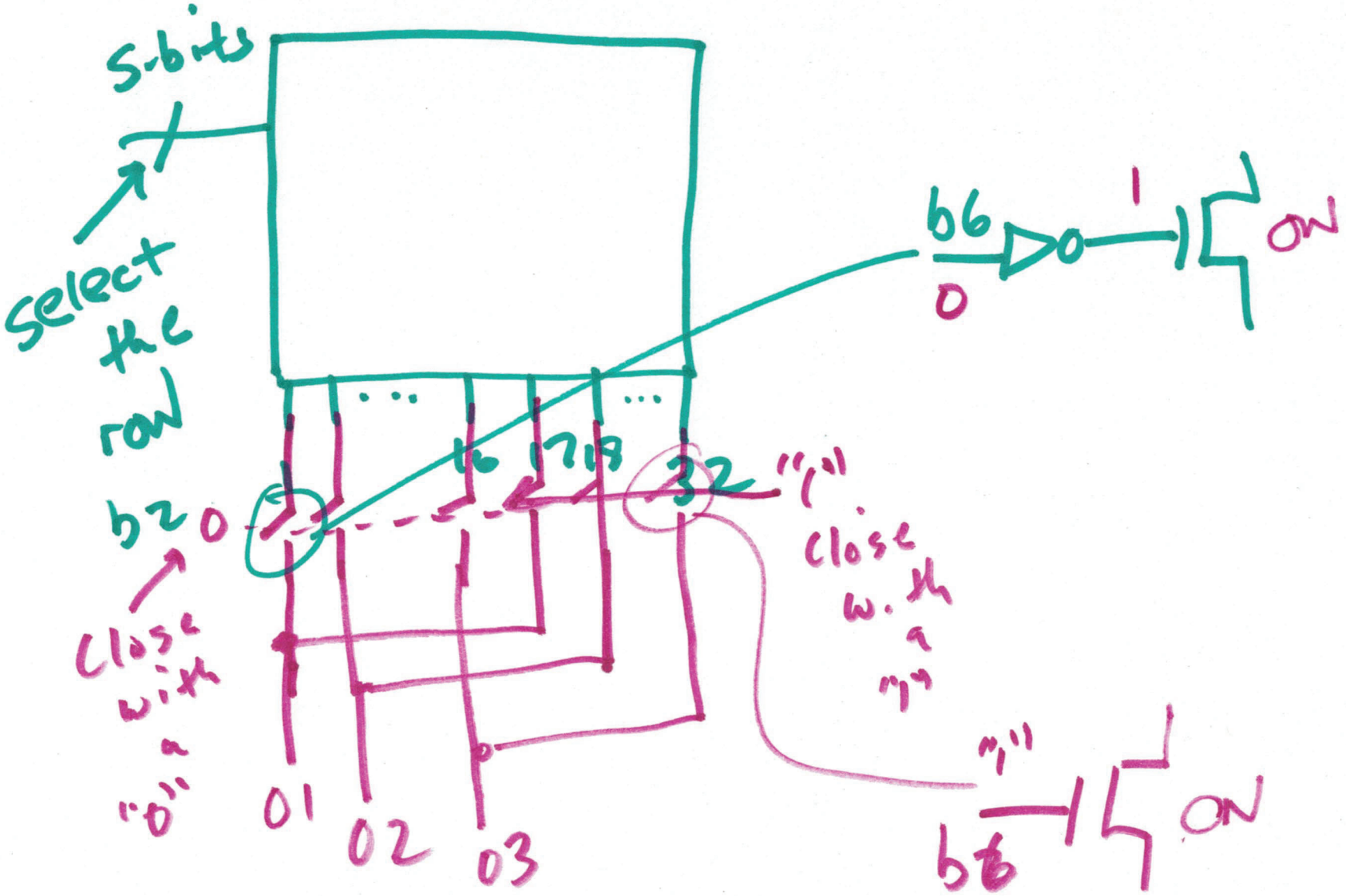

A4
A4
A3
A3
A2
A2
A1
A
A0
A0
5 bits
32
Row 0


5-bits
Select the row
b6
0
1
ON
b2
0
16
17/18
32
"1"
Close with a "1"
Close w. th a "1"
"0"
01
02
03
"1"
b6
ON

32 x 32 RF

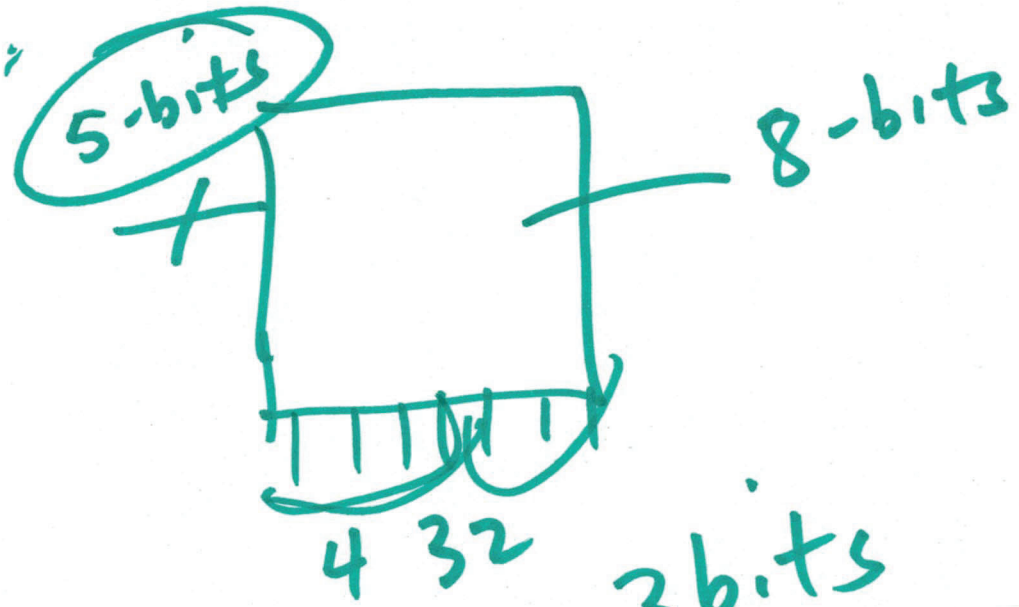
32 4-bit words

32

32 32x32

$\frac{32 \cdot 32}{4}$ = # of words

256

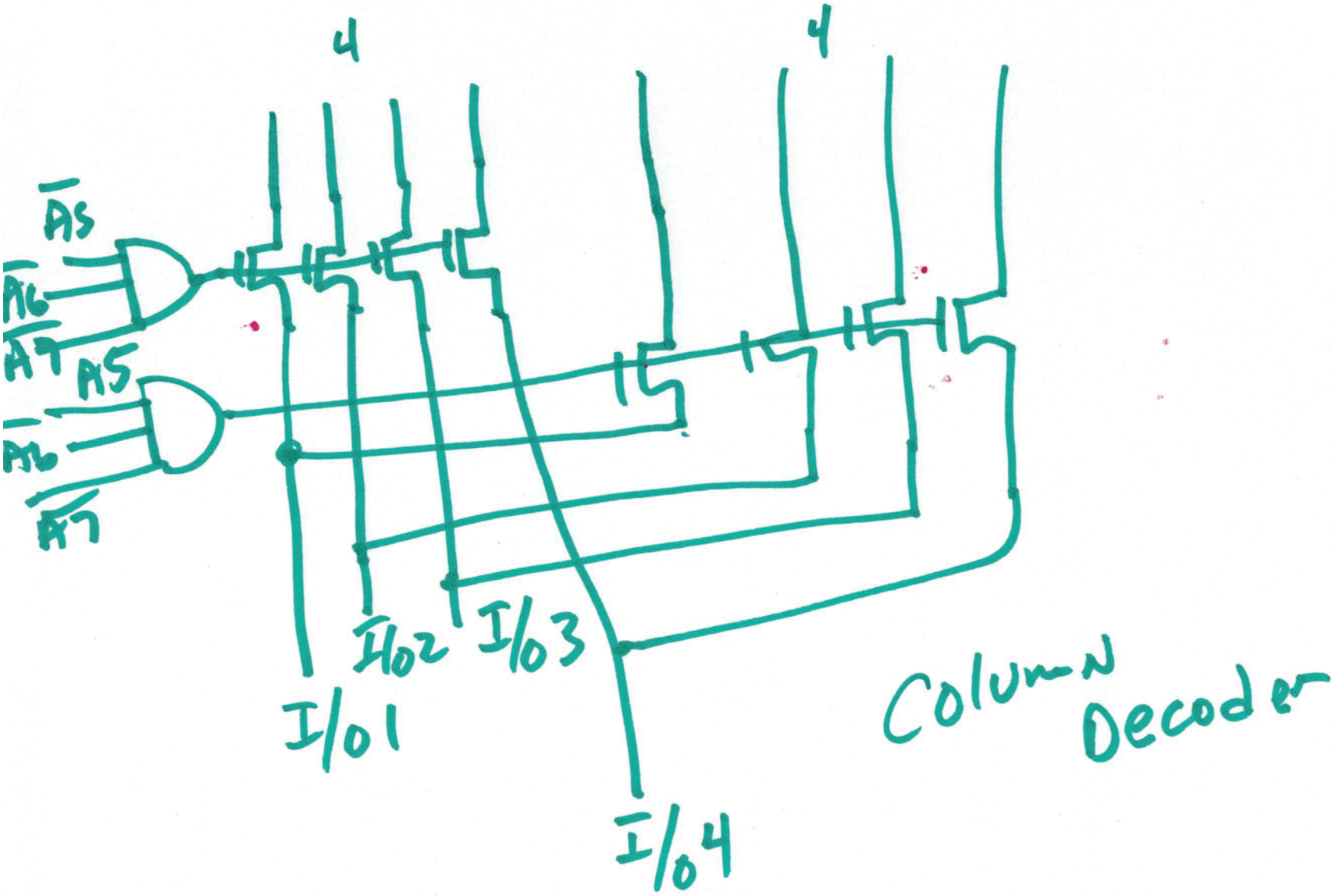


8 → 3 bits

000

001

111


4
4
$\overline{A5}$
$\overline{A6}$
$\overline{A7}$
A5
$\overline{A6}$
$\overline{A7}$
I/O1
$\overline{I/O2}$
I/O3
$\overline{I/O4}$
Column Decoder