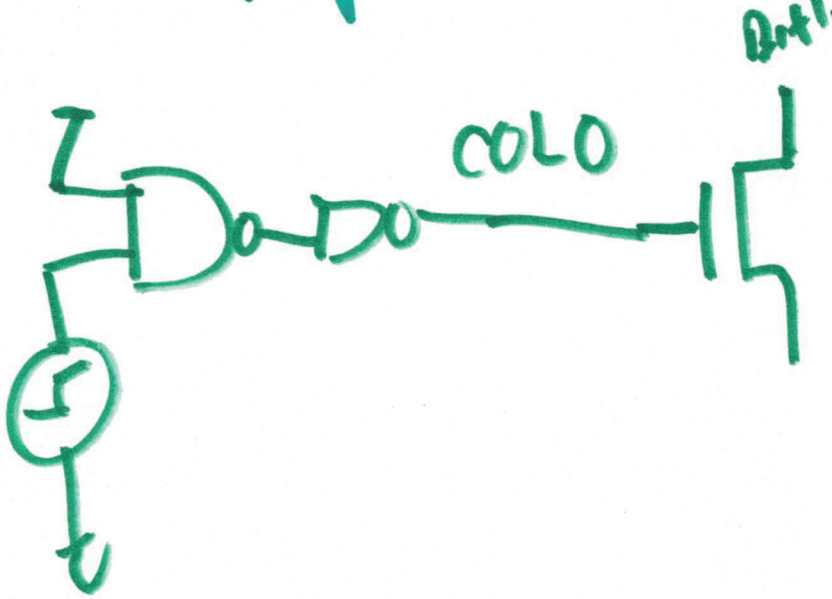
Lecture 24

CPE 100 Digital logic Design

April 26, 2021



SRAM Static RAM

Register file

Levels of CACHE

central processing unit

Micro Controller

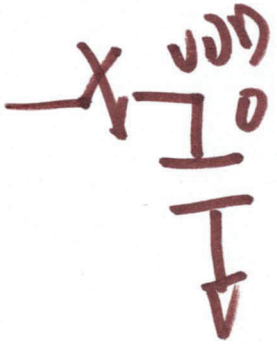
Apps Processor

Cellular Baseband modem processor

CPU
- Core cores
  - ALU
  - RF
  - Cache
- Interrupt Controller
- Controllers on chip
  - PCIe
  - USB
  - SSD

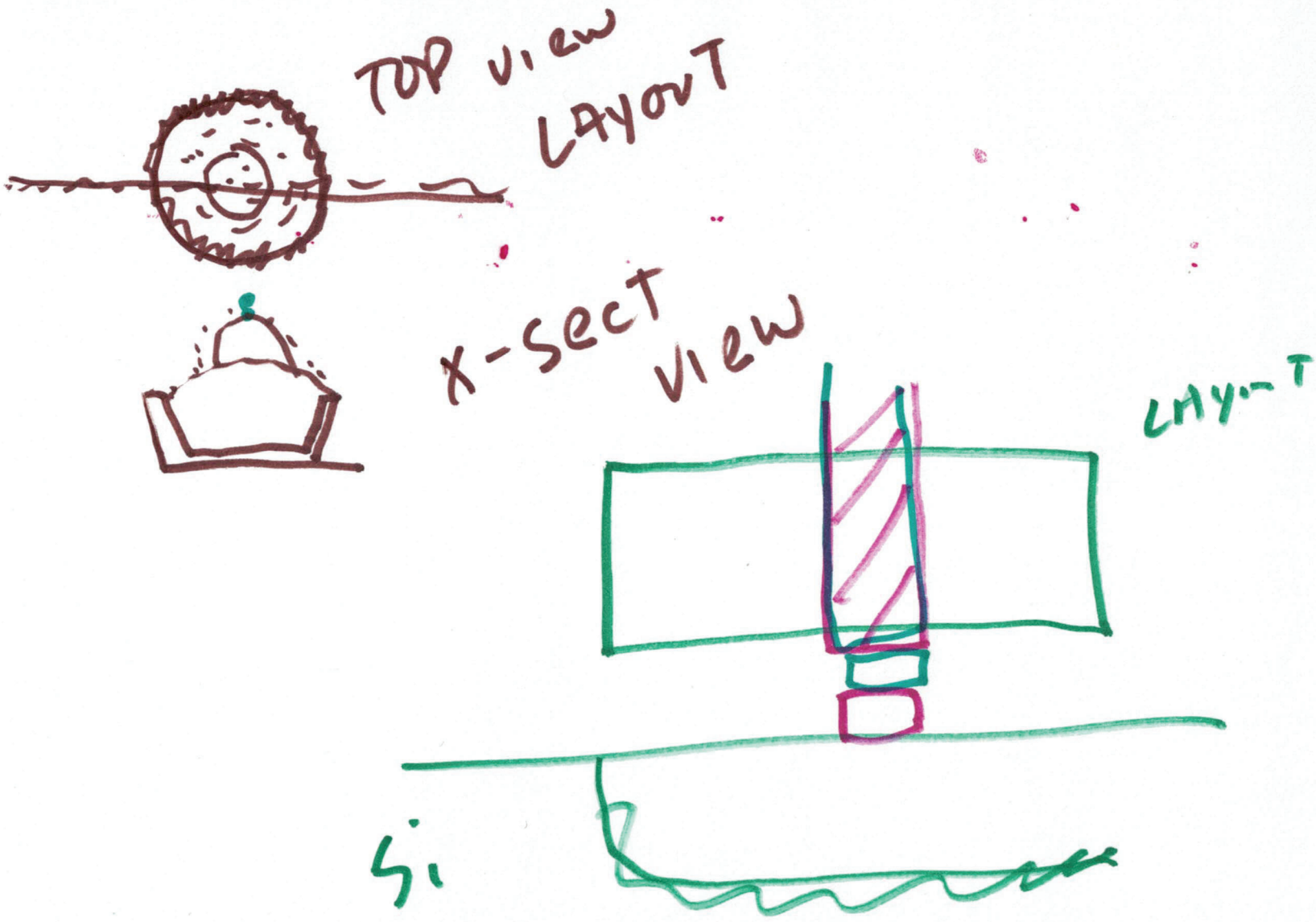
Dynamic RAm
"computer memory"

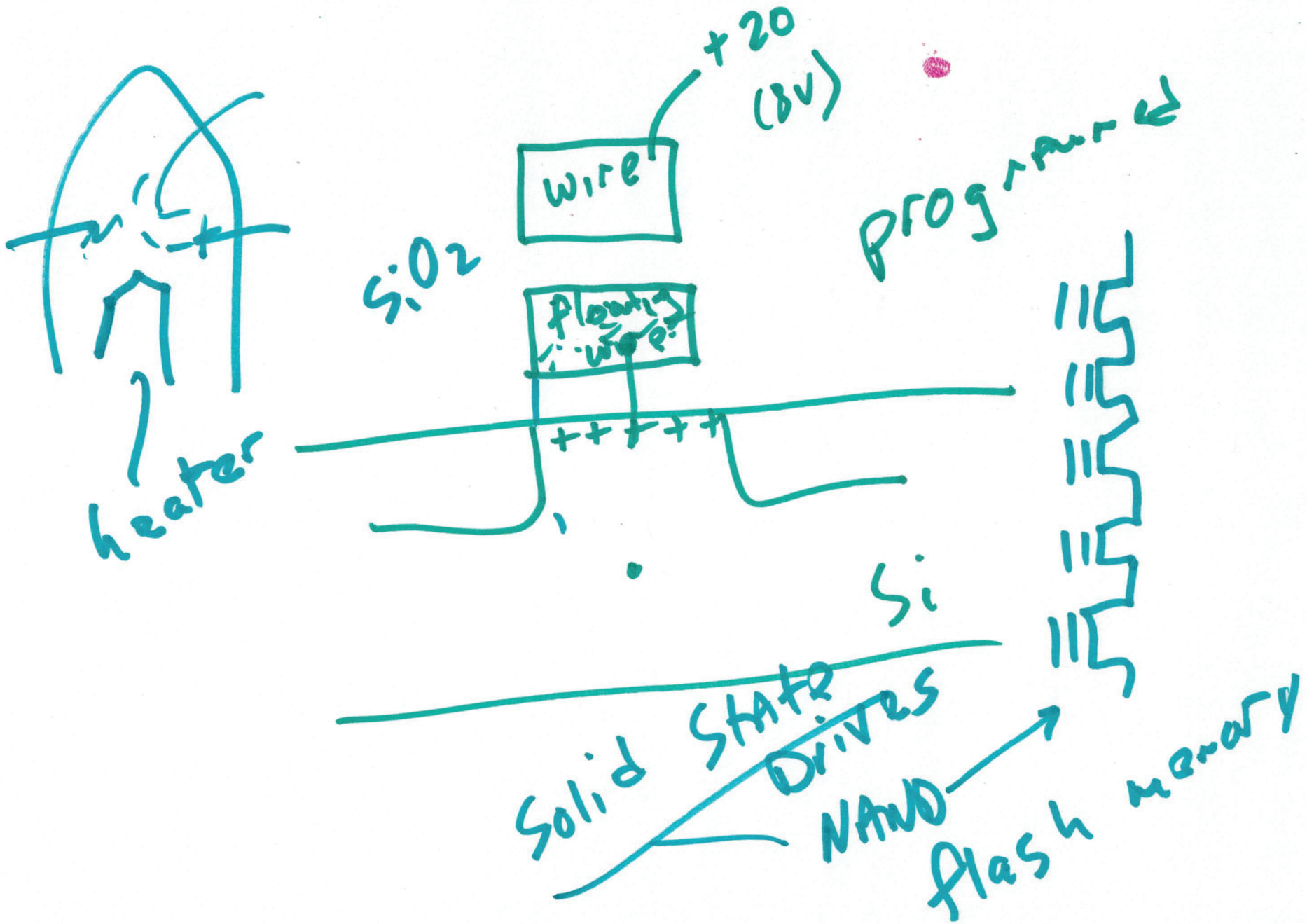
DIMMS



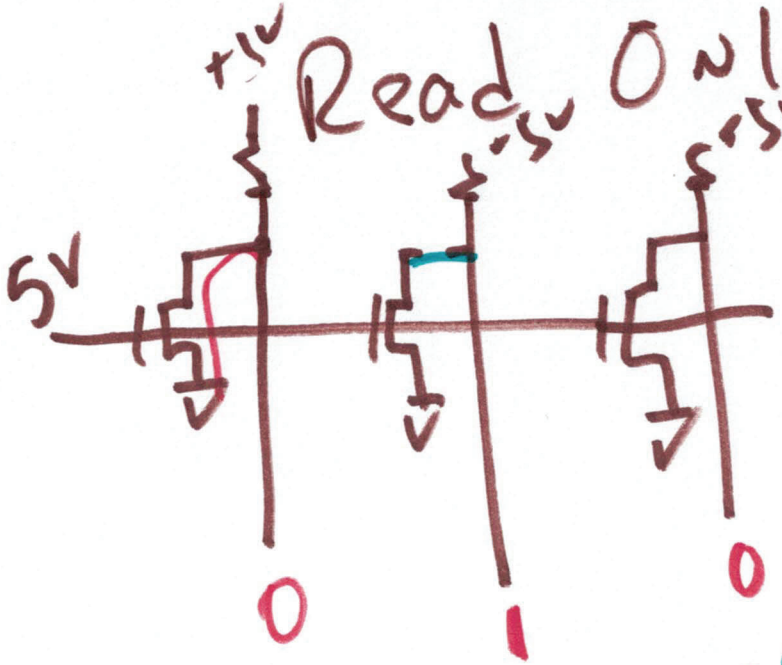
1T1C DRAm memory cell

Flash Memory




+20
(8V)
wire
SiO2
floating
wire
heater
Si
Solid State
Drives
NAND
flash memory

Read Only Memory

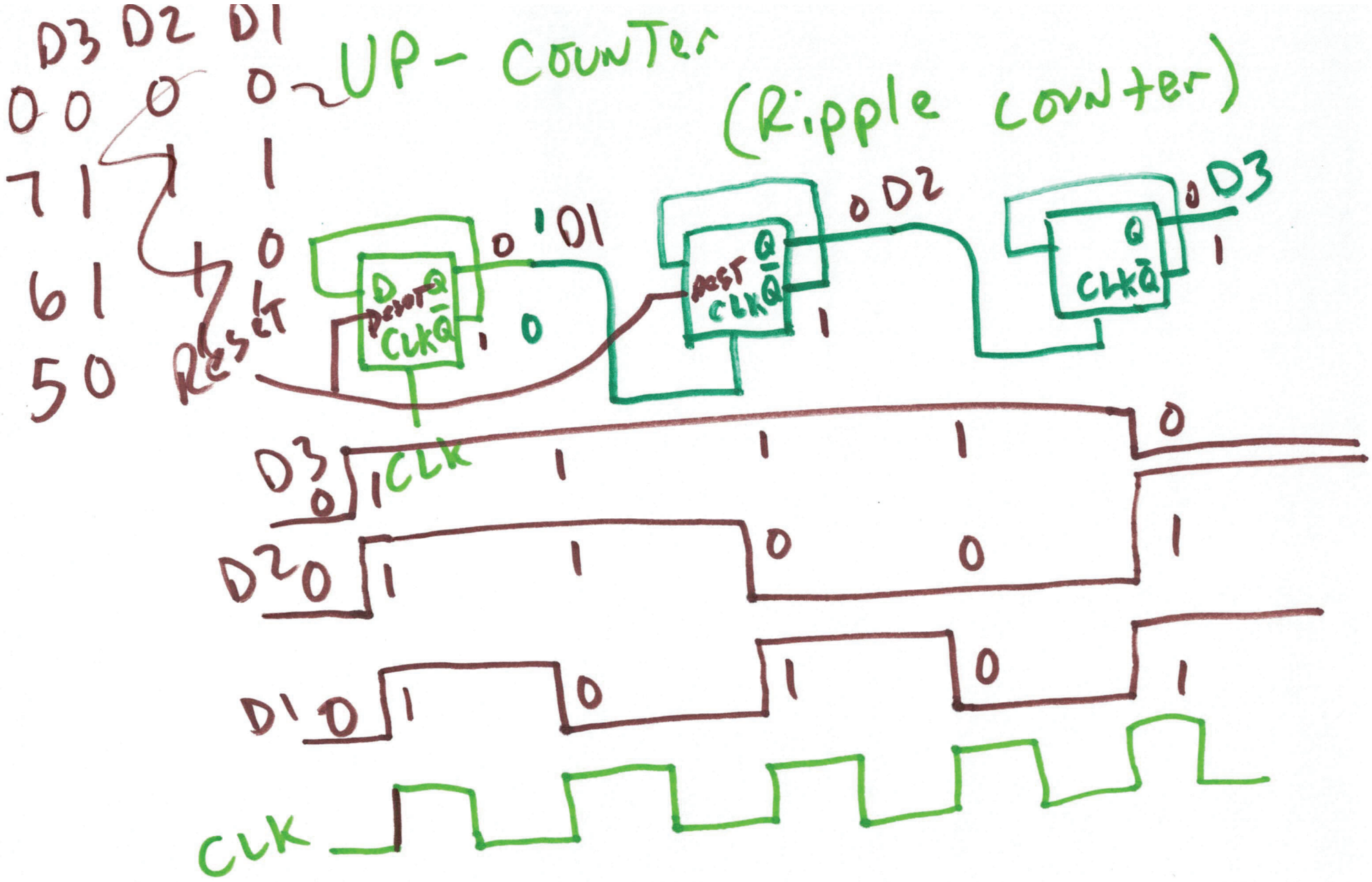


1^{24} * $14 - 10^{-6}$ m

Chalcogenide type of glass

Amorphous ← Random organization of atoms

Crystalline → organized arrangement


D3 D2 D1
0 0 0
7 1 1
6 1 0
5 0 Reset
UP - COUNTER
(Ripple counter)
D
Preset
Q
CLK
Q
D1
D2
D3
CLK
D3
D2
D1
CLK

	D_3	D_2	D_1
8	0	0	0
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1

Down counter

UP counter use $\bar{Q}$

1101 → 13

× 1001 9

1101

0000

0000

1101

---

64 32 16 4 1

1 1 0 1 0 1 → 117

1

13

× 9

117

9

$23 \rightarrow 23. \times 10^{0}$

23 billion $\rightarrow 23. \times 10^{9}$

mantissa

23416753221 . . .