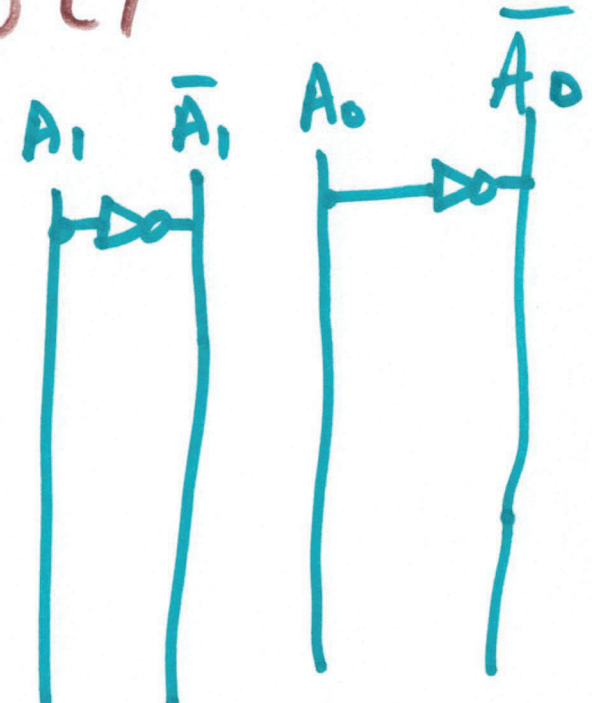
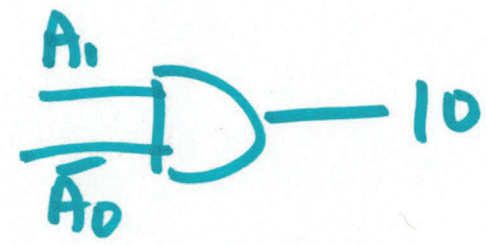
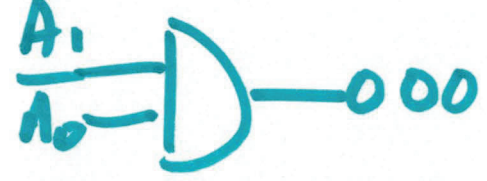
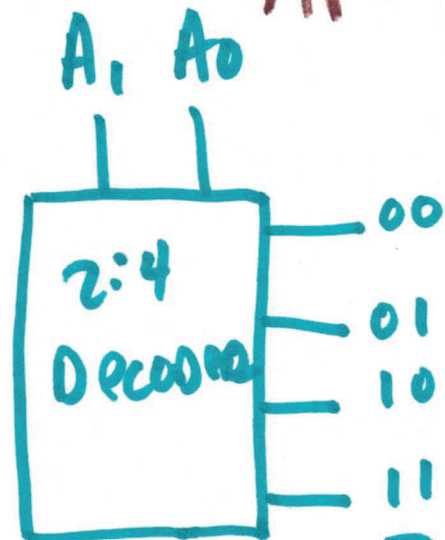
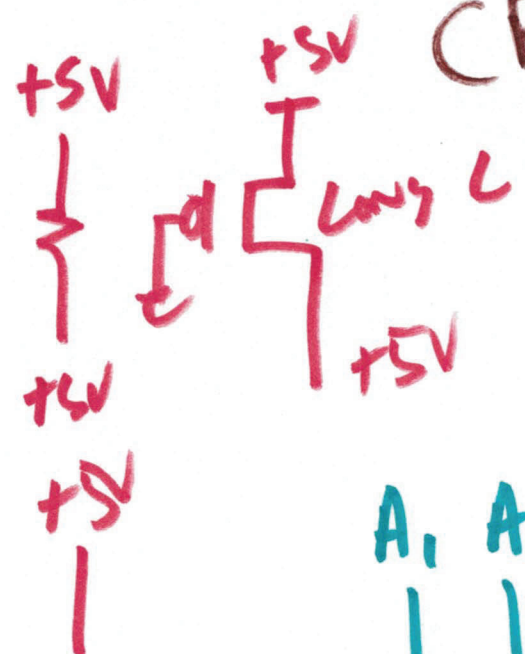
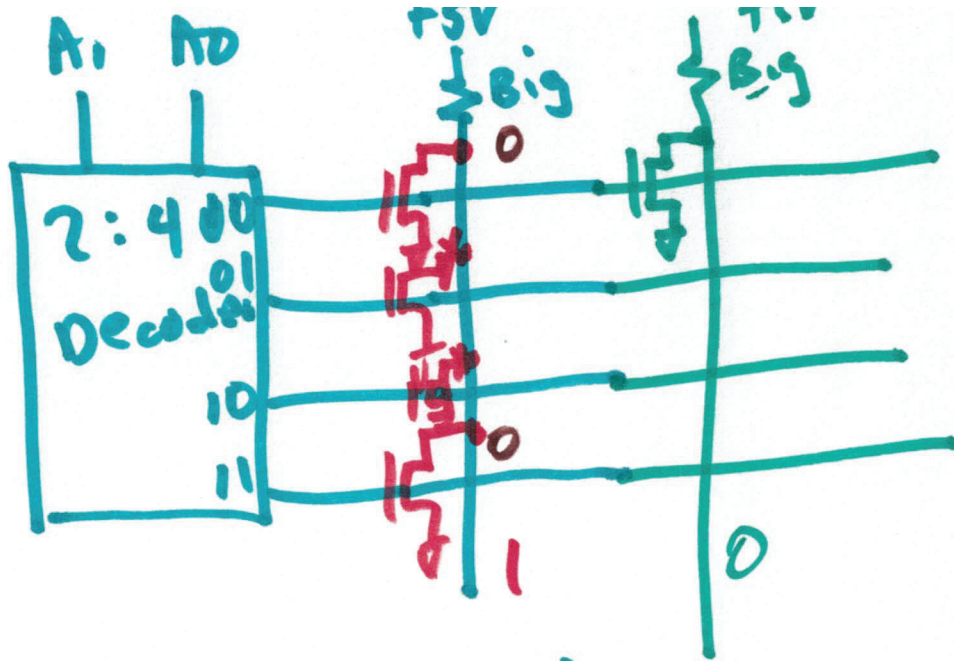


UNLV CPE 100 Digital Logic Design
 Lecture 25
 April 28, 2021





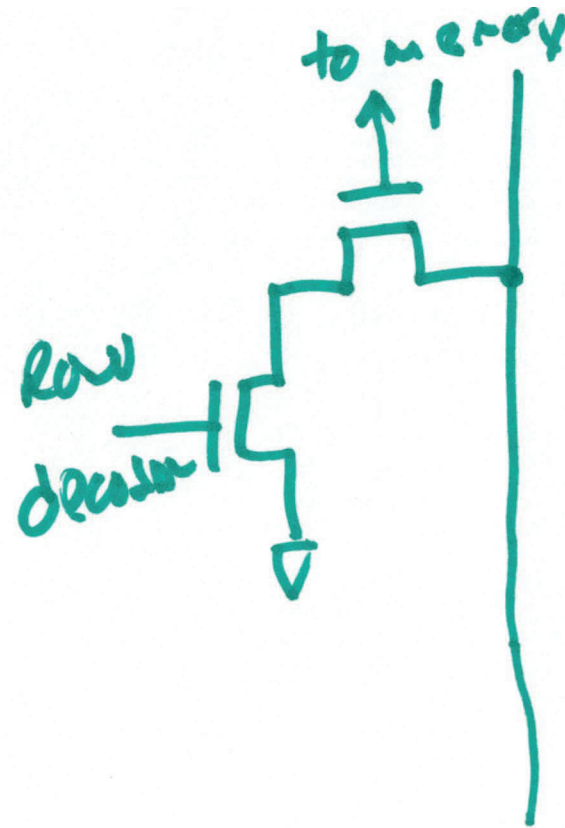
XOR logic

A ₁	A ₀	XOR
0	0	0
0	1	1
1	0	1
1	1	0

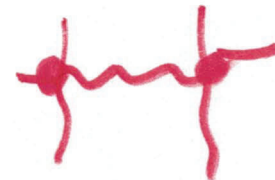
OR gate

A ₁	A ₀	OR
0	0	0
0	1	1
1	0	1
1	1	1

2)



Anti fuse



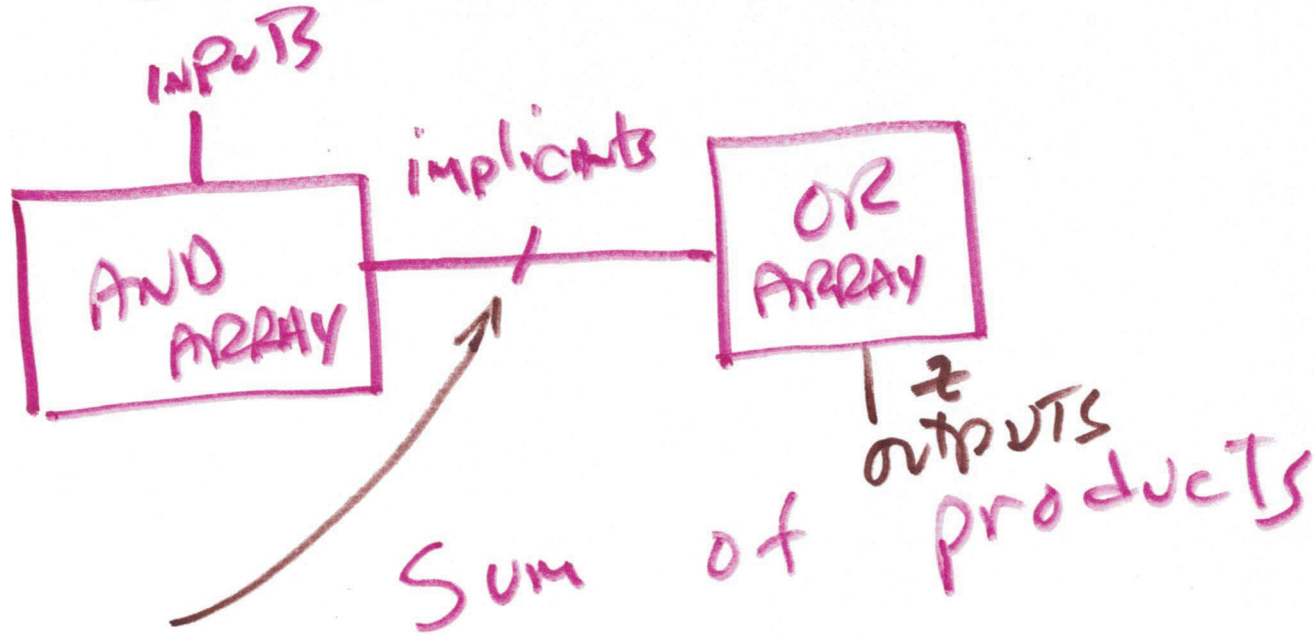
$$A\bar{B}$$

$$= \bar{Y}$$

$$Y = \bar{A} + B$$

3)

Programmable Logic ARRAY (PLA)



$$X = \bar{A}\bar{B}C + A\bar{B}\bar{C}$$

$$\left. \begin{array}{l} A\bar{B}C\bar{D} \\ A\bar{C} \\ \bar{A}D \end{array} \right) \text{implicants}$$

$$z = A\bar{B}C\bar{D} + A\bar{C} + \bar{A}D$$

4)