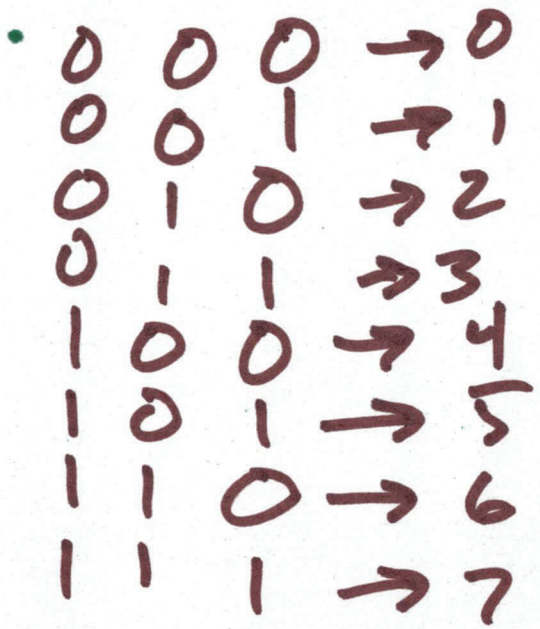
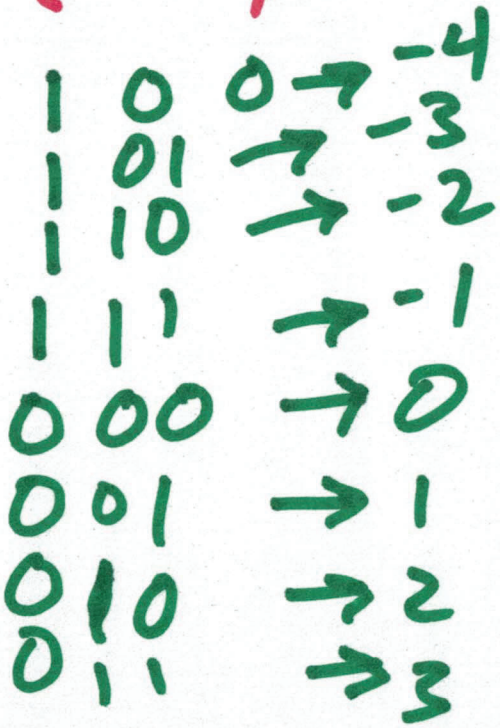
CpE 100 Logic Design

February 1, 2021

Lecture 4





two's comp

x x x x x x

16 8 4 2 1

52

x

64

001 → +1

-77

13

11,321

11321

100 1101 110

+ 1

111 → -1

0100 1101 → +77

1011 0010
+1

1011 0011 → -77

0001 0001 → 17

$$\begin{array}{r} (17) \\ +(-77) \\ \hline -60 \end{array}$$

$$\begin{array}{r} 1011\ 0011 \\ +\ 0001\ 0001 \\ \hline 1100\ 0100 \\ -\ 1 \\ \hline 1100\ 0011 \end{array} \leftarrow -60$$

$$\begin{array}{r} 0010 \\ \hline 1100\ 0100 \\ 1111\ 1111 \\ \hline 1100\ 0011 \end{array} \rightarrow -60$$

~~0111 0011~~

32 16 8 4 → 60

0011 1100

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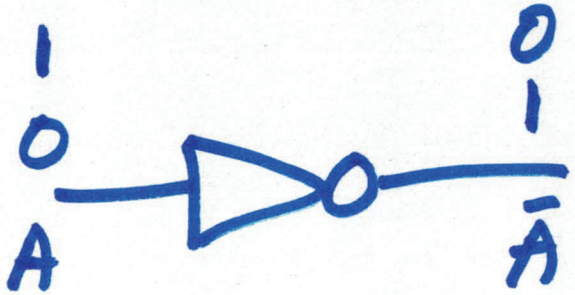
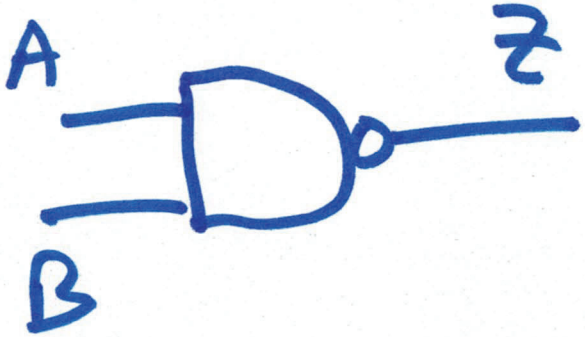
4)

Inverter

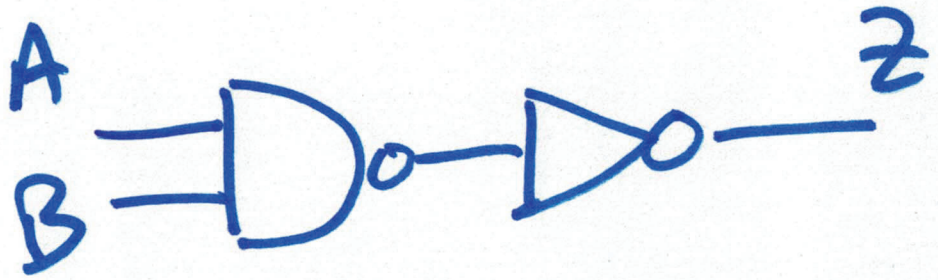


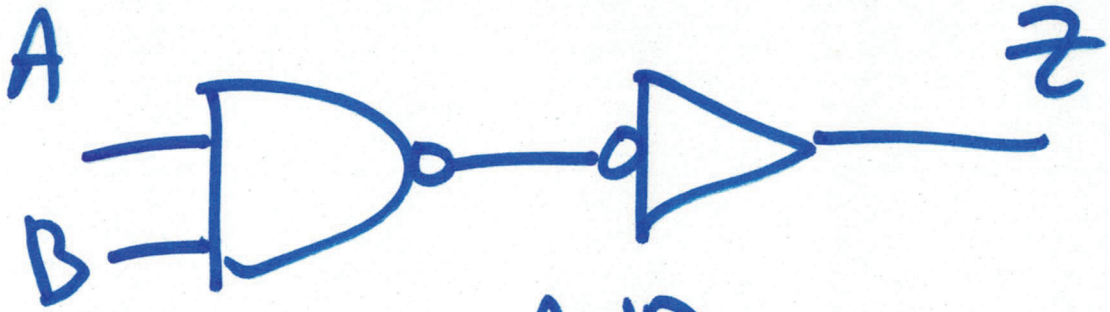
A	$\bar{A}$
0	1
1	0

NAND

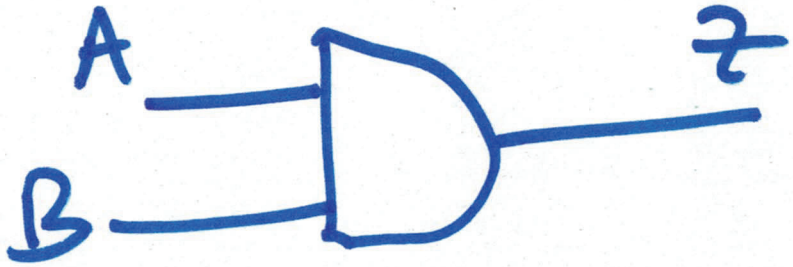


A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

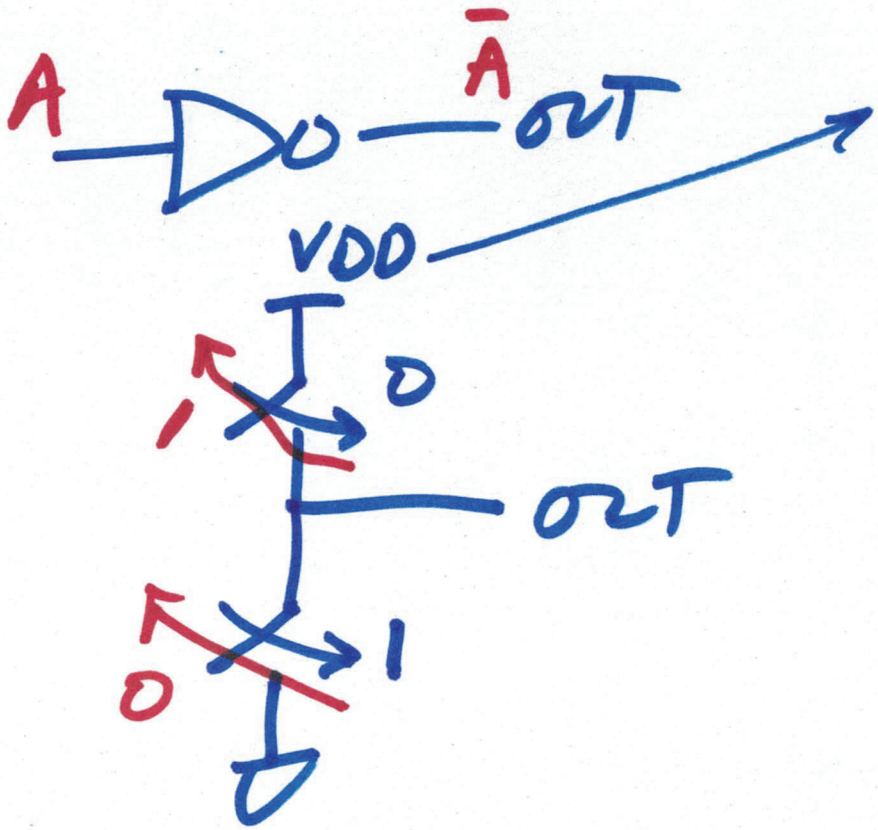


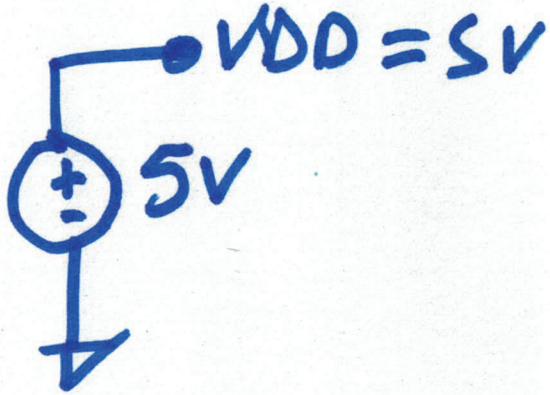


AND



A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1


A
$\bar{A}$
OUT
VDD
1
0
OUT
0
1


VDD = 5V
5V

-45 + 45

```
   0010 1101
   1101 0011
  ----------
  10000 0000
```

↙ Bit Bucket

64	32	16	8	4	2	1
0	1	0	1	1	0	1

```
   0010 1101 → +45
   1101 0010
           1
  ----------
   1101 0011 → -45
```

-128 67

0 0000 0011

256

128 64 32 16 8 4 2 1

0 1 0 0 0 0000 → +128

1 1 1 1 1 1 1 1

1 0 1 1 1

1

---

1 100 0000 → -128

0 0100 0011 → 67

---

1 1100 0011 → -61

9)