Tutorial presentation on Design of Σ-Δ sensing circuits for multi-level resistive memory.

ECE 614 Advanced Analog IC Design
Spring 2008
Presented by Hemanth Ande
Talk outline

- Delta Sigma Modulation Sensing
- DSM in Flash memory
- Resistive Memory (Types and concerns)
- Modeling Resistive memory in LT Spice
- Design development of Sensing circuit.
- Simulation Results of the DSM in Resistive Memory
- Multi Bit Sensing
- Conclusion
Comparison of Traditional & Delta Sigma Sensing Analogy with water level.

Traditional Sensing

(delta) No noise

(b) With noise

Delta Sigma Sensing

Float

Water level to be sensed

Valve

Delta

Remove a cup of water if the water level is above the line.

Figure from CMOSED.com
Example to illustrate DSM

- Let Speed of water flowing in to the sigma bucket 1/4cup every 10sec
- Ref level of sigma bucket be 5 cups.
- Sensing at every 10sec.
- Can be found out from the table as we increase the sense time we reduce the error and the average gets close to the actual value = .25cups/10sec
DSM Sensing in Flash Memory

- Rate of charge removed from bit line in one clock cycle is 
  \[ I_{bit} = C_{bit} \frac{\Delta V_{bit}}{T} \]

- Amount of charge removed from bit line (which is supplied from \( I_{cup} \)) 
  \[ Q_{bit} = I_{bit} \cdot T = \Delta V_{bit} \cdot C_{bit} \]

- The rate we add charge to bitline 
  \[ Q_{bit} = I_{bit} \cdot T = Q_{cup} = I_{cup} \frac{M}{N} \cdot T \]

\[ \frac{I_{bit}}{I_{cup}} = \frac{M}{N} \]
Resistive Memory

Programmable Resistance RAM (PRRAM)

Erased cell
Think of as 1 MEG

Programmed cell
Think of as 10k

Figure from CMOSEDU.com
Resistive Memory

- Access Transistor
- Word line
- Bit line
- Bit line Cap
- $I_{\text{mbit}}$
- $R_{\text{mbit}}$
- $V_{\text{DD/2}}$

- $R_{\text{Prog Ideal}} = 0 \Omega$
- $R_{\text{erase Ideal}} = \infty \Omega$

- $I_{\text{mbit}}$
- Voltage across $R_{\text{mbit}}$

- $R_{\text{Prog low resistance}}$
- $R_{\text{Prog High resistance}}$

- Voltage across $R_{\text{mbit}}$

- Different Resistance

- Single bit Practical case
- Multi bit Practical case

April 23, 2008
Problem with Phase change memory

Problems
- Not Ideal as shown
- Sensing is challenging
- Programming the Multi bit becomes more challenging


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Modeling Resistive memory

```
Vprog

PULSE(-.5 .5 0 1u 1u 0 2u)

.tran 0 2u 0 1n

.model CSW SW(Ron=10k Roff=1Meg Vt=0 Vh=.2)
```
Modeling Multi bit Resistive memory

```
.model CSW SW(Ron=100k Roff=10Meg Vt=0 Vh=.1)
.model CSW1 SW(Ron=100k Roff=15Meg Vt=0 Vh=.2)
.model CSW2 SW(Ron=100k Roff=20Meg Vt=0 Vh=.3)
.tran 0 2u 0 1n
```

April 23, 2008
Programming single bit Phase Change Memory

![Graph showing the temperature-time relationship for amorphization and crystallization pulses in Phase Change Memory](image)

- **Amorphizing (RESET) Pulse**
- **Crystallizing (SET) Pulse**

Figure from Ovonyx, Inc.
Concept of Sensing Resistive Memory

- Problems
  - Offset
  - Finite gain Error
  - Noise
  - Timing control & sensing
Programming

Problems
- Voltage Varies
- Process Variation
- Temperature Variation
- Noise on Word line
- Mosfet resistance comparable with $R_{\text{mbit}}$
- Cannot Write in to Multi bit resistive memory
DSM Sensing topologies

- Forcing the Current
- Holding Voltage at $V_{\text{ref}} + V_{\text{os}}$
DSM Sensing topologies

- Forcing the Current
- Holding Voltage at $V_{\text{ref}} + V_{\text{os}}$
Creating an offset

- Creating offset by mismatching one side of the comparator
- Very crucial to design this offset with so many variations affecting the operation (temp, process, vdd)
- Design tip: need to use some killer offset to ensure for all process run we have +offset in the direction we think.
Writing

Problems
• 2 transistors Layout concern
• Noise on wordline
• Problem with controlling

Basic Idea
• forcing current, and holding bit line voltage at Vref
Design topology

Does not change current (even bit line changes)
Cannot clock this circuit at high frequencies
• Chance of changing data
• Fundamental problem is due to the parasitic capacitance
• Doesn't start instantly PMOS has to go to saturation (takes time)
• False sensing giving rise to error
Design topology

\[ Q_{\text{cup}} = C_{\text{cup}} VDD \]

\[ Q_{\text{cup}} = C_{\text{cup}} (VDD - V_{\text{bit}}) \]
Design topology

\[ Q_{\text{cup}} = C_{\text{cup}}(VDD-V_{\text{ref}}-V_{\text{Thp}}) \]

\[ I_{M\text{bit}} = \frac{V_{os}}{R_{M\text{bit}}} = Q_{\text{cup}} \frac{M}{N \cdot T} \]

\[ = (VDD-VDD/2-V_{\text{THP}}) \cdot C_{\text{cup}} \frac{M}{N \cdot T} \]

\[ R_{M\text{bit}} = \frac{V_{os} \cdot T}{(VDD-VDD/2-V_{\text{THP}}) \cdot C_{\text{cup}} \frac{M}{N}} \]

\[ VDD=1v \]
\[ V_{os}=50mv \]
\[ V_{\text{THP}}=280mv \]
\[ C_{\text{cup}}=100fF \]

\[ R_{M\text{bit}} \approx 25K \cdot \frac{N}{M} \]
Simulations

\[
R_{Mbit} = 25k \cdot \frac{50}{36} = 35k \text{(actual Value 25K)} \\
R_{Mbit} = 25k \cdot \frac{50}{17} = 73k \text{(actual Value 50K)} \\
R_{Mbit} = 25k \cdot \frac{50}{10} = 125k \text{(actual Value 100K)} \\
R_{Mbit} = 25k \cdot \frac{50}{6} = 208k \text{(actual Value 200K)}
\]
Design topology

- Simple Design
- Can use 4 of the same NMOS in parallel to get the same process resistance
- Cannot be modified
- No control on the resistance
- Multi bit sensing becomes tough.
Final Design with Integrated sensing and Programming

Bit line

Word line

$I_{mbit} = \frac{V_{DD}}{2}$

$V_{DD} = V_{DD/2}$

$V_{Erase} = 0 - V_{DD}$

$V_{Write} = \frac{V_{write} = .7V}{V_{DD/2} = .5V}$
Simulation Result
Multi Bit Sensing and Programming.

Diagram: A circuit diagram illustrating multi-bit sensing and programming. The diagram includes symbols and voltages such as VDD/2, VDD, +Vthp, and VRef. The circuit is designed to handle different programming voltages for multi-level cells.
Conclusion

- Brief discussion about Resistive Memory Sensing and Programming
- Modeling Resistive memory in LT Spice
- Problems with various topologies
- Design & development of multi bit DSM sensing scheme for Resistive memory
References


Questions ?
An overview of extracting parasitics in an integrated circuit from a CAD tool perspective

By,
Mahesh Balasubramanian
Outline

- Need for Layout Parasitic Extraction (LPE).
- Parasitics to be addressed
  - Proper representation of parasitics.
  - Parasitic resistance and capacitance in interconnects.
    - ‘Lumped C’ where the coupling capacitances are grounded.
    - ‘Lumped Coupled C’ where only capacitances (coupling and to-ground) are extracted.
    - ‘Distributed RC’ where wire resistances and capacitance are extracted but coupling capacitance are grounded.
    - ‘Distributed Coupled RC’ where wire resistance and capacitance are extracted and the coupling capacitances are not grounded.
  - Device parasitics
    - Gate to Source and Gate to Drain parasitic capacitance.
    - Source/Drain to Substrate parasitic capacitance.
    - Well and Substrate resistance
    - Parasitic Diodes.
    - Junction capacitances.
Outline Continued ..

- Limitation and Consideration
- Testing and Verification
- Conclusion and Future prospects
Introduction

- Rapid advancement in the semiconductor industry.
- Scaling.
- Sensitivity to parasitics.
- High frequency circuits.
- Result: Designs that do not meet performance constraint.
Parasitics representation

- Proper representation of parasitics
  - Netlist format a huge criteria for designers
  - Proper data representation:

```
*** Via5: area_cap=0.00FF/um^2, edge_cap=0.6
*** Metal-6: area_cap=0.0433FF/um^2, edge_cap
.OPTIONS NMODE NPAGE

*** TOP LEVEL CELL: SimpleNet(lay)
  XPO p1 p2 p3 R 4.6 C=0.10FF len=39.5
  .SUBCKT RCLINE n1 n2
  01 n1 0 n2 0 RTRC
  .MODEL TRC tala R={6} C={6} len={6}
  .END

*** Metal-6: area_cap=0.0433FF/um^2, edge_cap
.OPTIONS NMODE NPAGE

*** CELL: subcell(lay)
  .SUBCKT subcell
  ** Extracted Parasitic Capacitors
  C0 net00 0 5.04FF
  ** Extracted Parasitic Resistors
  .END subcell

*** TOP LEVEL CELL: ParentCell(lay)
  Xsubcell1@ subcell
  ** Extracted Parasitic Capacitors
  C0 net00 0 5.04FF
  ** Extracted Parasitic Resistors
  .END
```
Parasitic resistance and capacitance in interconnects

- **Lumped C**
  - \( C_{\text{poly1-sub}} = 34 \text{fF} \)
  - \( C_{\text{poly2-sub}} = 36 \text{fF} \)
Parasitic resistance and capacitance in interconnects continued …

- Presence of resistance for ‘Lumped C’.
- Wrong estimation of capacitance of Poly2 to substrate.
Parasitic resistance and capacitance in interconnects continued …

- Approach for ‘Lumped C’ parasitic extraction.
  - Simple way would be to use geometrics and find area of overlap if any and exclude it.
  - The drawback would be a slight over estimation or an underestimation when using Manhattan geometry.
  - Decide if and when to exclude area of overlap based on certain parameters.
Parasitic resistance and capacitance in interconnects continued …

✓ Decide if and when to exclude area of overlap based on certain parameters.
✓ The parameters: time for extraction, impact on circuit, etc.
Parasitic resistance and capacitance in interconnects continued ...

- ‘Lumped Coupled C’ where only capacitances (coupling and to-ground) are extracted.
  - A 3D model is being considered for implementation with several applicable algorithms.
  - The first issue would be to add interlayer parasitic capacitance in the tool.
  - Available options:
    - Simple overlap Capacitance
      (Low accuracy, faster)
    - Pattern matching
      (High accuracy, slower)
Parasitic resistance and capacitance in interconnects continued …

- A simple overlap capacitance as shown in the figure on left would result in a slight over estimation due to the fringe capacitance of M2-M1.
- The area of overlap can be estimated using the co-ordinates of M1 and M2.
- \( \text{Cap}_{M1-M1} = \frac{\varepsilon}{d} (t \times L) \)
- The consideration here is the distance between adjacent metal lines.
- The effect of coupling capacitance on adjacent metal line increases to larger distance (d) as we move up to higher order metal layers.
Parasitic resistance and capacitance in interconnects continued …

- For complex coupled parasitic capacitance extraction, pattern matching can be used.
- For any given technology, tens of thousands of test structures are enumerated and a step called pre-characterization is performed.
- The data from the tests are used to build lookup tables.
- As the geometric pattern becomes complex, i.e. more the parameters needed to describe a pattern harder it is to match.
- The matching algorithm complexity defines the speed of extraction and accuracy.
Parasitic resistance and capacitance in interconnects continued …

➢ ‘Distributed RC’ where wire resistances and capacitance are extracted but coupling capacitance are grounded.
Parasitic resistance and capacitance in interconnects continued …

✅ The area of concern here is the over estimation of resistance due to the overlap of arcs at junctions/nodes. Area marked E.

✅ Can be addressed by merging the arcs to form one coherent metal wire before parasitic extraction.

✅ Again consideration and choices need to be made when two different layers overlap.
Parasitic resistance and capacitance in interconnects continued …

- ‘Distributed Coupled RC’ where wire resistance and capacitance are extracted and the coupling capacitances are not grounded.
  - The most complex of all interconnects parasitic extraction.
  - Network analysis algorithm required for complex networks.
  - High level of pattern matching is required for accuracy.
  - The way to tackle this situation is do a selective analysis of nodes which are of high importance and where ‘Distributed Coupled RC’ has higher prominence.
Testing and Verification

- Using a 31 stage ring oscillator for parasitic effect due to interconnects.

- Frequency: \( f = \frac{1}{n(t_{PHL} + t_{PLH})} = 80\text{MHz} \); \( t = 12.5nS \)
- R=7k
  (Over estimation)
- C=20pF
- Delay=0.05pS
Testing and Verification Continued ...

Oscillator simulation with added RC

Oscillator simulation from Layout with and without parasitic
Conclusion and Future prospects

- Considerable research and thought has been put to develop an approach for layout parasitic extraction (LPE). This could potentially be changed to better suit the requirement as and when development is done for a particular model.
- One of the first thing to consider in the future would be to include parasitic inductance.
- Increase the accuracy and speed.
- Considerable research needs to be done in extracting device level parasitics and parasitic devices.
- Develop LPE for other technologies.
References

circuits”, Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE