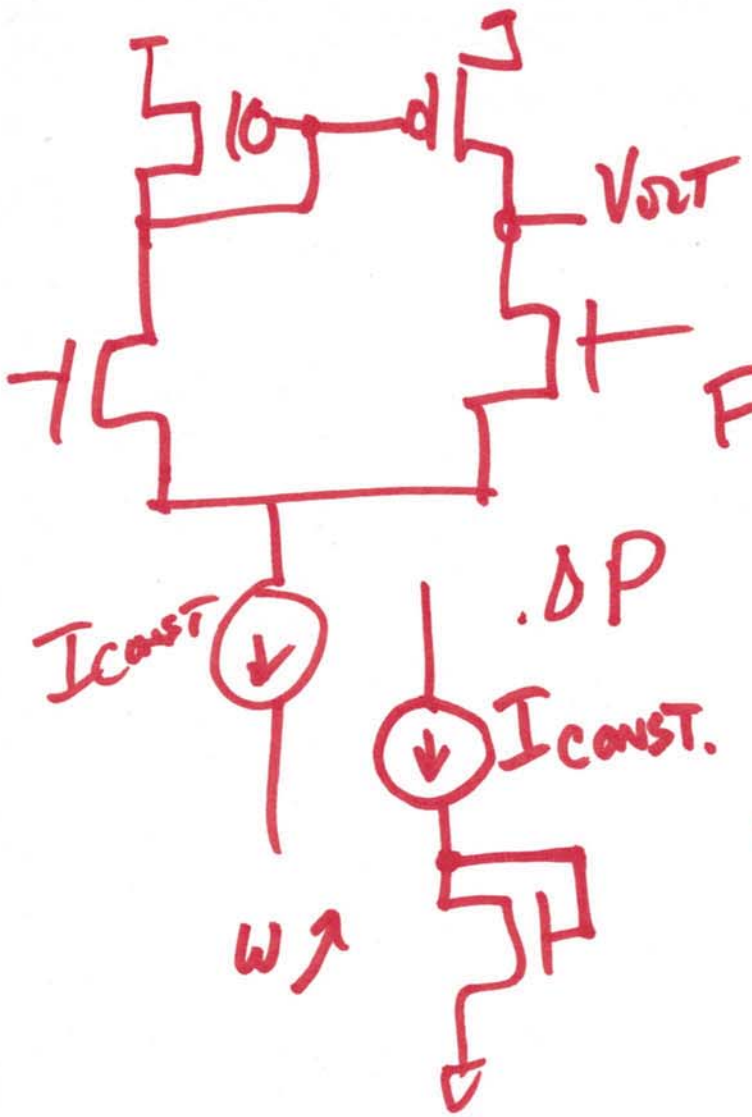
EE 720
Advanced Analog IC Design



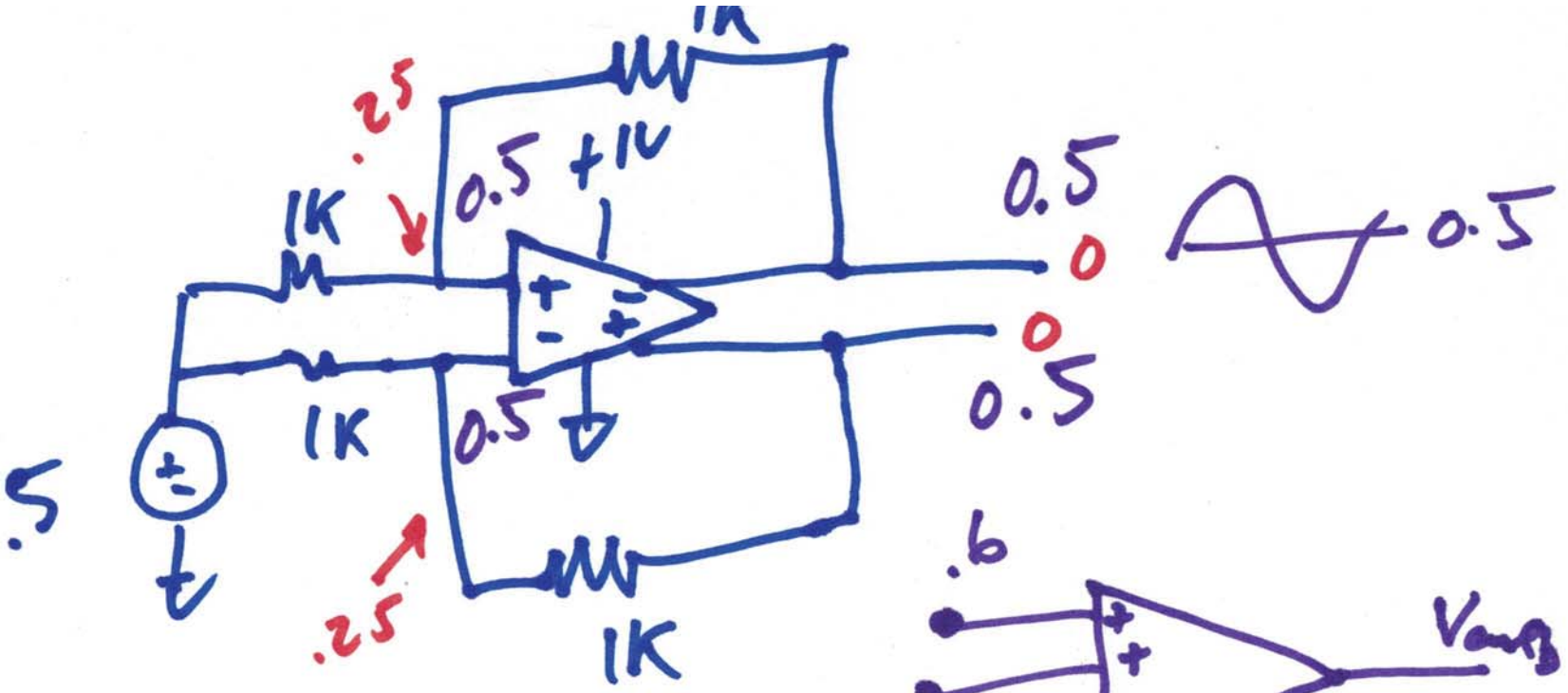
Feb. 19, 2016

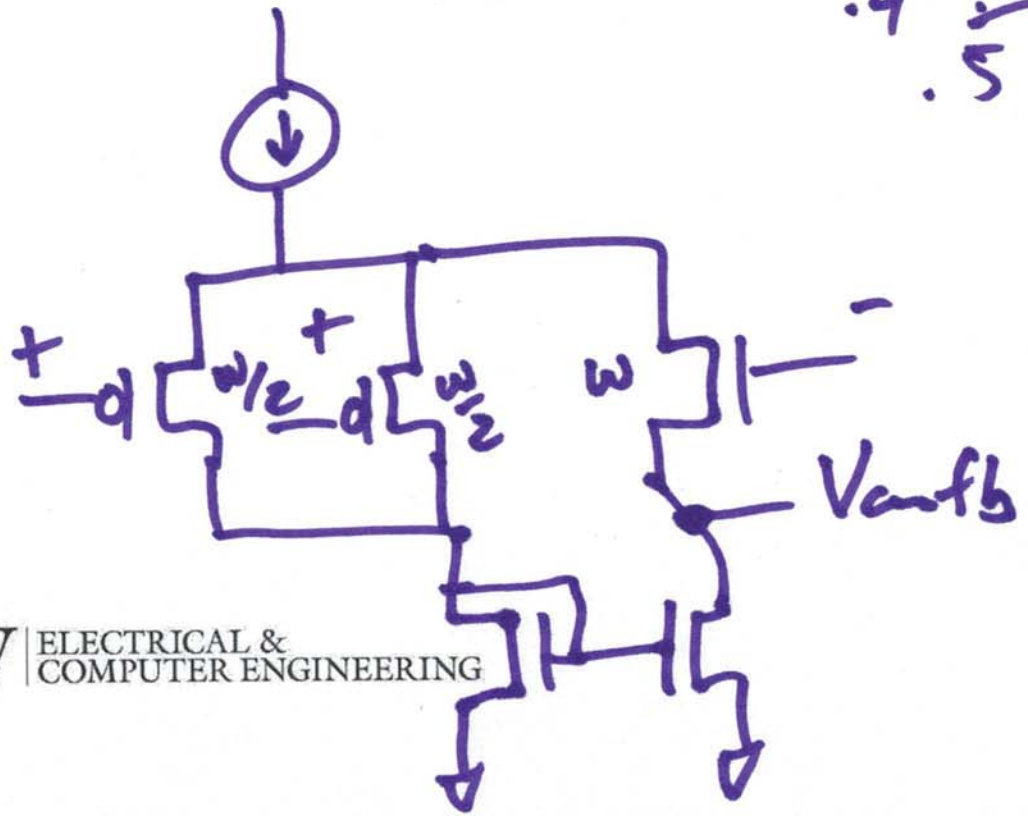
Lecture 10

$V_{GS}\downarrow \quad f_T\downarrow \quad g_m r_o = \text{CONST.}\nearrow$

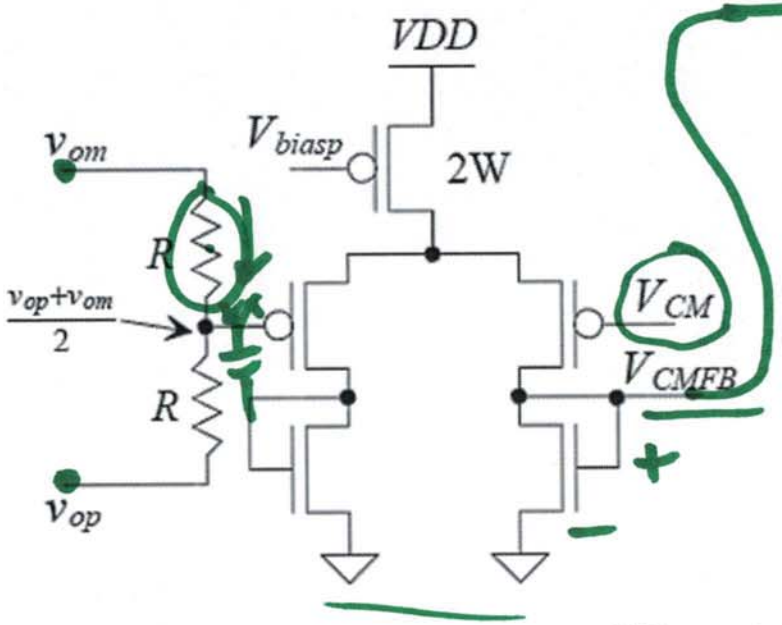
$g_m \nearrow = \sqrt{2 K_P \left(\frac{W}{L}\right) \cdot I_{D\,\text{CONST}}}$

$r_o \downarrow = \frac{1}{\lambda I_D}$

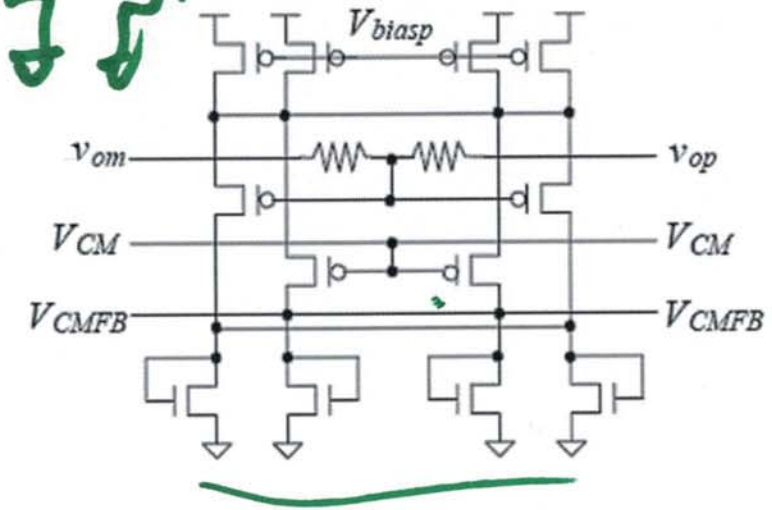




Has issues!



(a) Using resistors to average differential output signals.



(b) Symmetrical implementation of the CMFB circuit in (a).

Figure 26.14 Increasing CMFB amplifier input range.

$$\frac{V_{om}-V_{op}}{2R}$$

$$V_x = V_{om} - \frac{V_{om}-V_{op}}{2R}\cdot R$$

$$= \frac{2V_{om}}{2} + \frac{V_{op}-V_{om}}{2}$$

$$= \frac{V_{op}+V_{om}}{2}$$

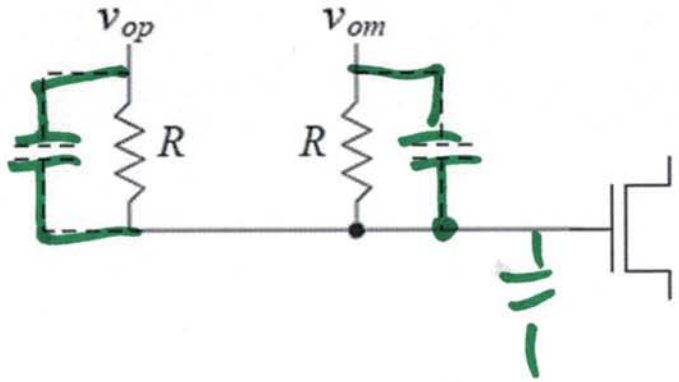


Figure 26.15 Adding parasitic capacitances across the resistors to compensate for the input capacitance of the MOSFET.

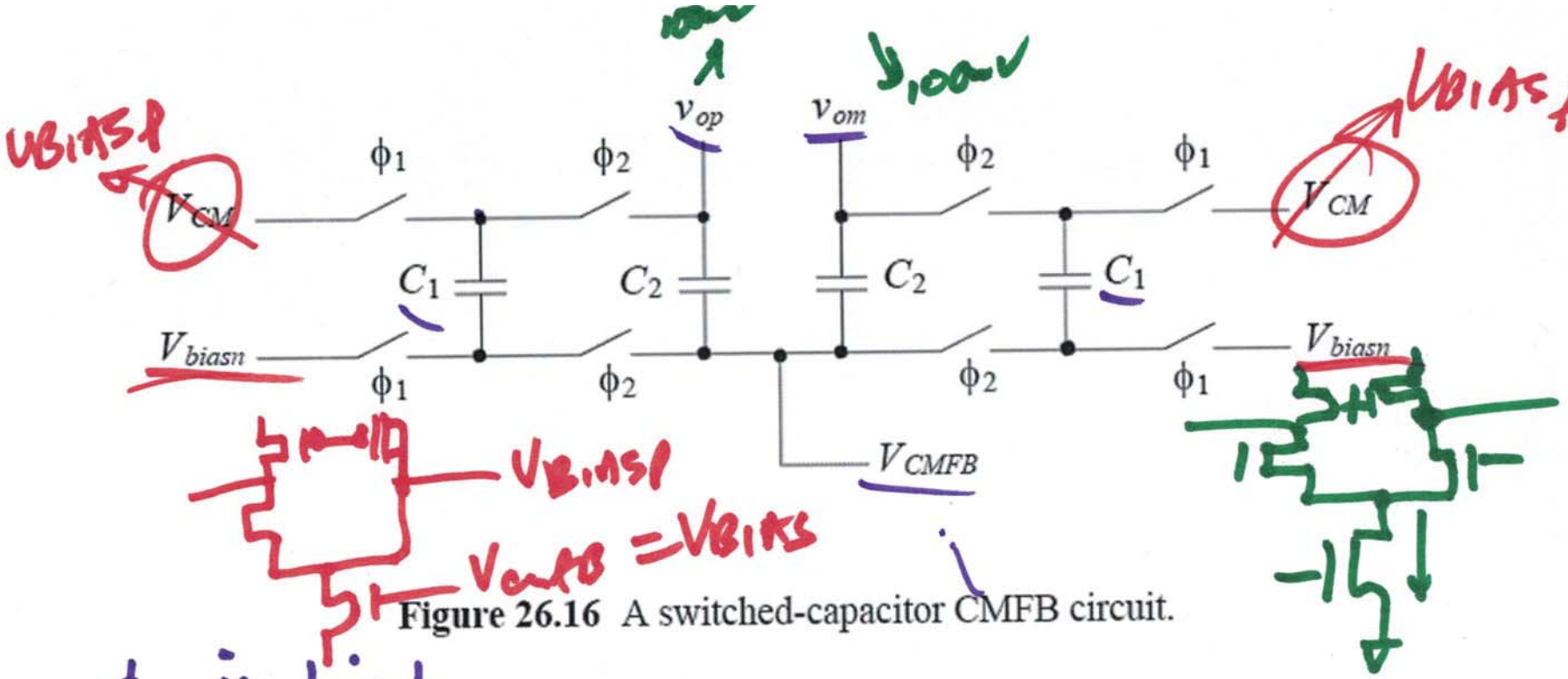


Figure 26.16 A switched-capacitor CMFB circuit.

ϕ_1 is high

$$q_1 = 2C_1(V_{biasN} - V_a)$$

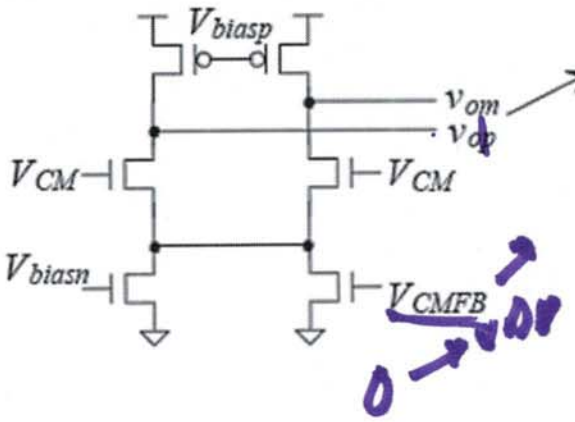
ϕ_2 is high

$$q_2 = C_1(V_{cmfb} - 2v_{op}) + C_1(V_{cmfb} - V_a)$$

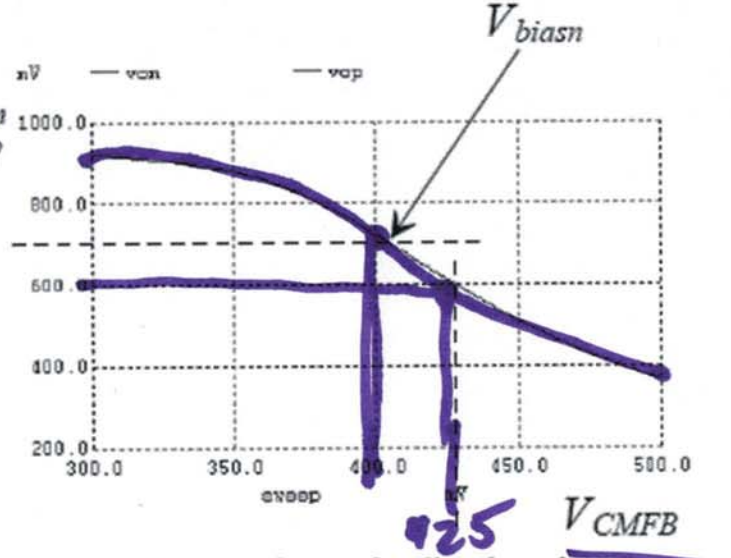
Figures from CMOS Circuit Design, Layout, and Simulation, Copyright Wiley-IEEE, CMOSedu.com

$$\Delta V_{cmfb} \cdot 2(C_1 + C_2) \propto (q_1 - q_2)$$

$$q_1 - q_2 = 2C_1\left(V_{bias} - V_{cmfb} + \frac{2v_{op} + 2v_{on}}{2} - V_{on}\right)$$



NMOS 10/1
PMOS 20/1
Bias circuit from Fig. 26.3



Value of CM feedback voltage when the outputs are 600 mV.

Figure 26.17 Plotting the output voltages as a function of the CM feedback voltage.

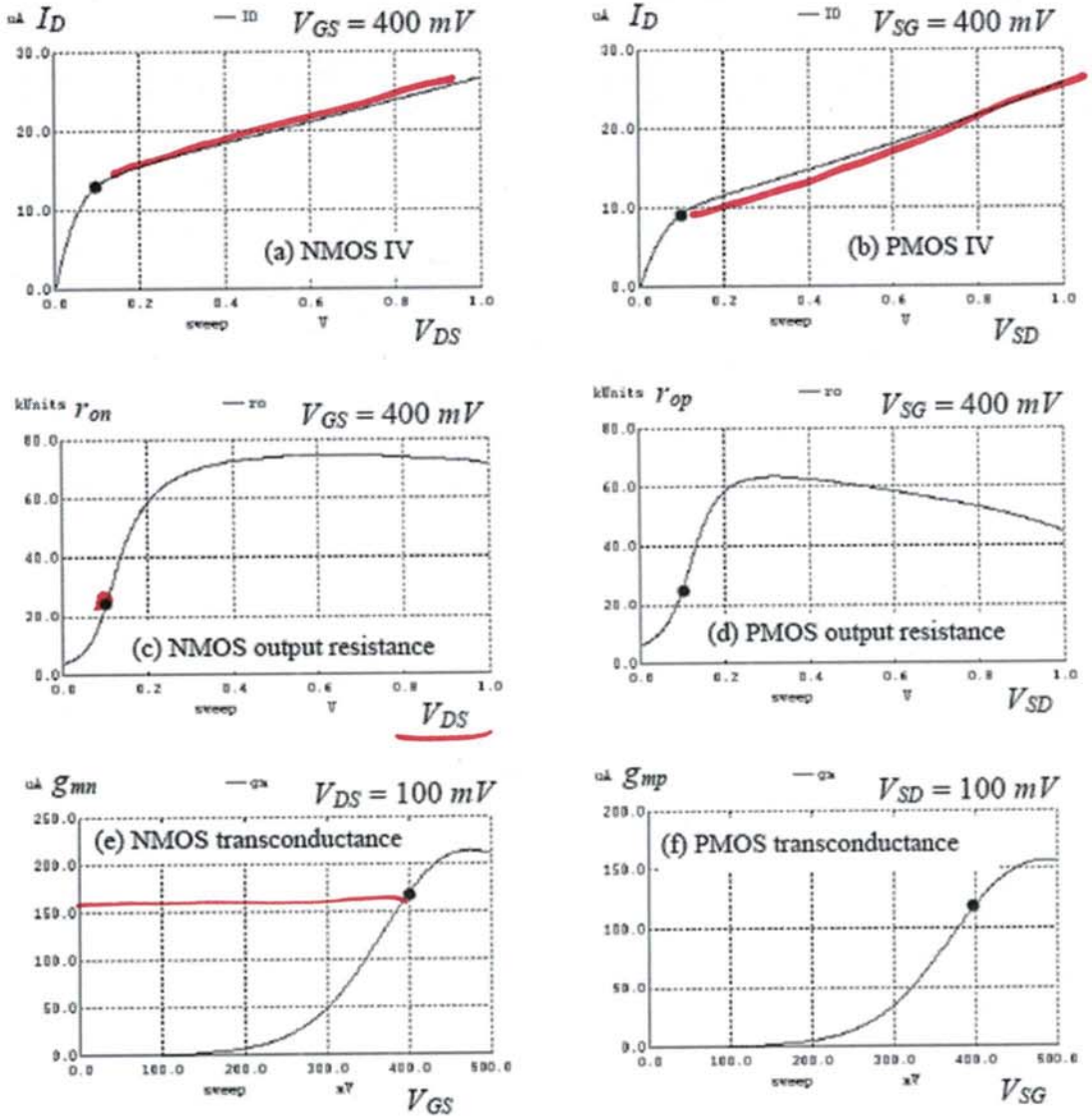


Figure 26.18 Characteristics of NMOS (10/1) and PMOS (20/1) devices.

$g_m r_o$

$30 \frac{V}{V} \cdot k\Omega = r_o$

$g_m = 150\mu A$

$0.03 \times 10^6 \times 150 \times 10^{-6}$

$= 4.5$

8)

NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.3

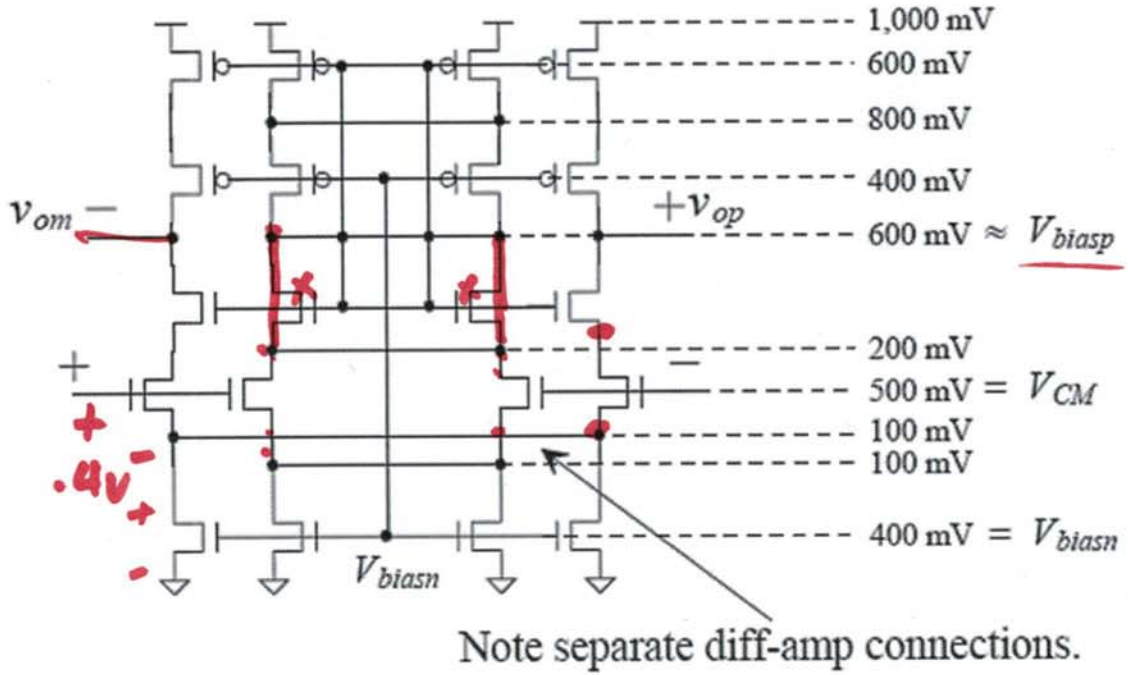


Figure 26.19 Fully-differential cascode diff-amp.

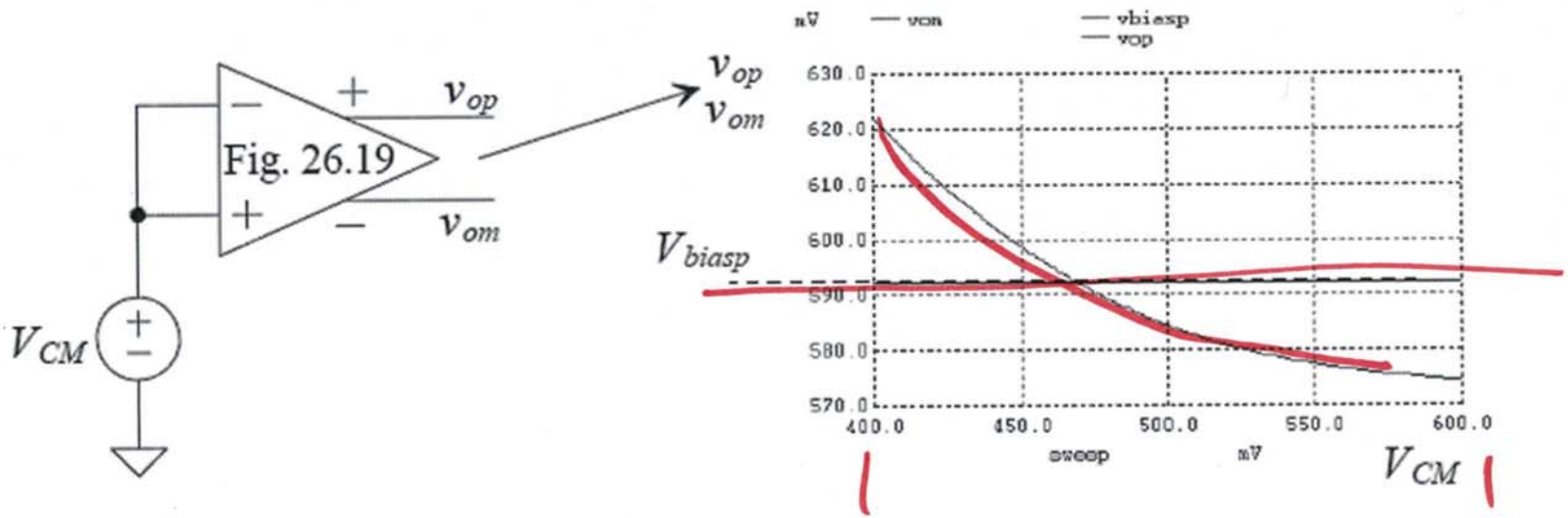


Figure 26.20 Varying the common-mode voltage and looking at the output.

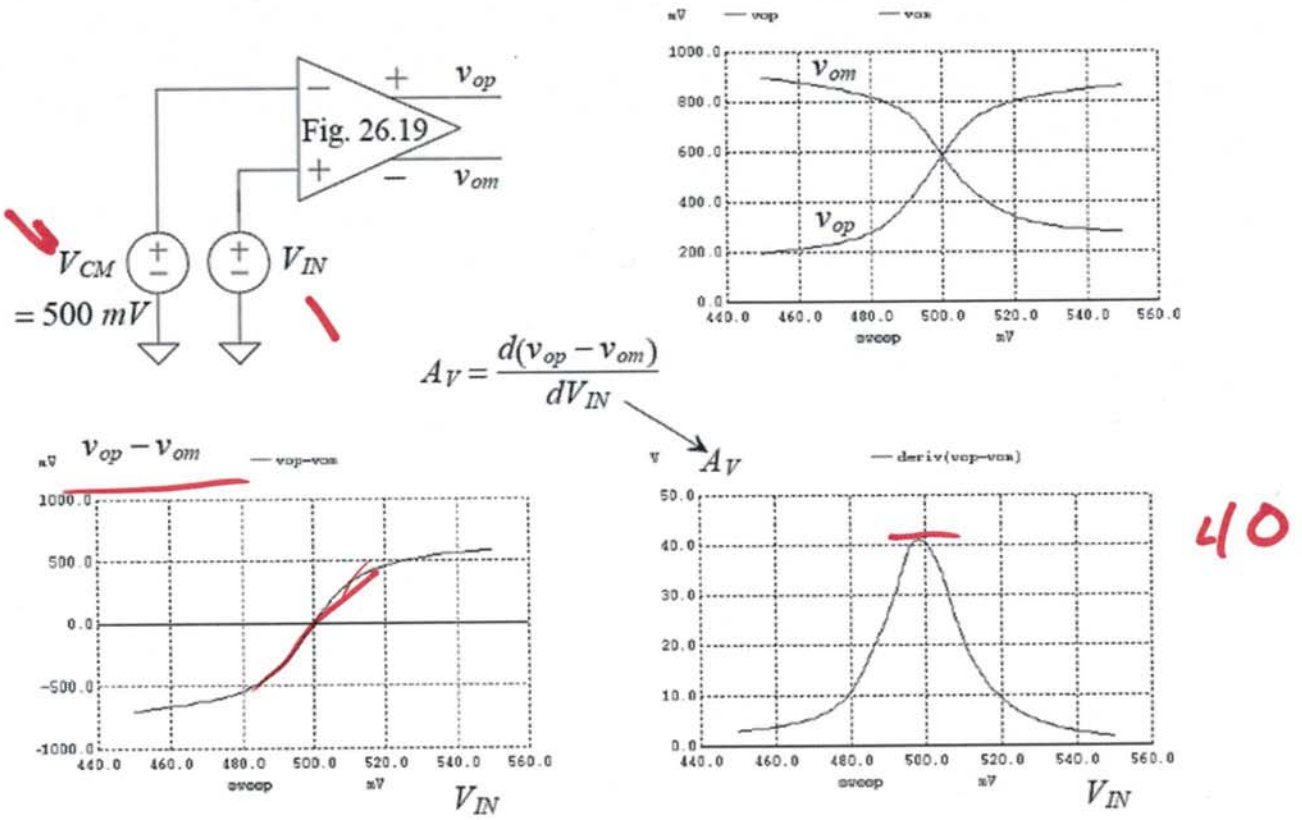
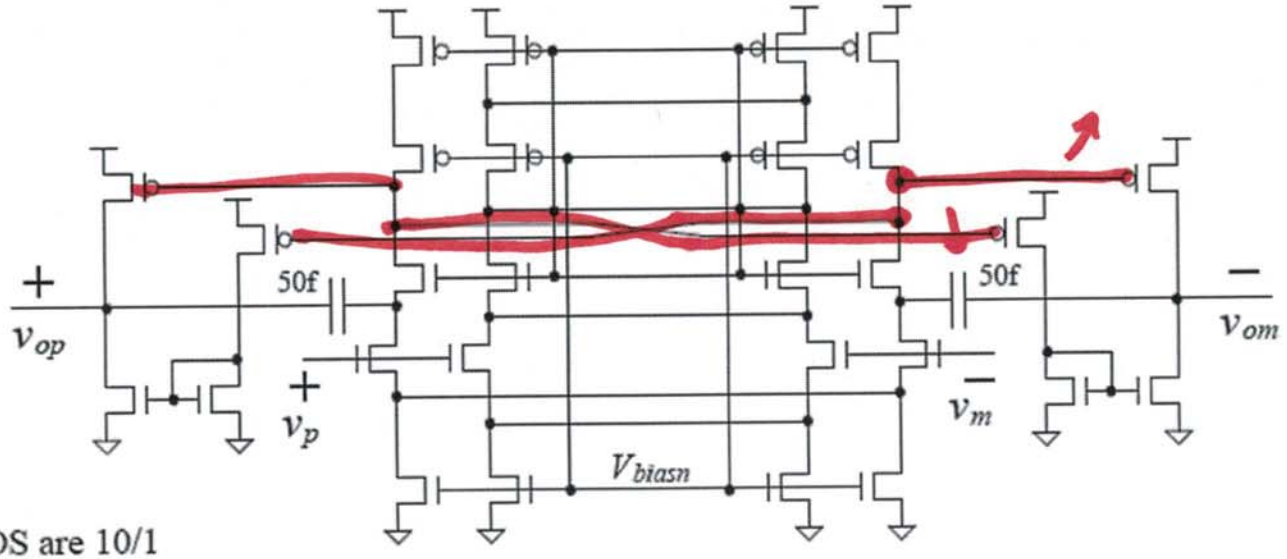


Figure 26.21 DC behavior and gain of the diff-amp in Fig. 26.19.



NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.3

Figure 26.22 Basic two-stage op-amp without CMFB.

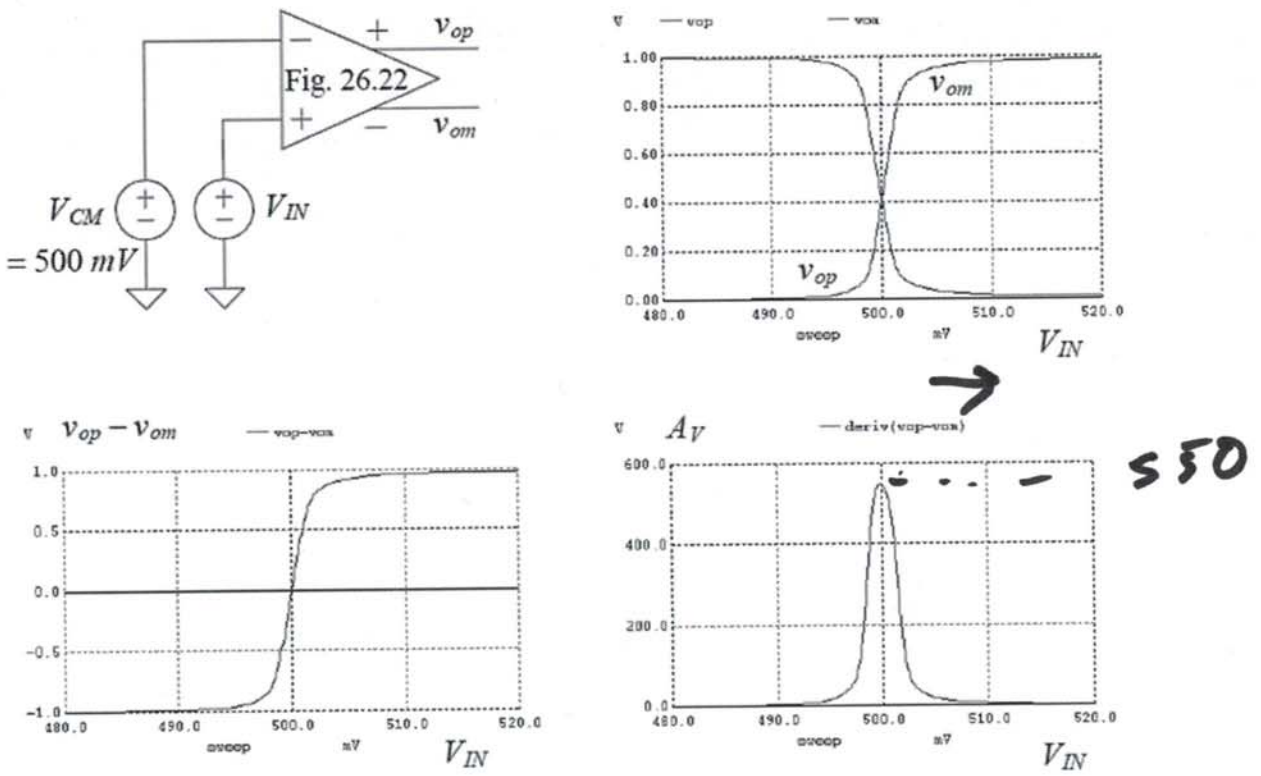


Figure 26.23 DC behavior and gain of the op-amp in Fig. 26.22.

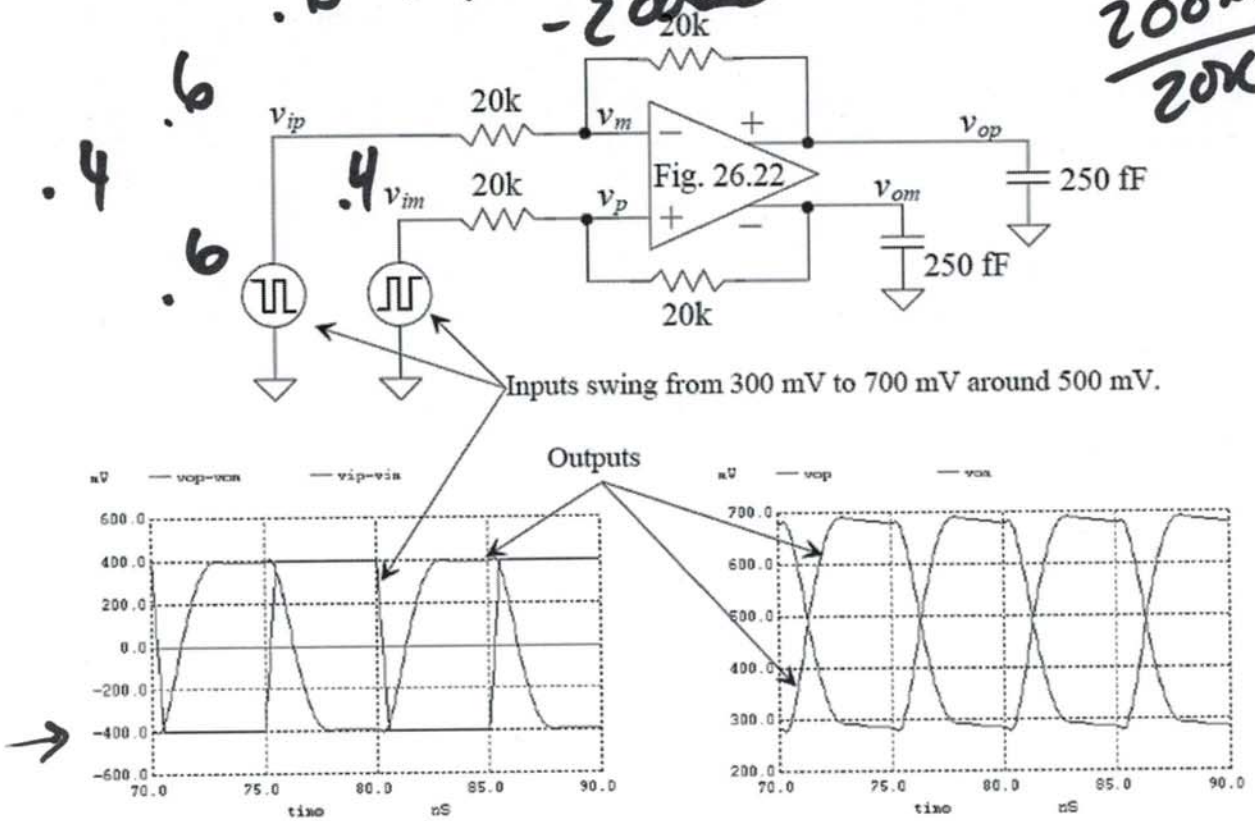


Figure 26.24 Step response of the op-amp in Fig. 26.22 driving 250 fF load capacitors and 20k feedback resistors.

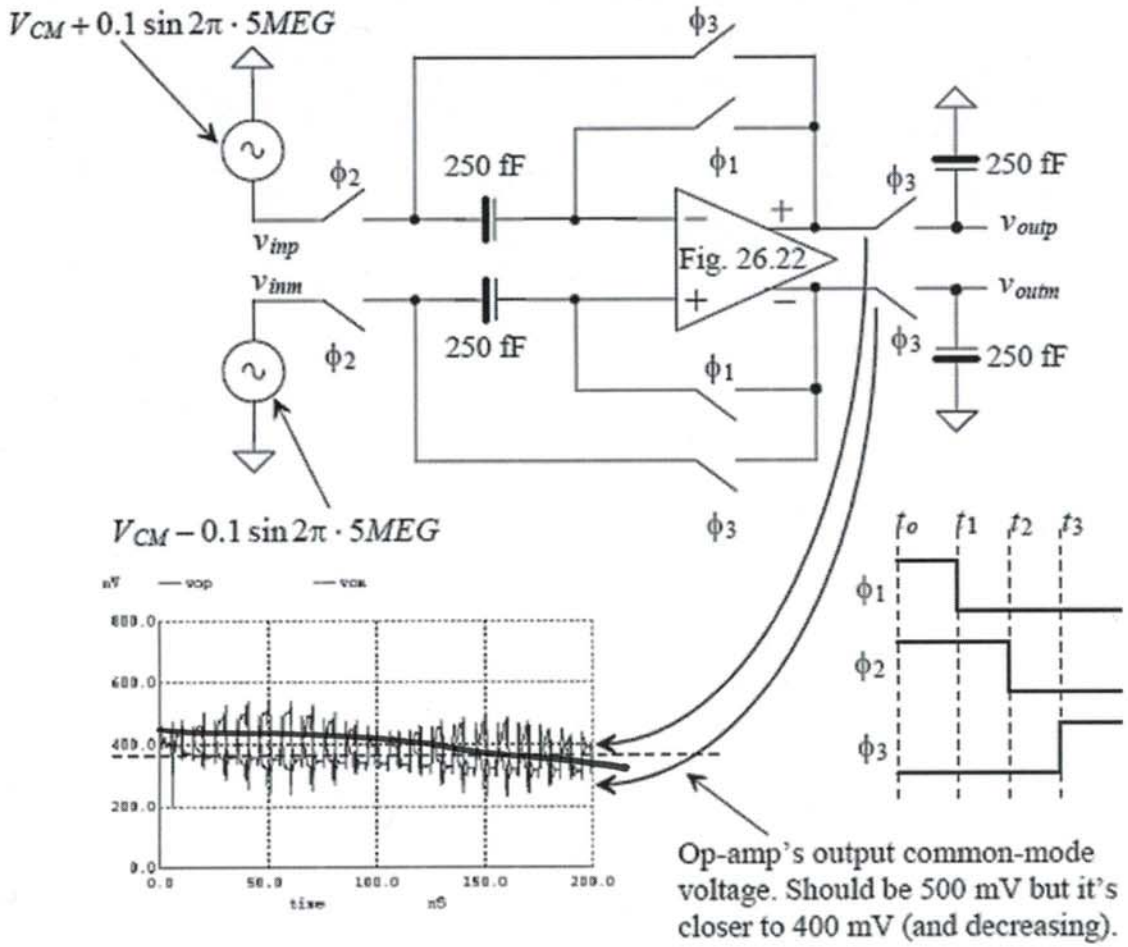


Figure 26.25 A sample-and-hold circuit. Notice how the output common-mode voltage is wandering.

15)

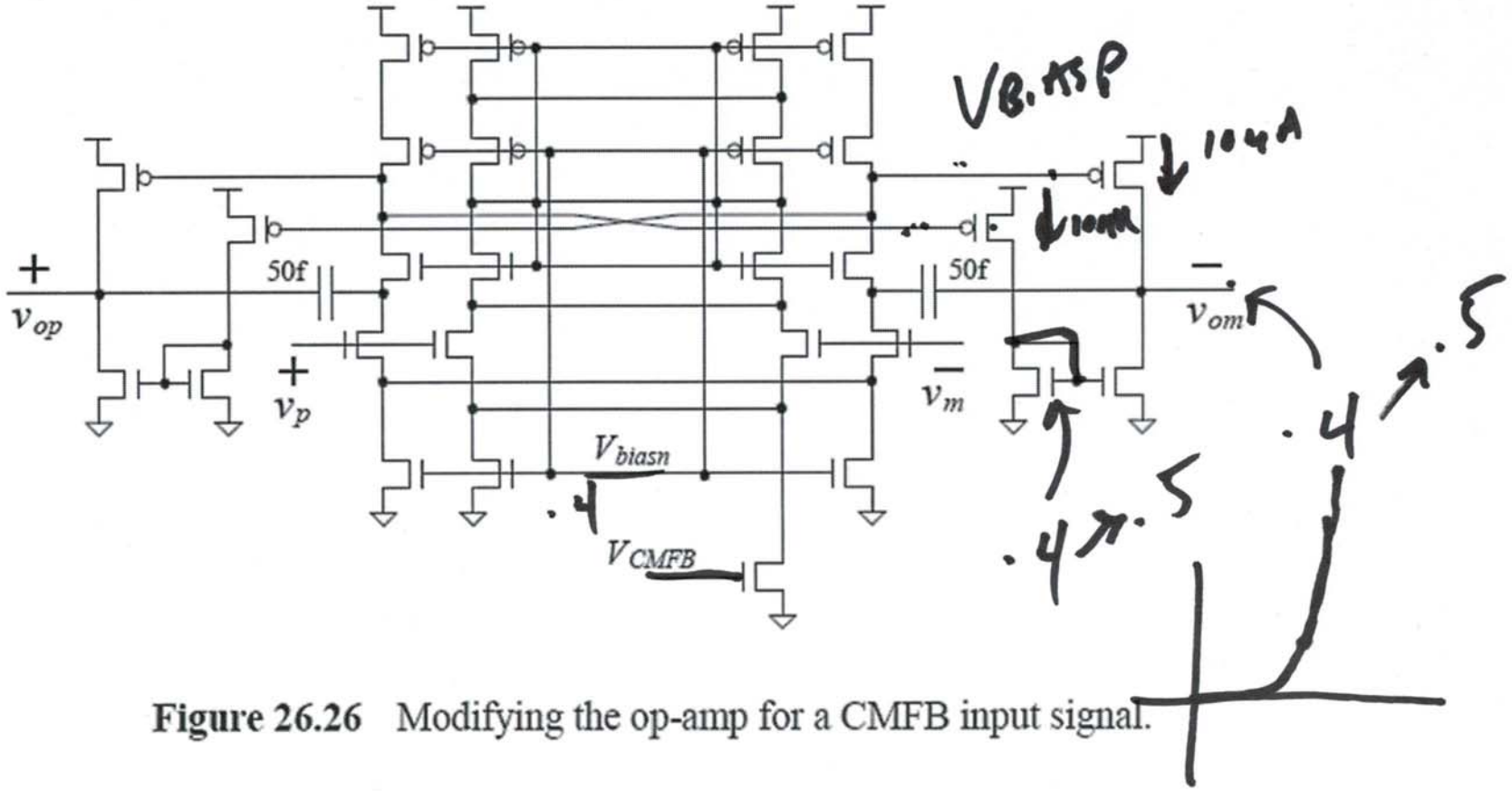


Figure 26.26 Modifying the op-amp for a CMFB input signal.

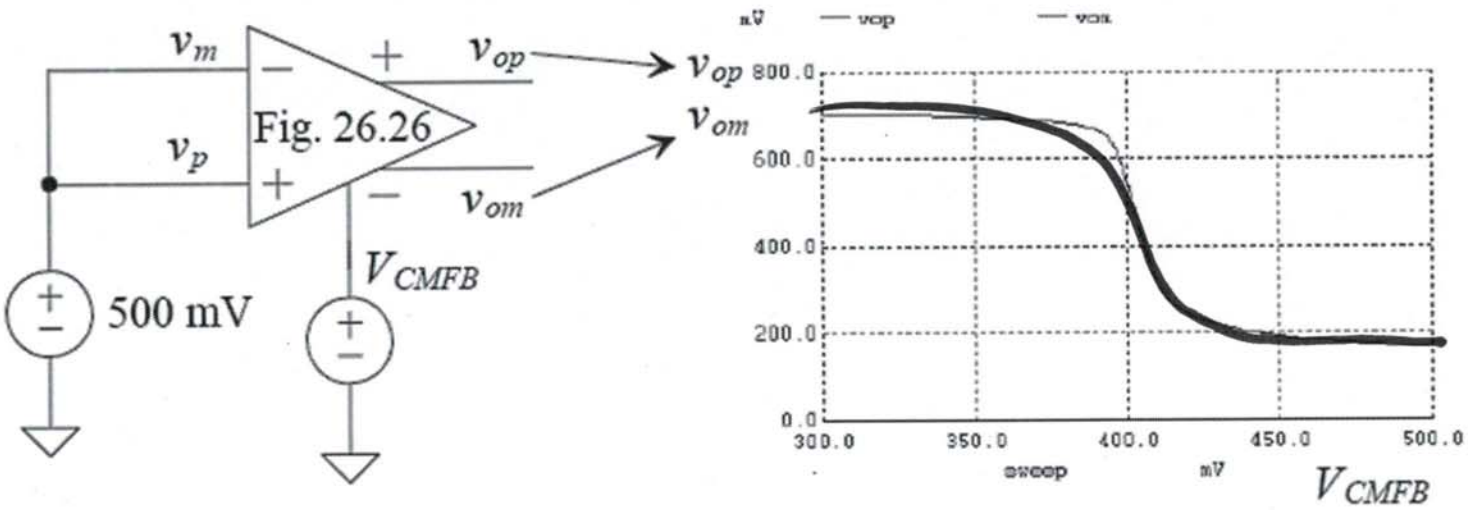


Figure 26.27 The CMFB input to output relationship. The gain is approximately 25 (considerably less than the forward differential gain).