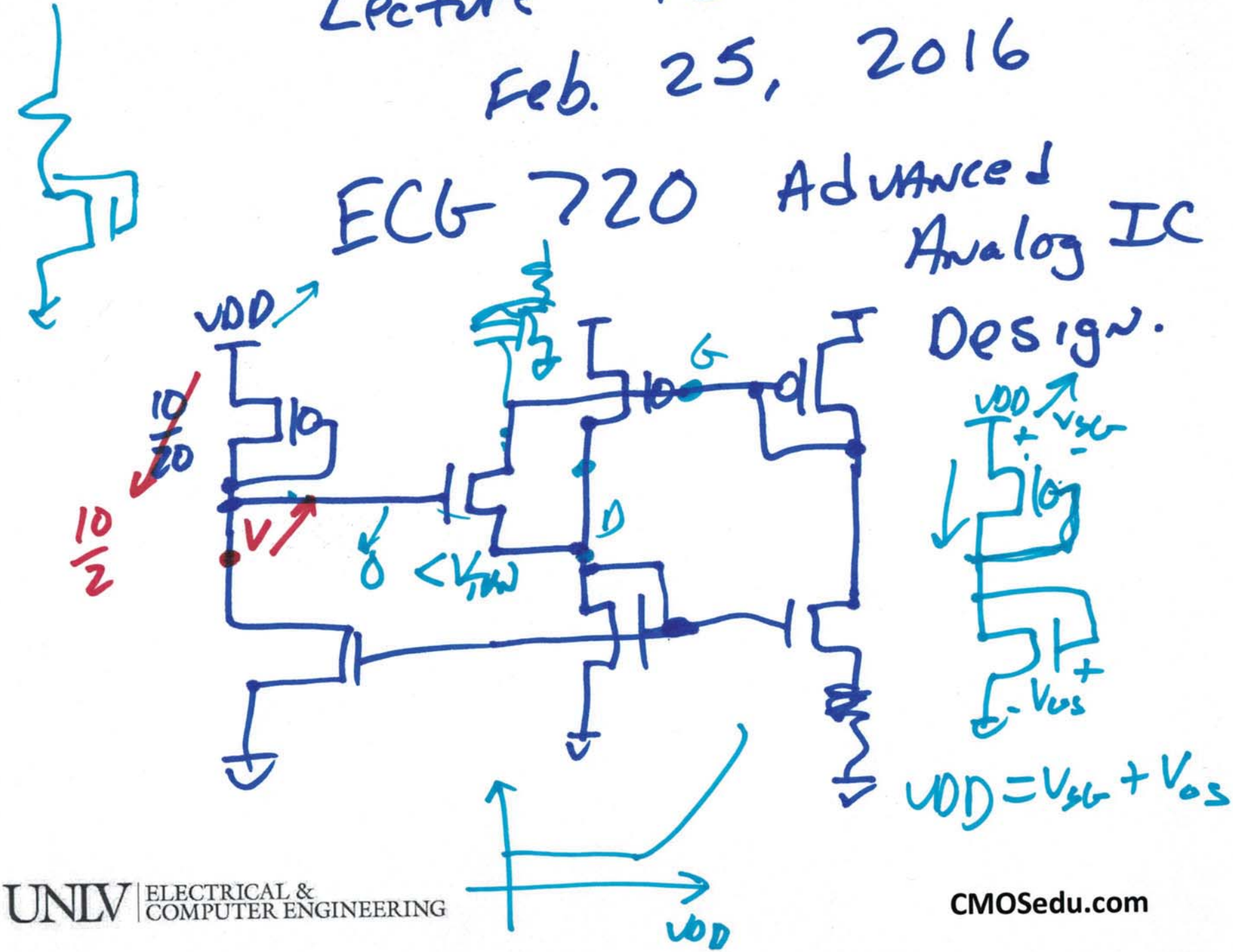
Lecture 12

Feb. 25, 2016

ECG 720 Advanced Analog IC Design.



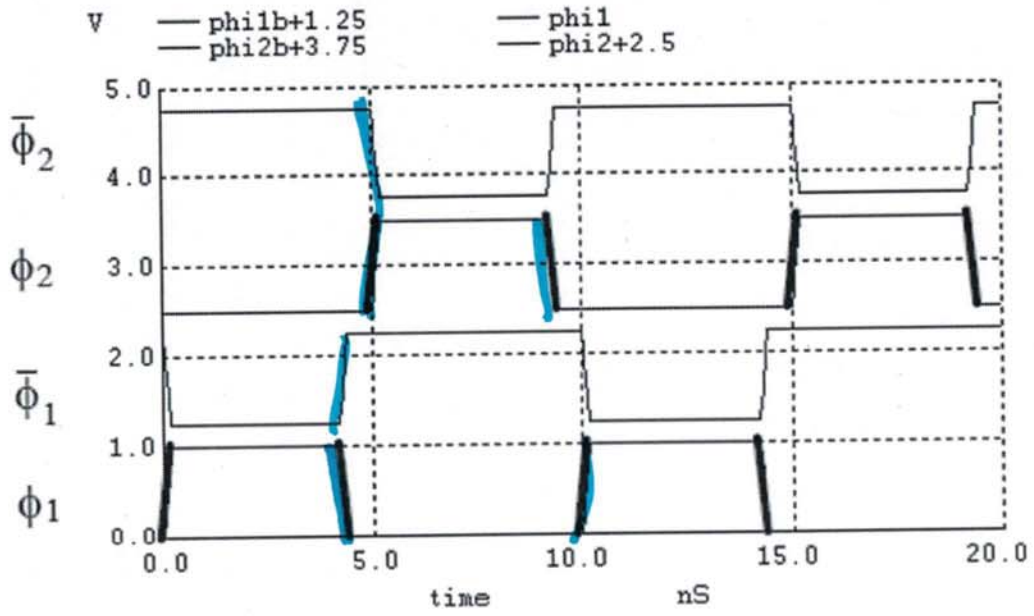
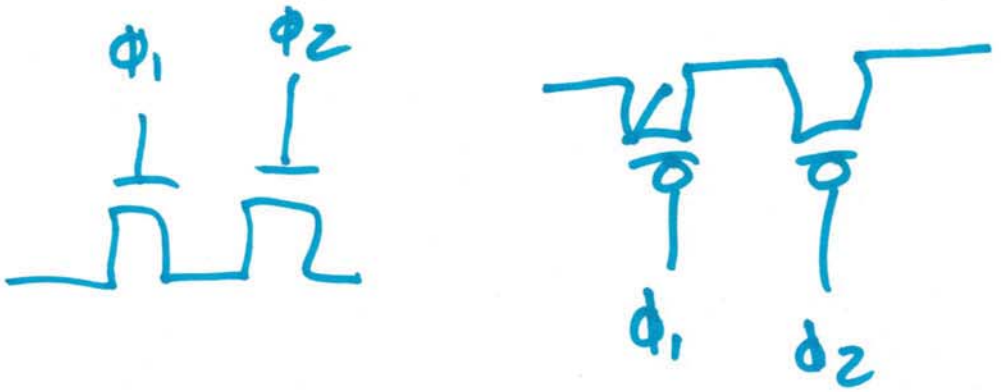


Figure 26.49 Generating nonoverlapping clocks for SC circuits.



2)

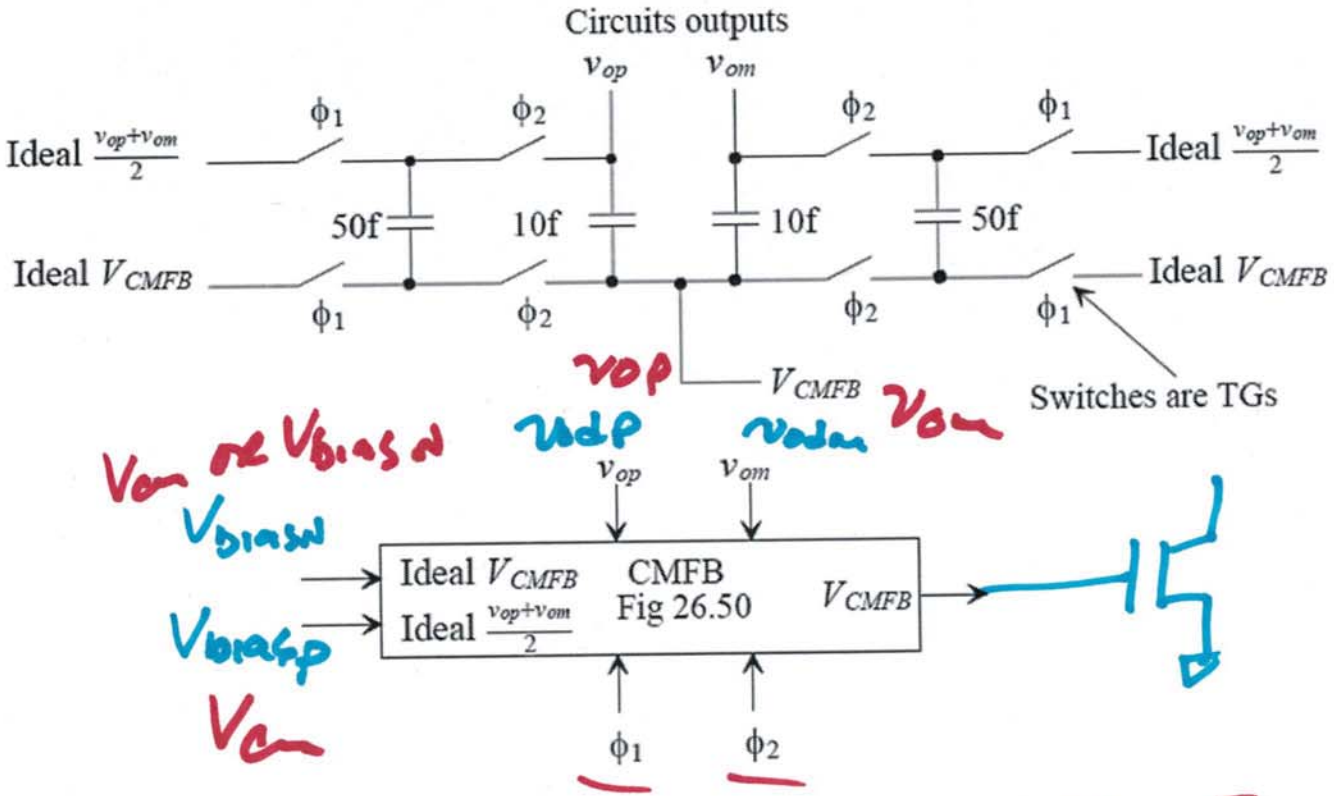
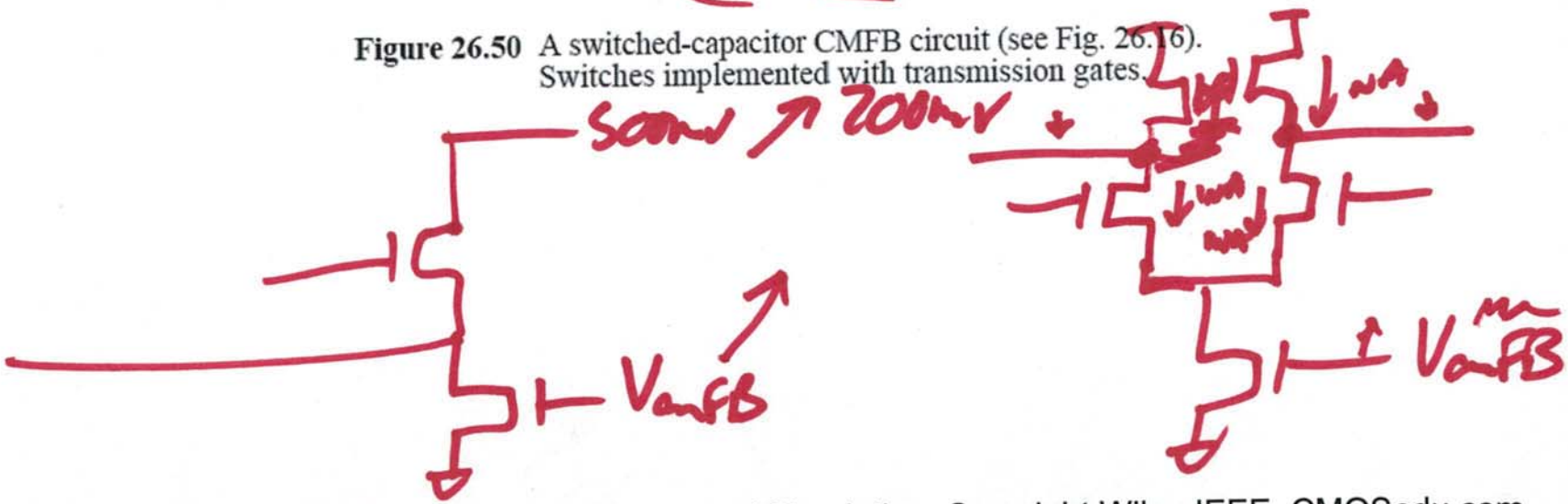


Figure 26.50 A switched-capacitor CMFB circuit (see Fig. 26.16). Switches implemented with transmission gates.



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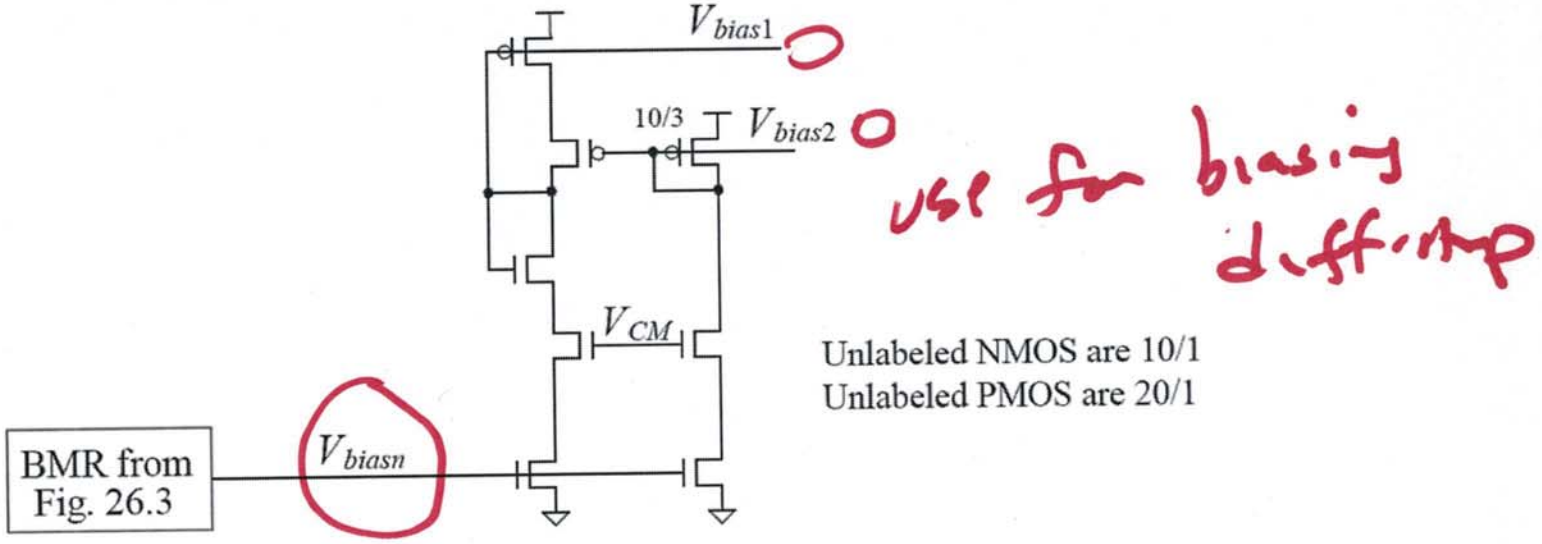
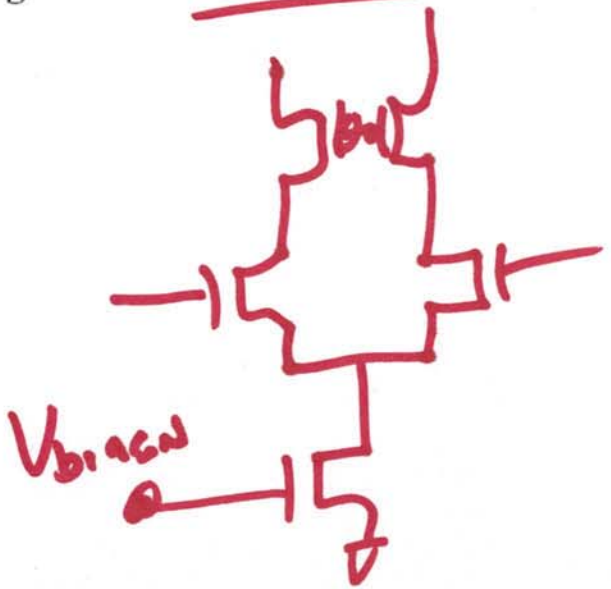
3)

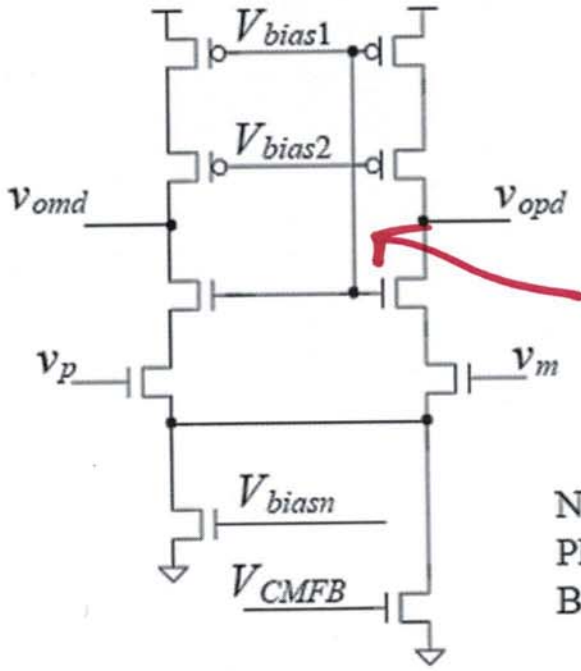


use for biasing diff. amp

Figure 26.52 Biasing circuit for the op-amp developed in this section.



4)



NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.52

(bad) see end of chap.

p. 904 ⇄ p. 26.18 ⇄ 26.19

Figure 26.53 Diff-amp used with the bias circuit of Fig. 26.52.

5)

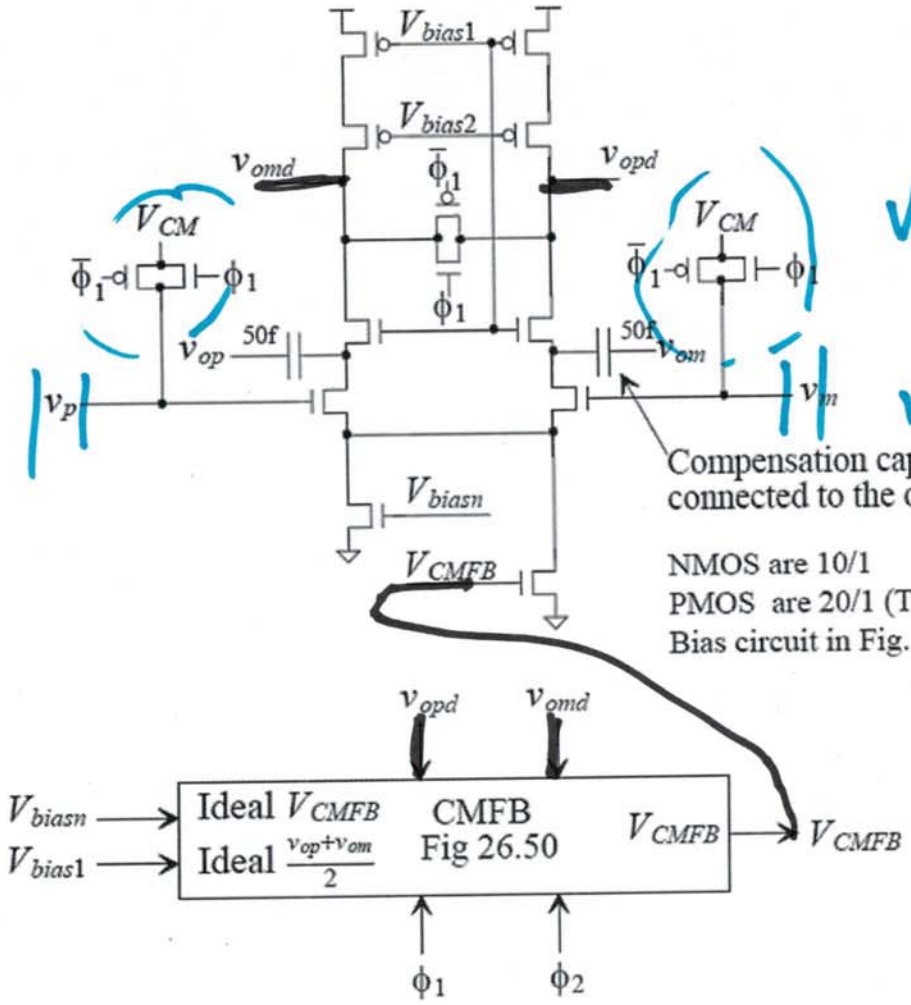
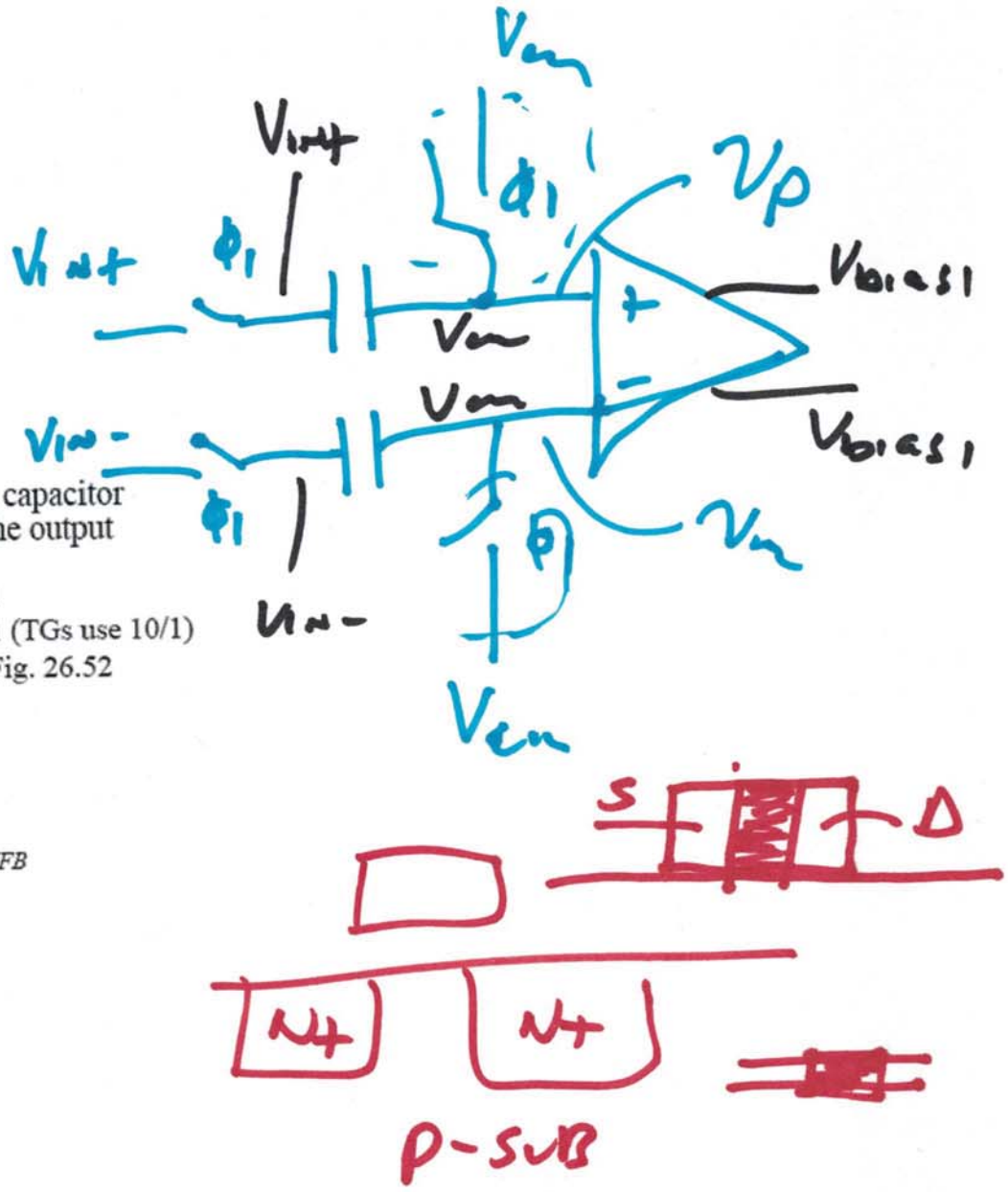


Figure 26.54 First-stage diff-amp with SC CMFB.



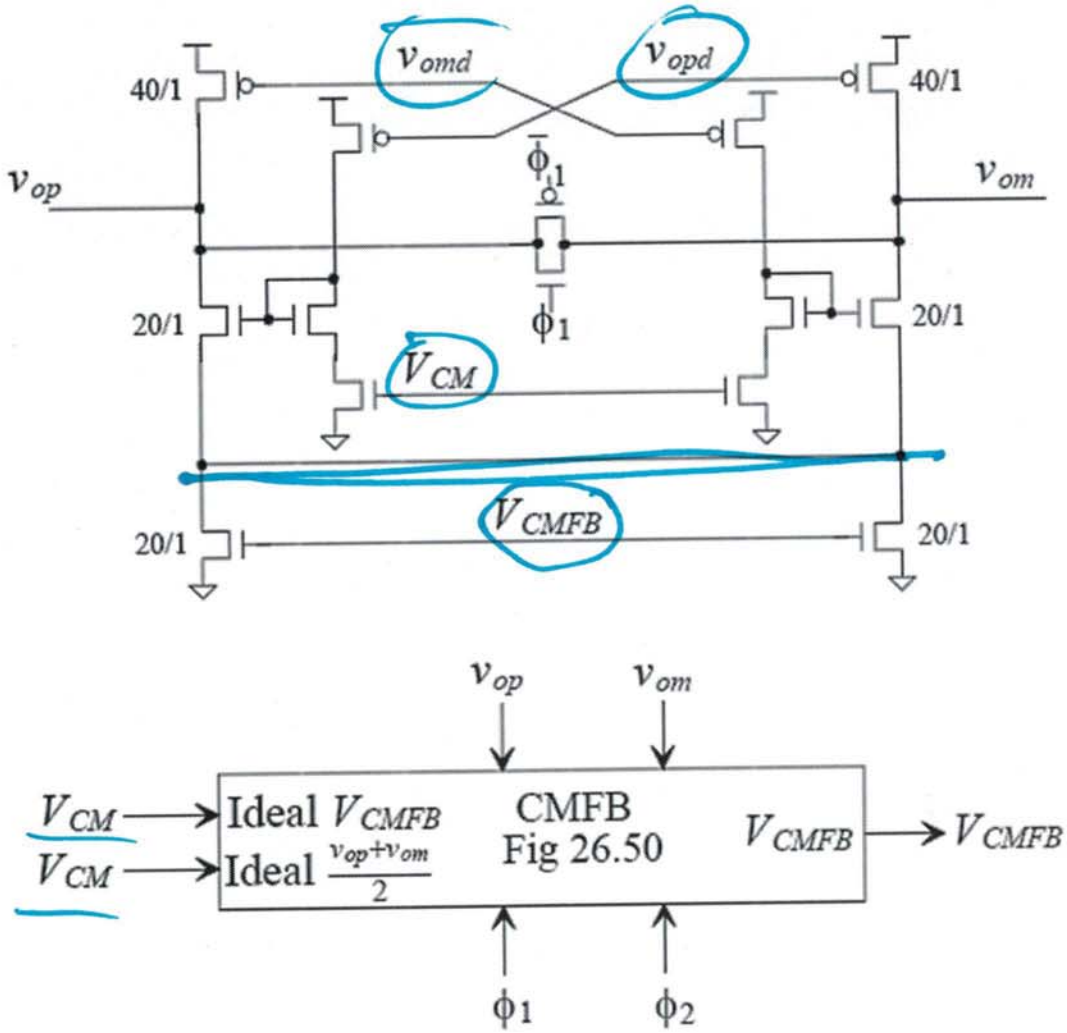
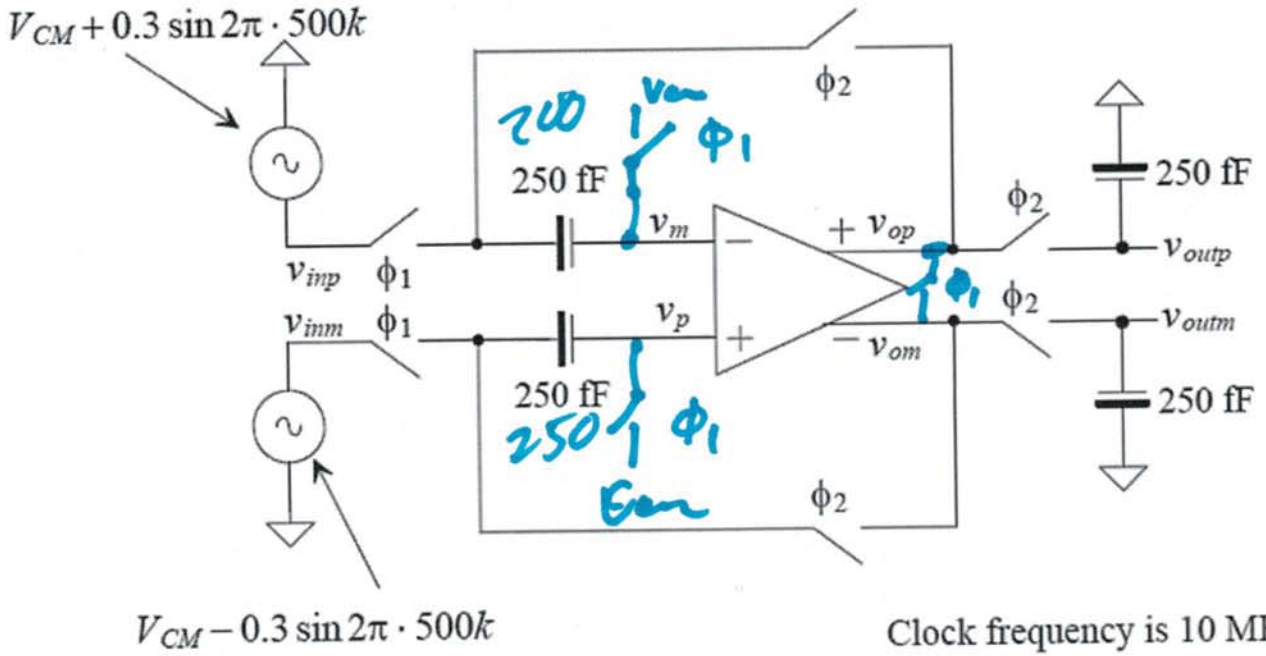


Figure 26.56 Output buffer and CMFB.



Clock frequency is 10 MHz.

Figure 26.58 Simulating the operation of the op-amp formed with the diff-amp in Fig. 26.54 and buffer in Fig. 26.56.

S/H