ECG 720 Lecture 20, April 5, 2016

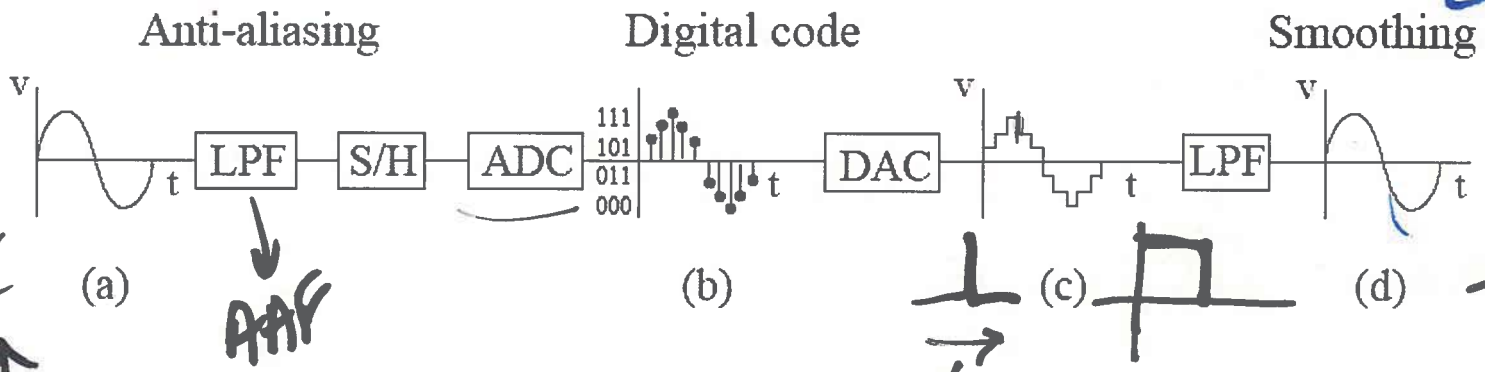
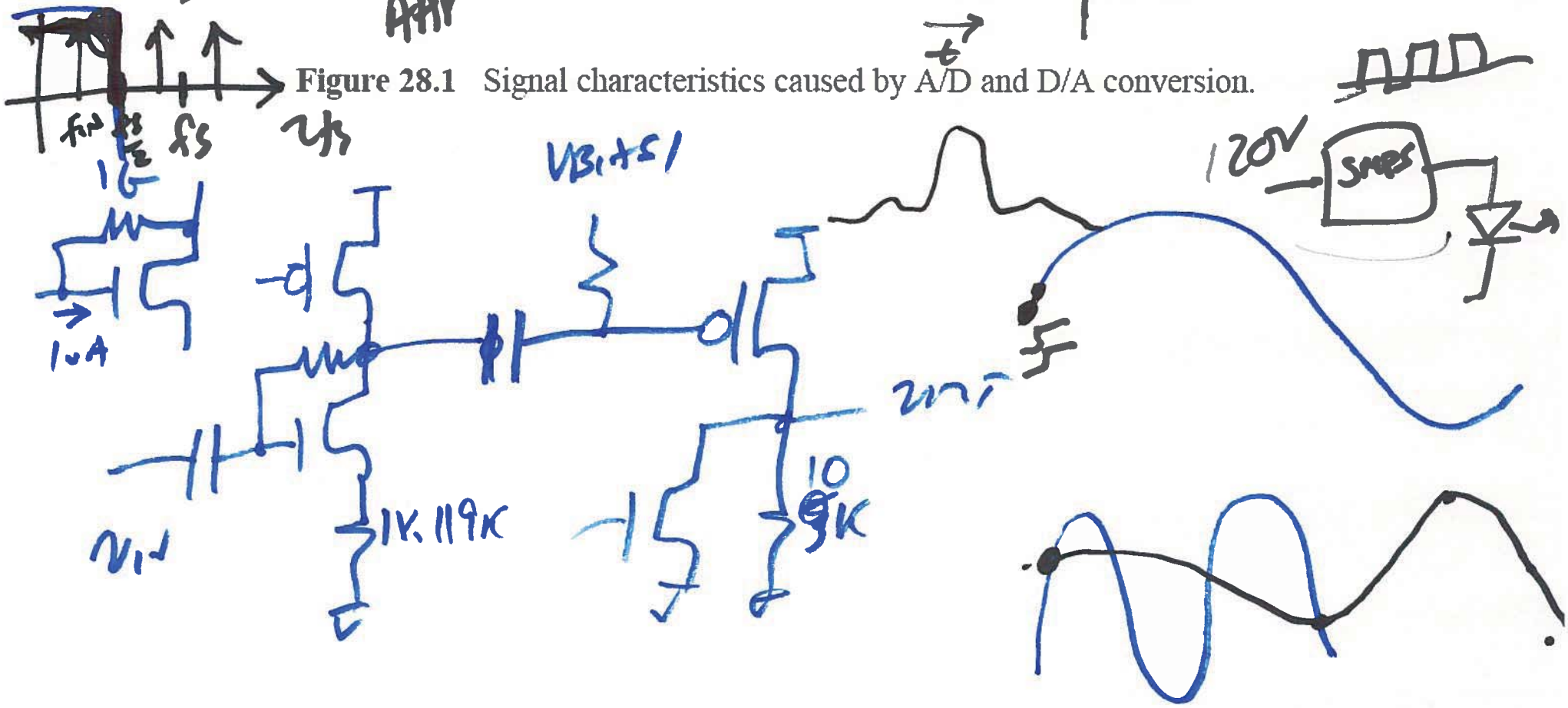


Figure 28.1 Signal characteristics caused by A/D and D/A conversion.



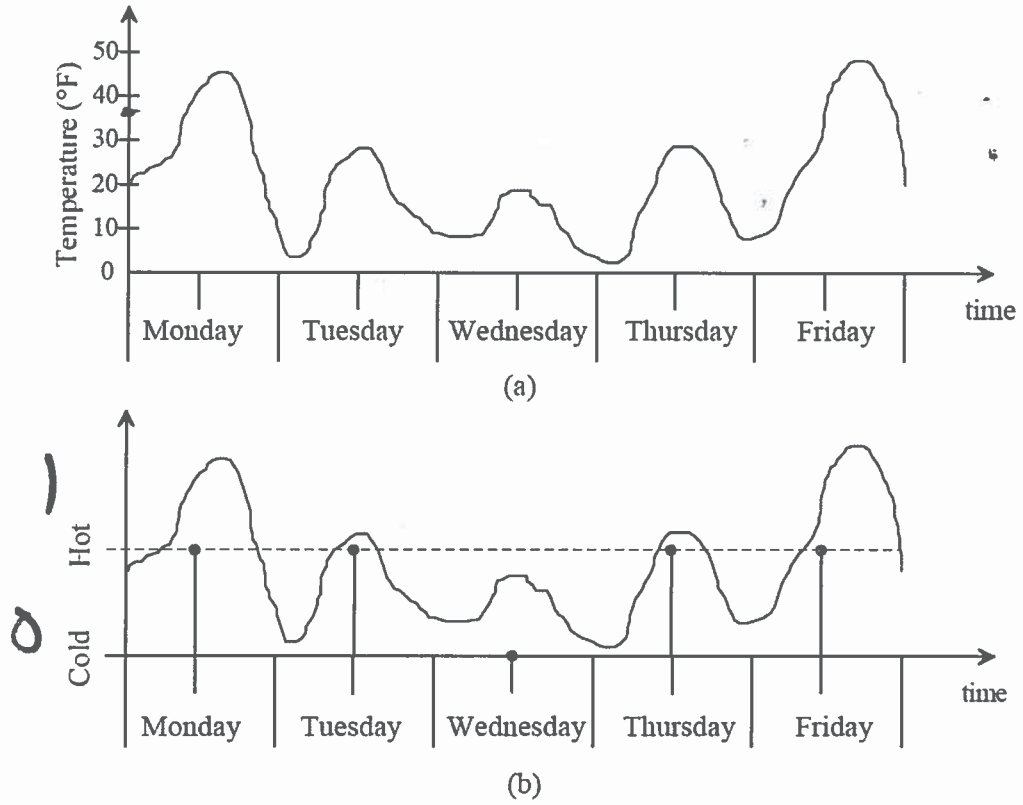


Figure 28.2 (a) An analog signal representing the temperature where you live and (b) a digital representation of the analog signal taking one sample per day with two quantization levels.

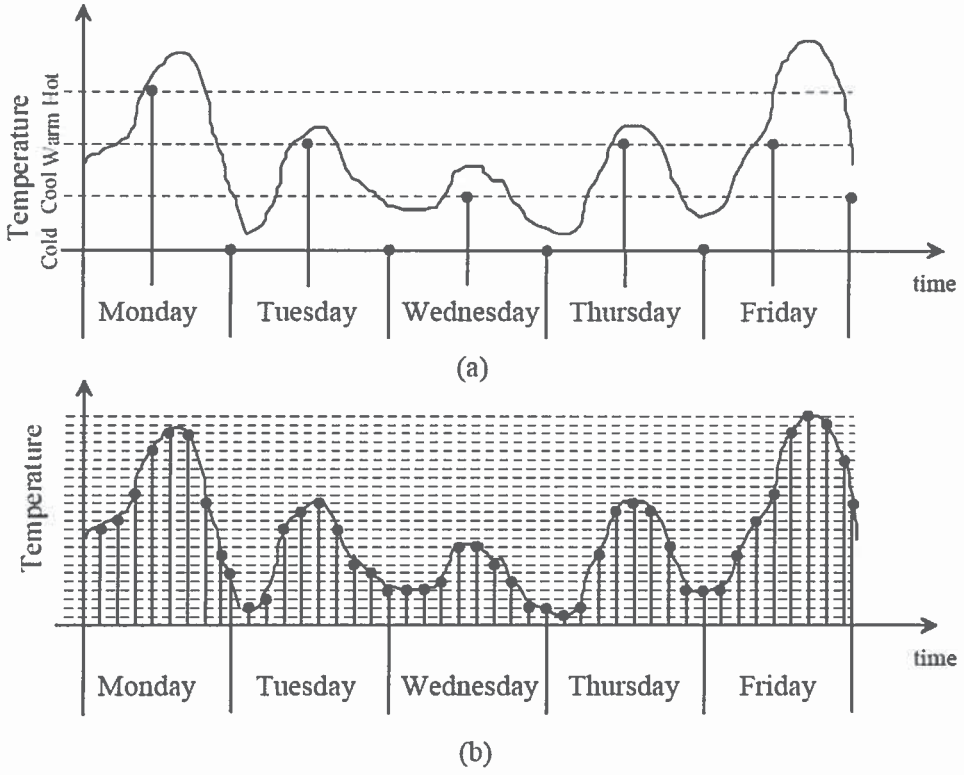
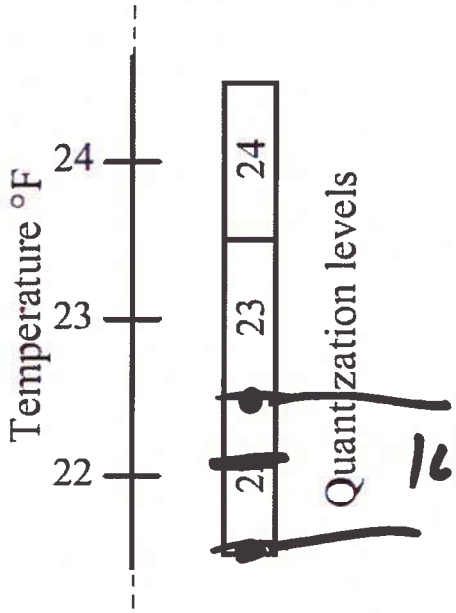


Figure 28.3 Digital representation of the temperature taking (a) two samples per day with four quantization levels and (b) nine samples per day with 25 quantization levels.



1°-quantization
1 LSB
1 LSB 0000 0000
0° → 255°

Figure 28.4 Quantization levels overlap actual temperature by ±½° F.

±½ LSB

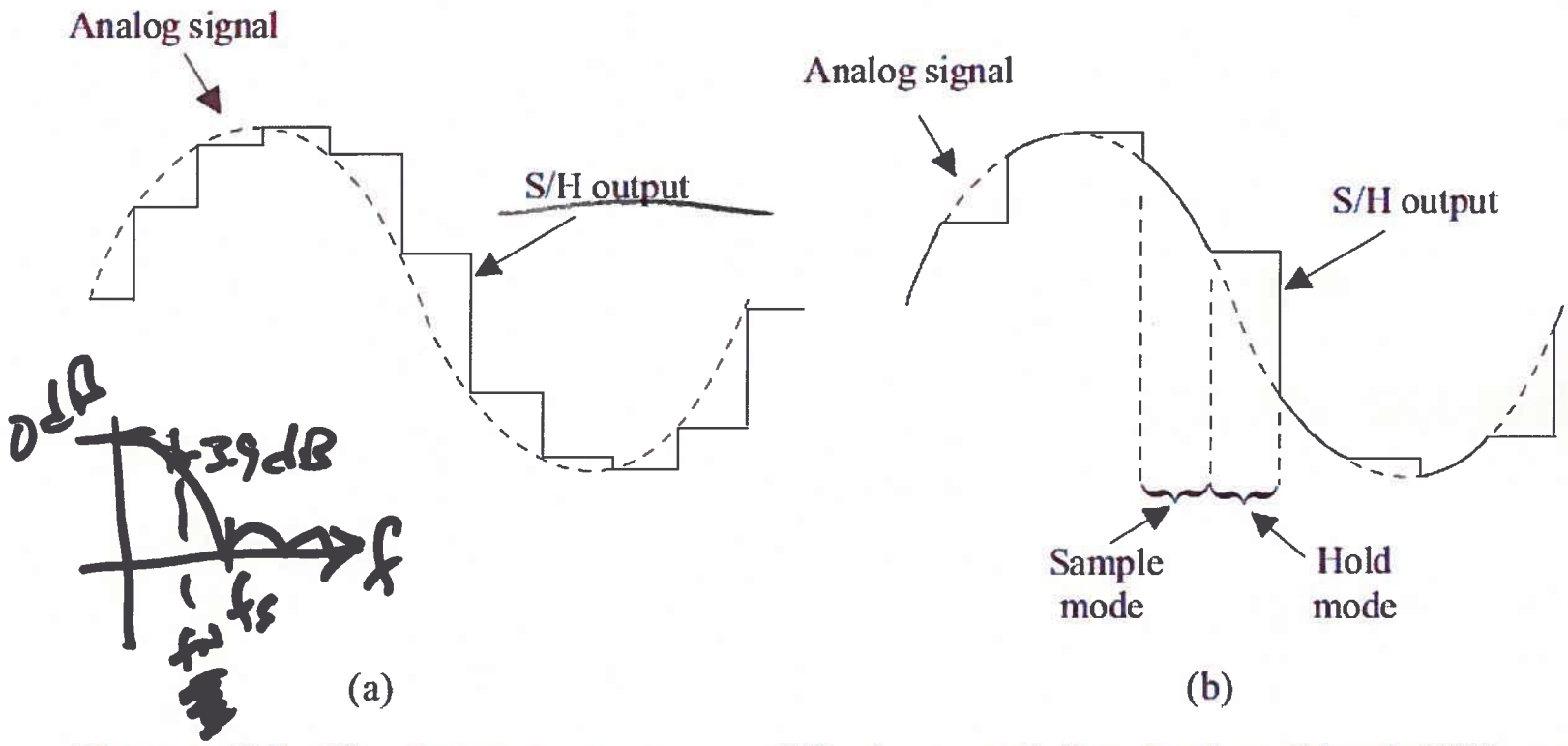
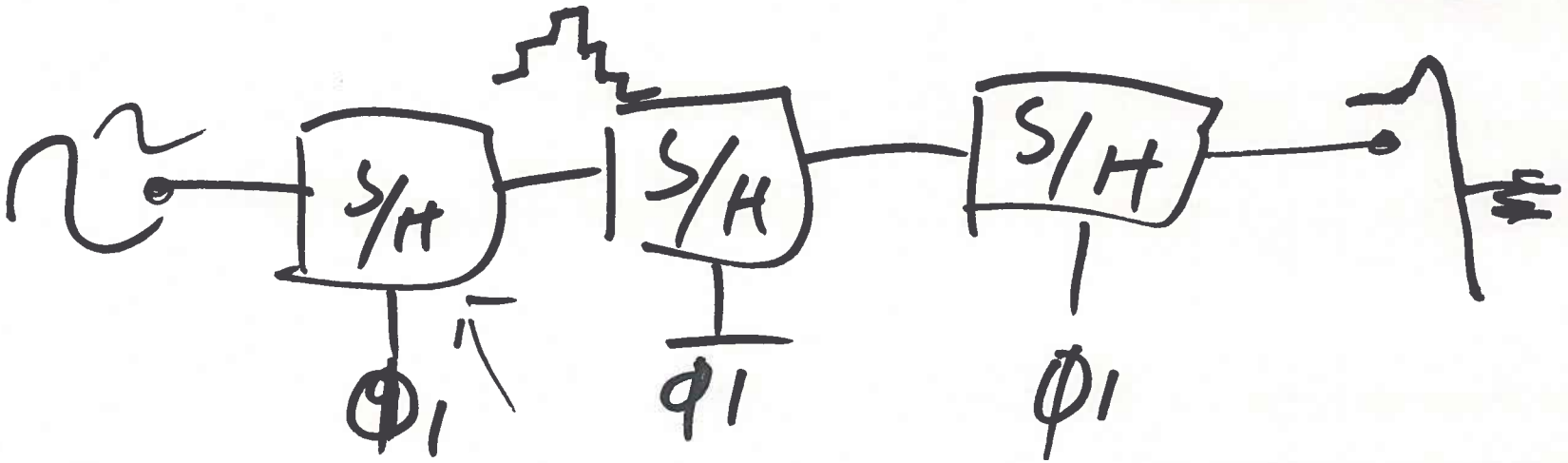


Figure 28.5 The output of (a) an ideal S/H circuit and (b) a track-and-hold (T/H).



5)

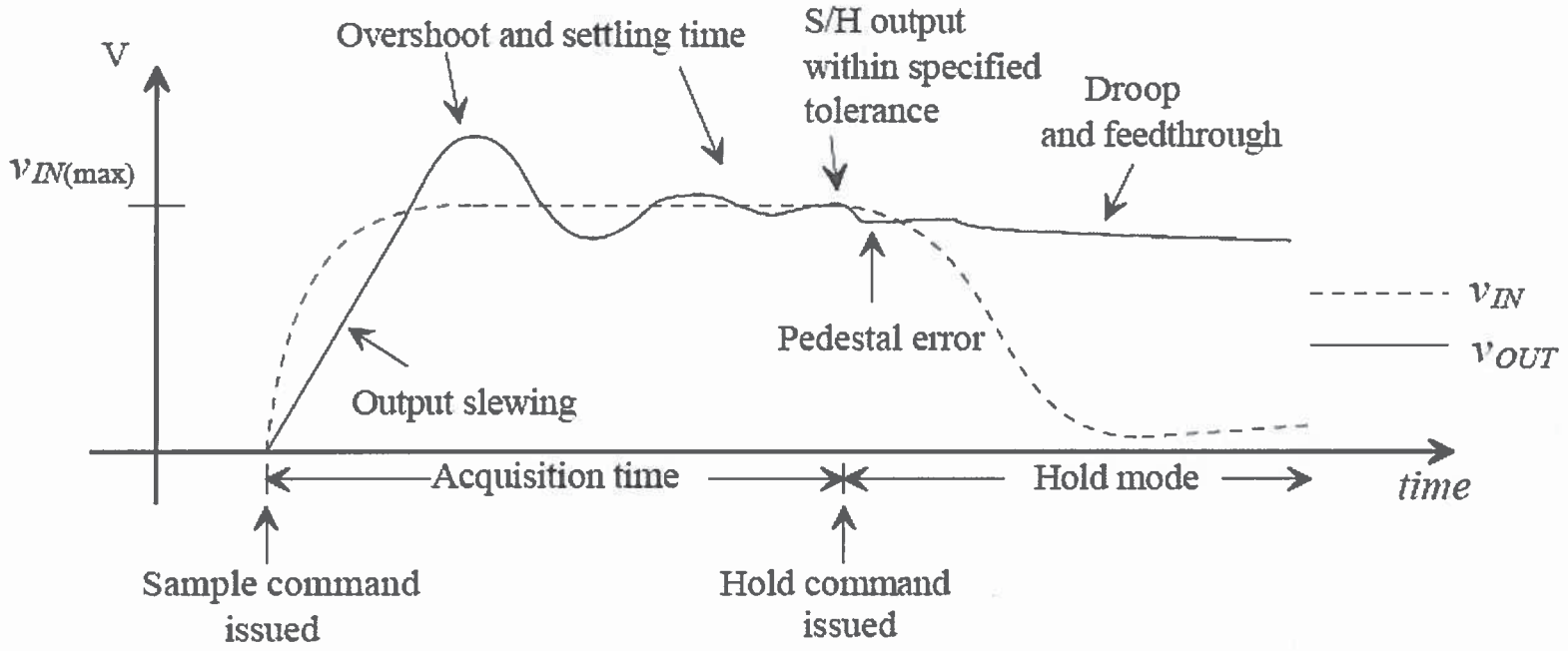


Figure 28.6 Typical errors associated wth an S/H.

$$V_0 = A_{OL}(1 - V_0)$$

1mV

A_{OL} M.U = ?

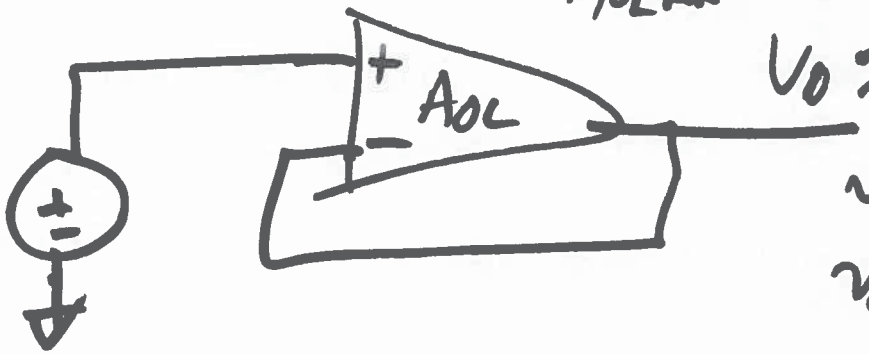
$A_{OL\,min.} \Rightarrow 1{,}000$

$V_0 \approx 1V$

$$V_0(1 + A_{OL}) = A_{OL}$$

1V

$$V_0 = \frac{A_{OL}}{1 + A_{OL}}$$



$v_0 \ggg .999V$

$v_0 < 1V$

6)

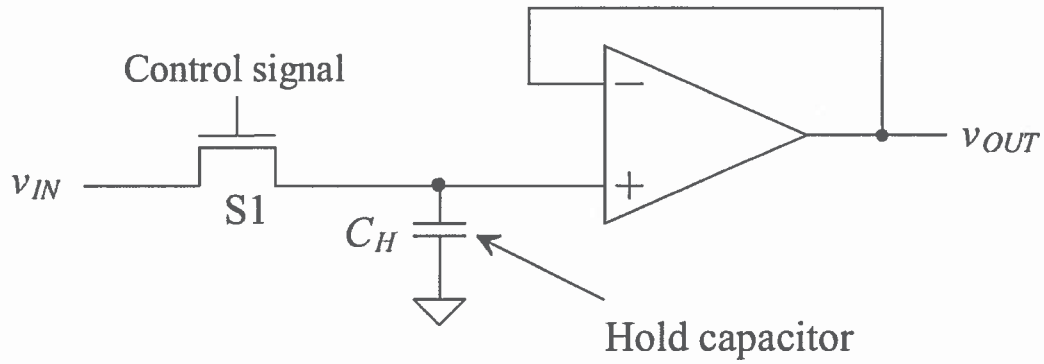


Figure 28.7 Track-and-hold circuit using an output buffer.

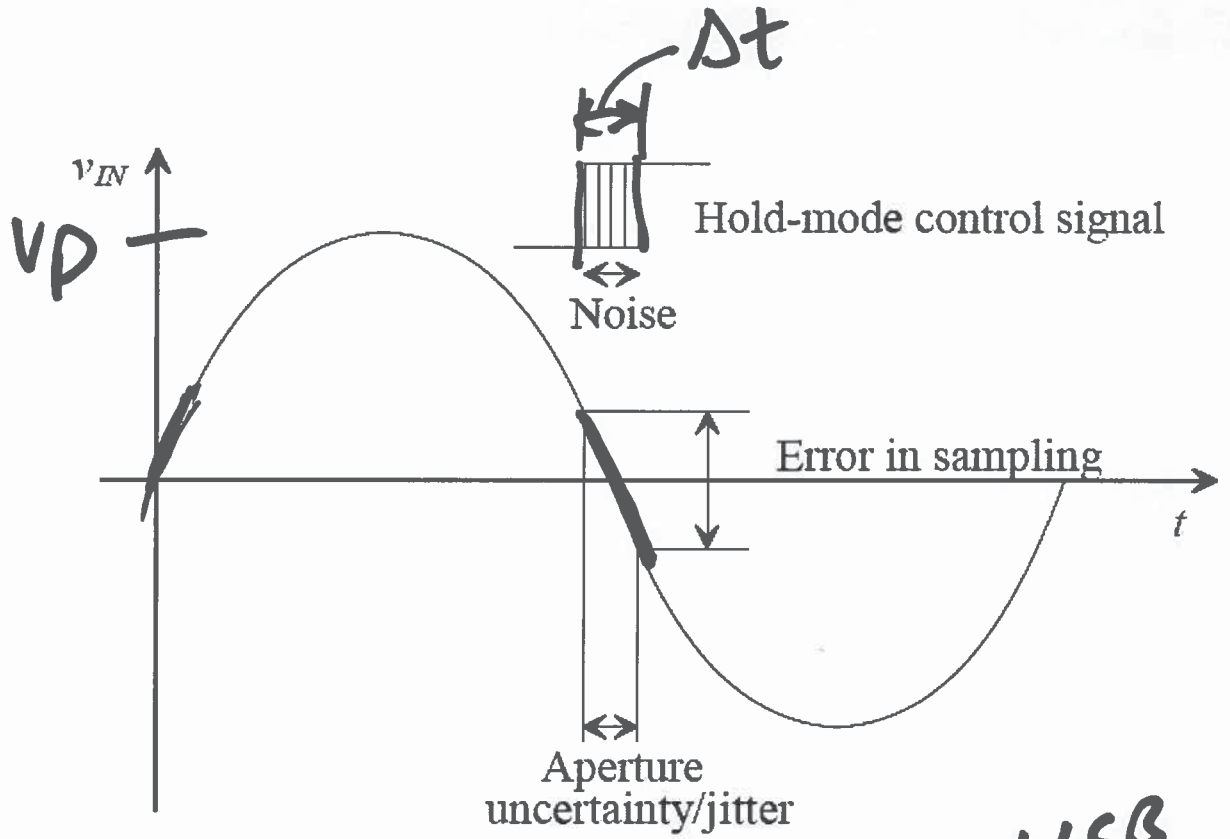


Figure 28.8 Aperture error.

$$\frac{1LSB}{\Delta t} = V_p \cdot 2\pi f$$

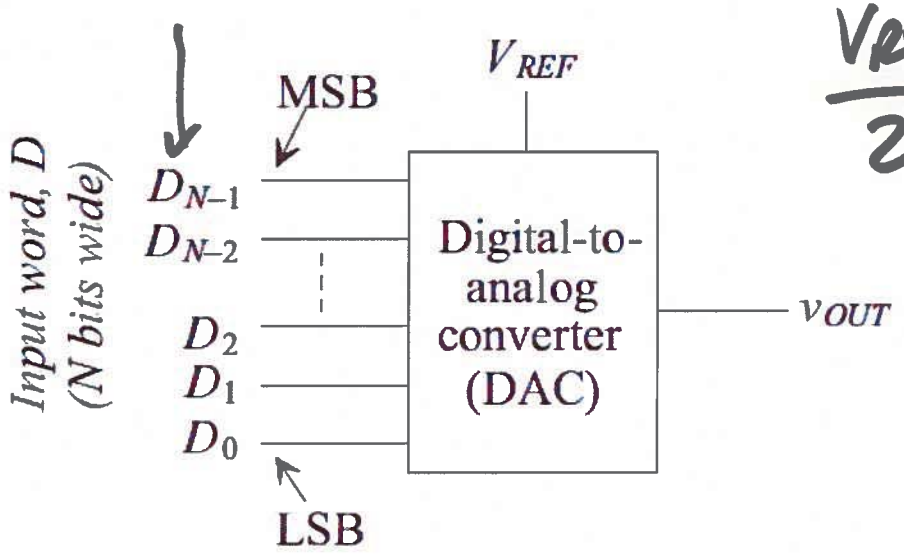
jitter

$$v_{in} = V_p \cdot \sin 2\pi f \cdot t$$

$$\frac{dv_{in}}{dt} = V_p \cdot 2\pi f \cdot \cos 2\pi f t$$

8)

D=1 OR D=0



$\frac{V_{REF}}{2^N} = 1LSB$

1LSB

N>1

Figure 28.9 Block diagram of the digital-to-analog converter.

$$V_{OUT} = \frac{V_{REF}}{2^N} \cdot \left(\frac{D_0}{2^N} + \frac{2D_1}{2^{N-1}} + \frac{4D_2}{2^{N-2}} + 2^3 \cdot D_3 + \cdots \frac{2^{N-2} D_{N-2}}{2^2} + \frac{2^{N-1} \cdot D_{N-1}}{2} \right)$$

9)

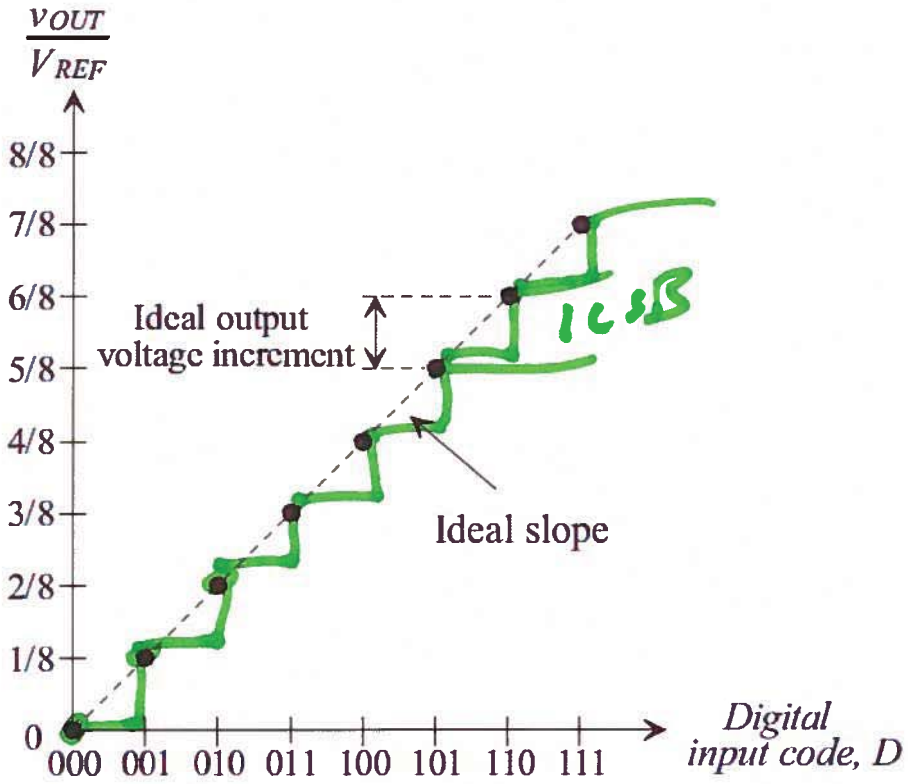


Figure 28.10 Ideal transfer curve for a 3-bit DAC.

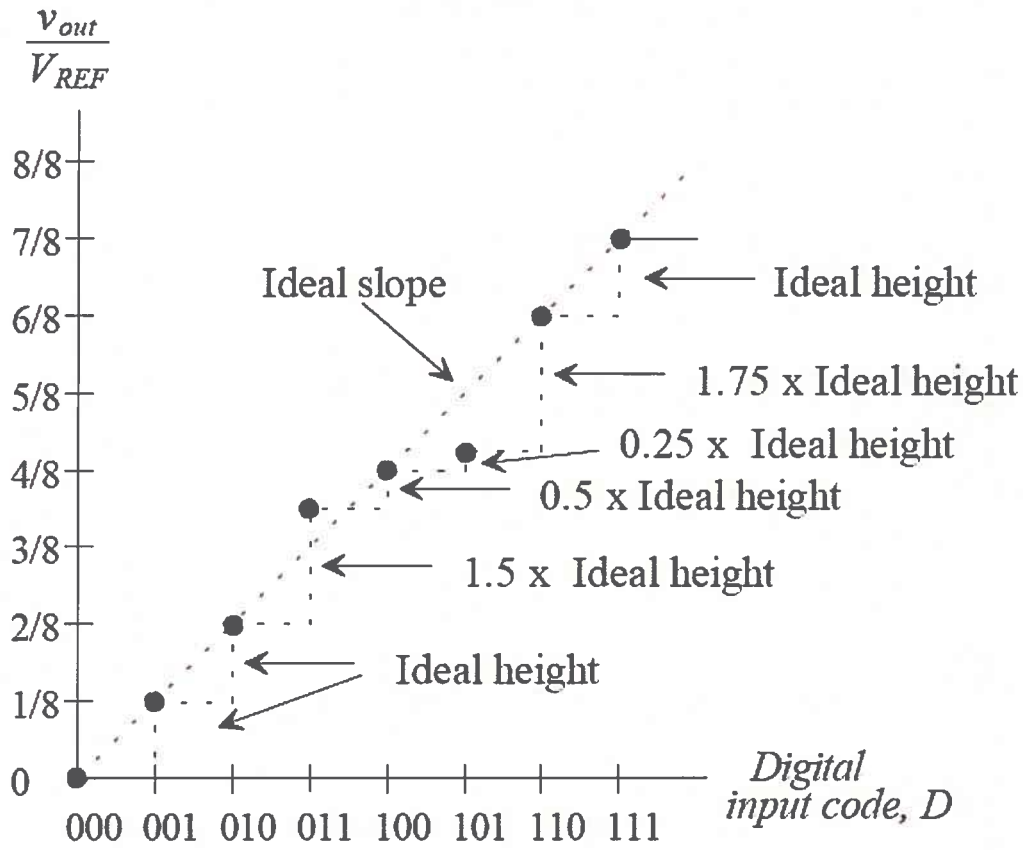


Figure 28.11 Example of differential nonlinearity for a 3-bit DAC.

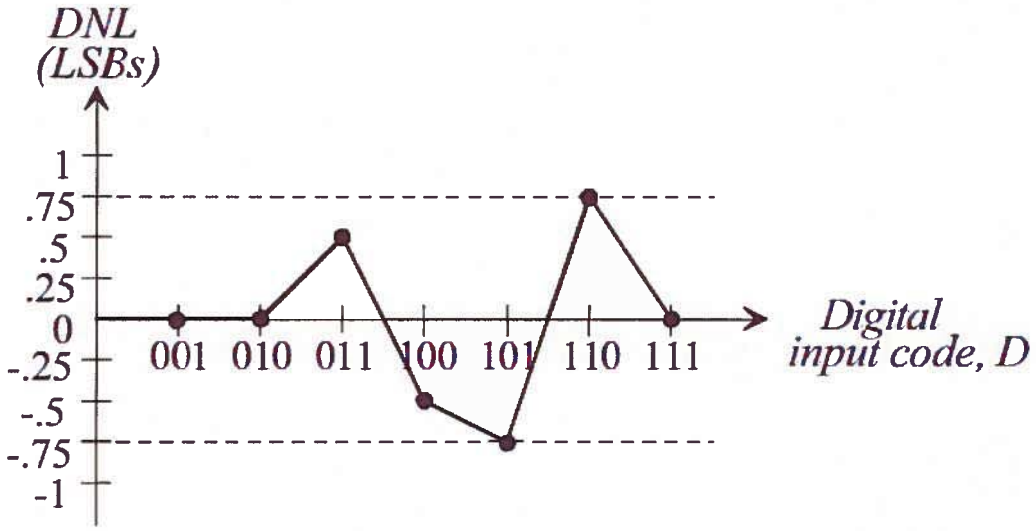


Figure 28.12 DNL curve for the nonideal 3-bit DAC.

$|DNL| < \frac{1}{2} LSB$

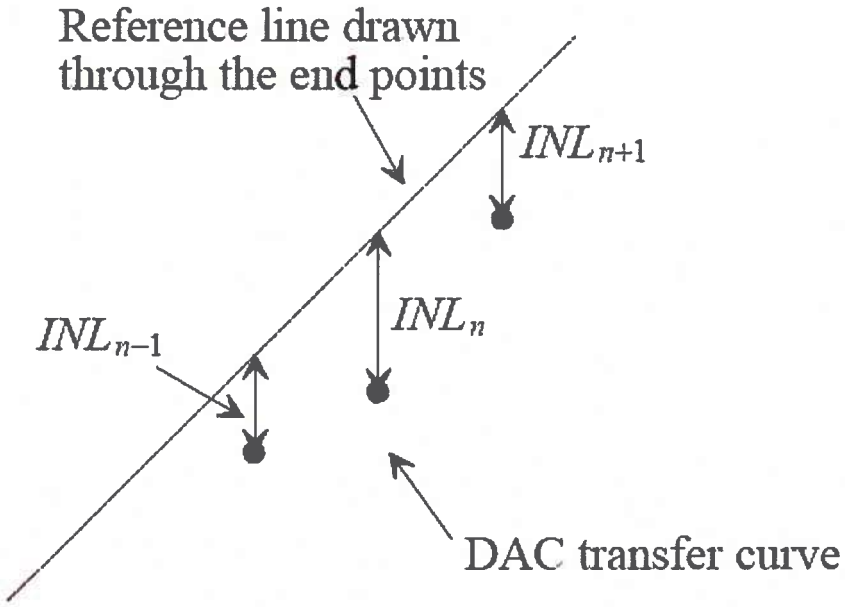
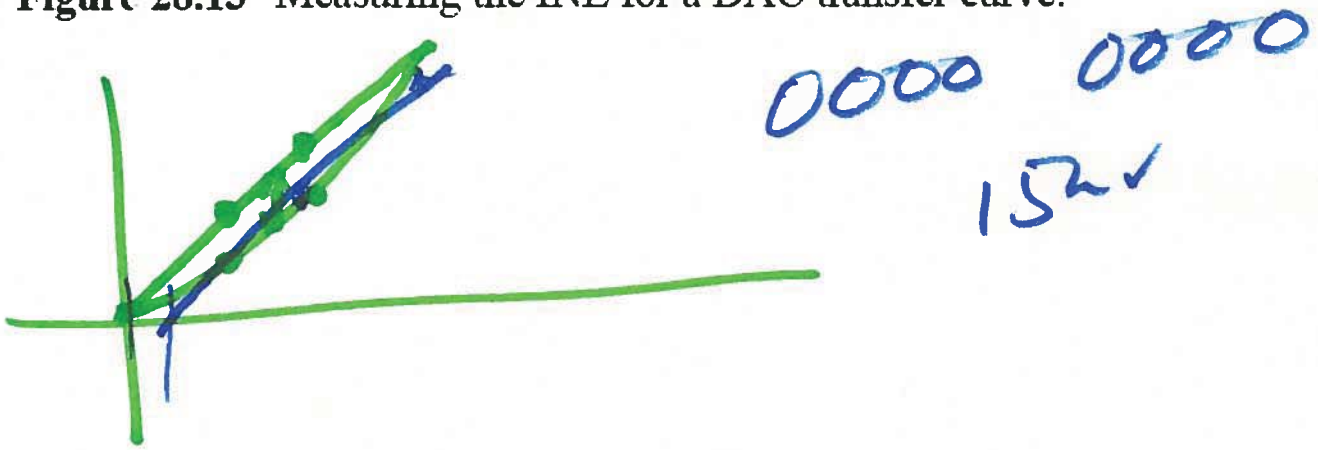


Figure 28.13 Measuring the INL for a DAC transfer curve.



13)

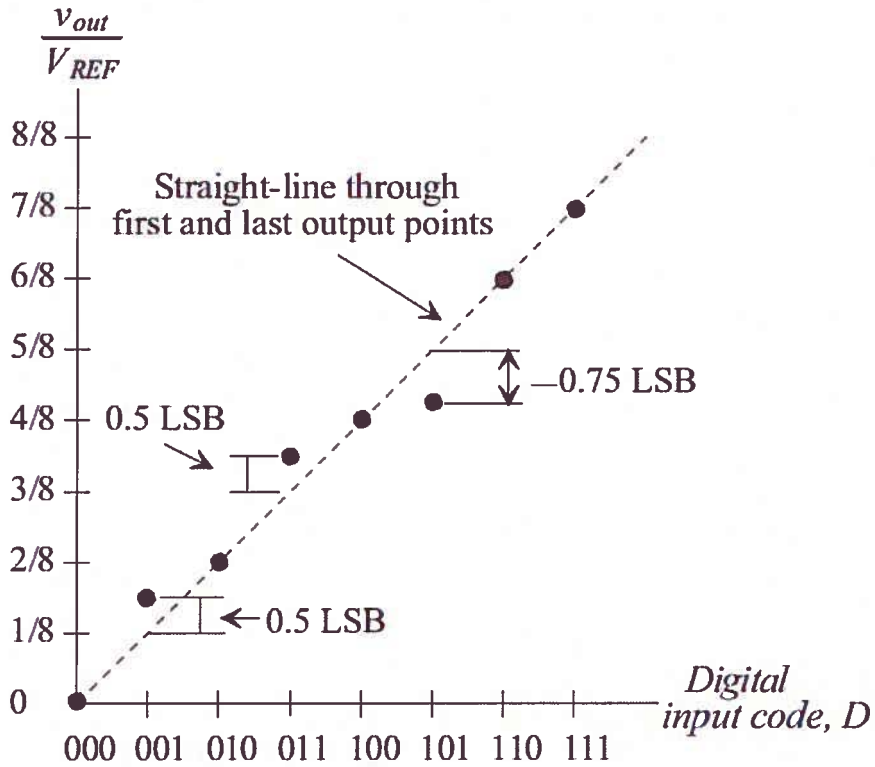


Figure 28.14 Example of integral nonlinearity for a DAC.

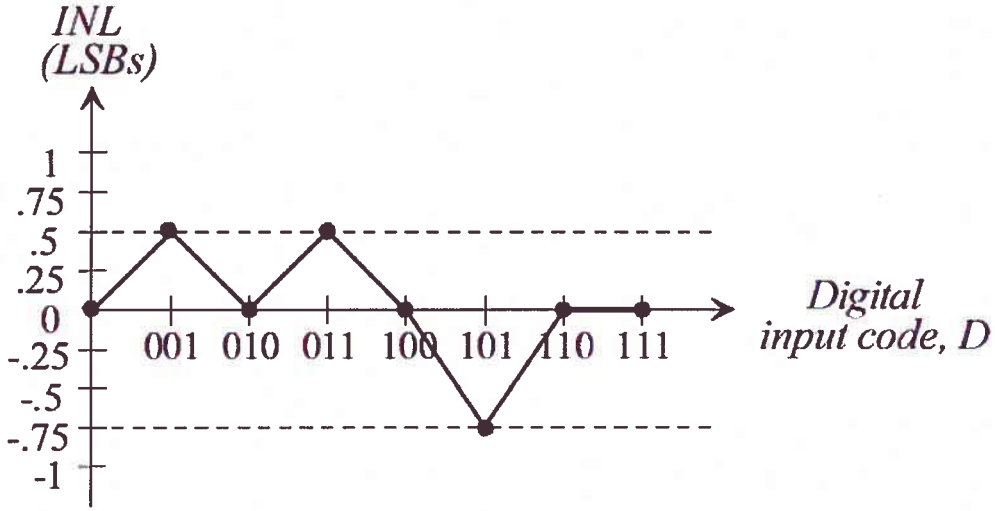


Figure 28.15 INL curve for the nonideal 3-bit DAC.

Integral NONLinearity

INL

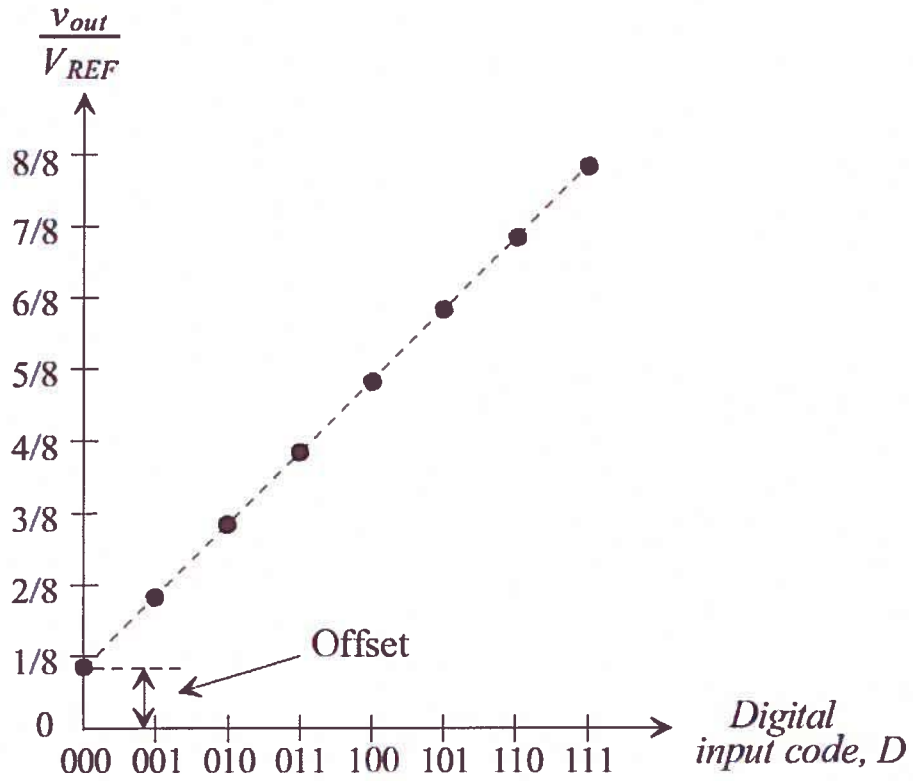


Figure 28.16 Illustration of offset error for a 3-bit DAC.

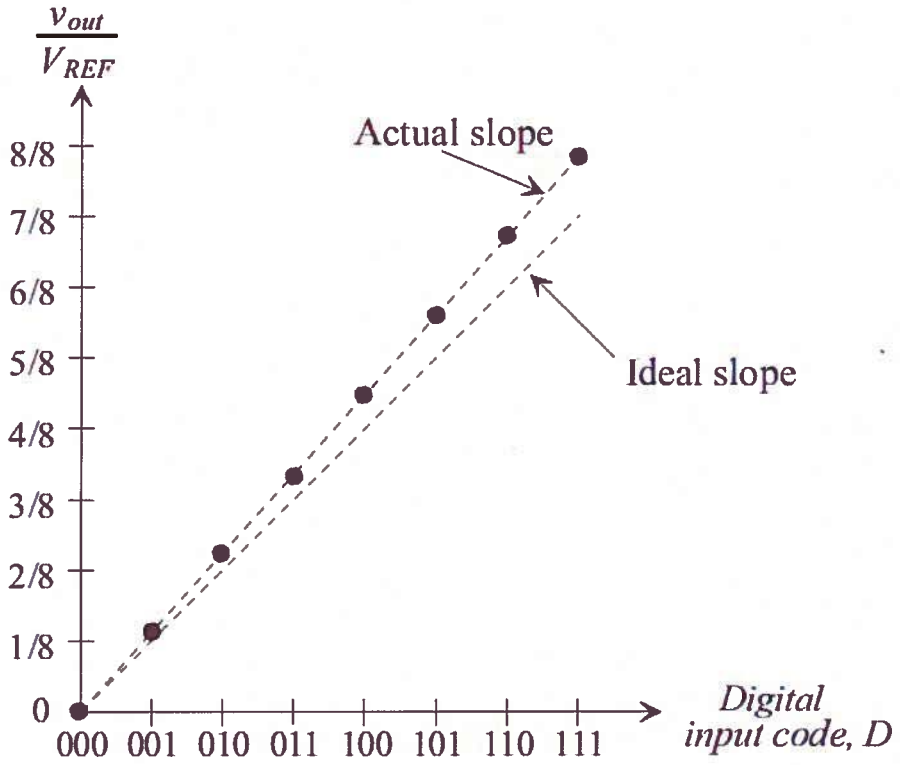


Figure 28.17 Illustration of gain error for a 3-bit DAC.

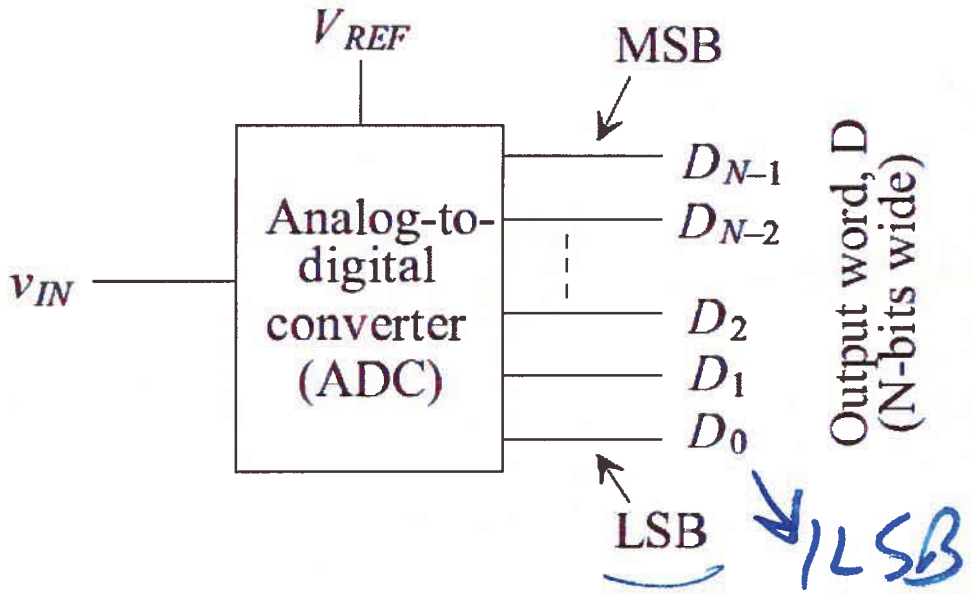
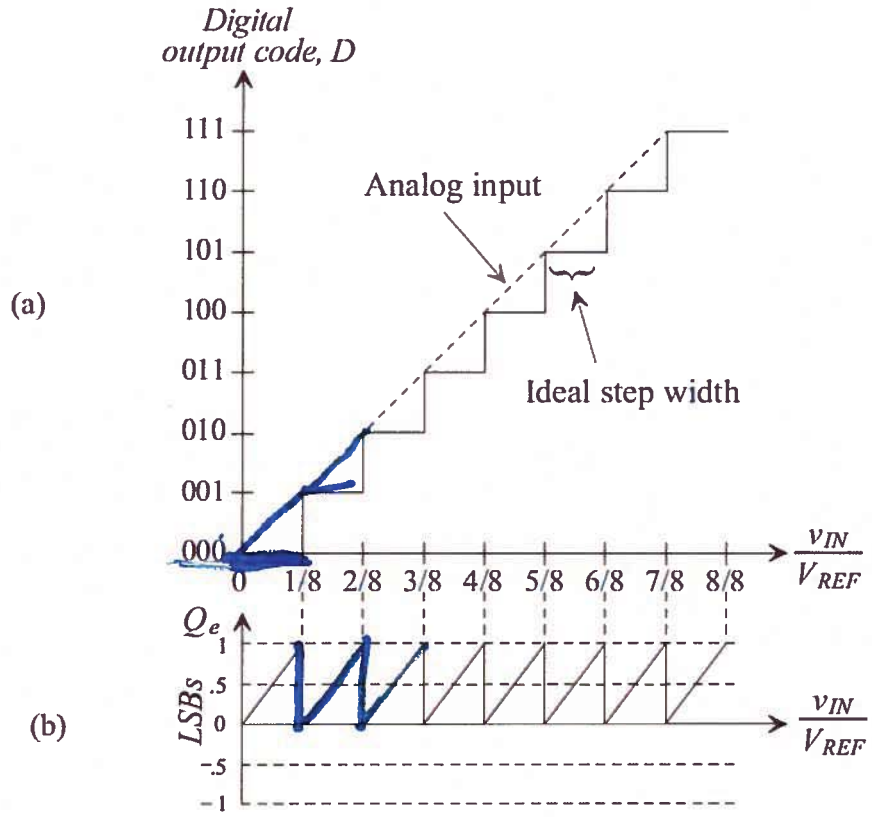


Figure 28.18 Block diagram of the analog-to-digital converter.



Analog input

Figure 28.19 (a) Transfer curve for an ideal ADC and (b) its corresponding quantization error.

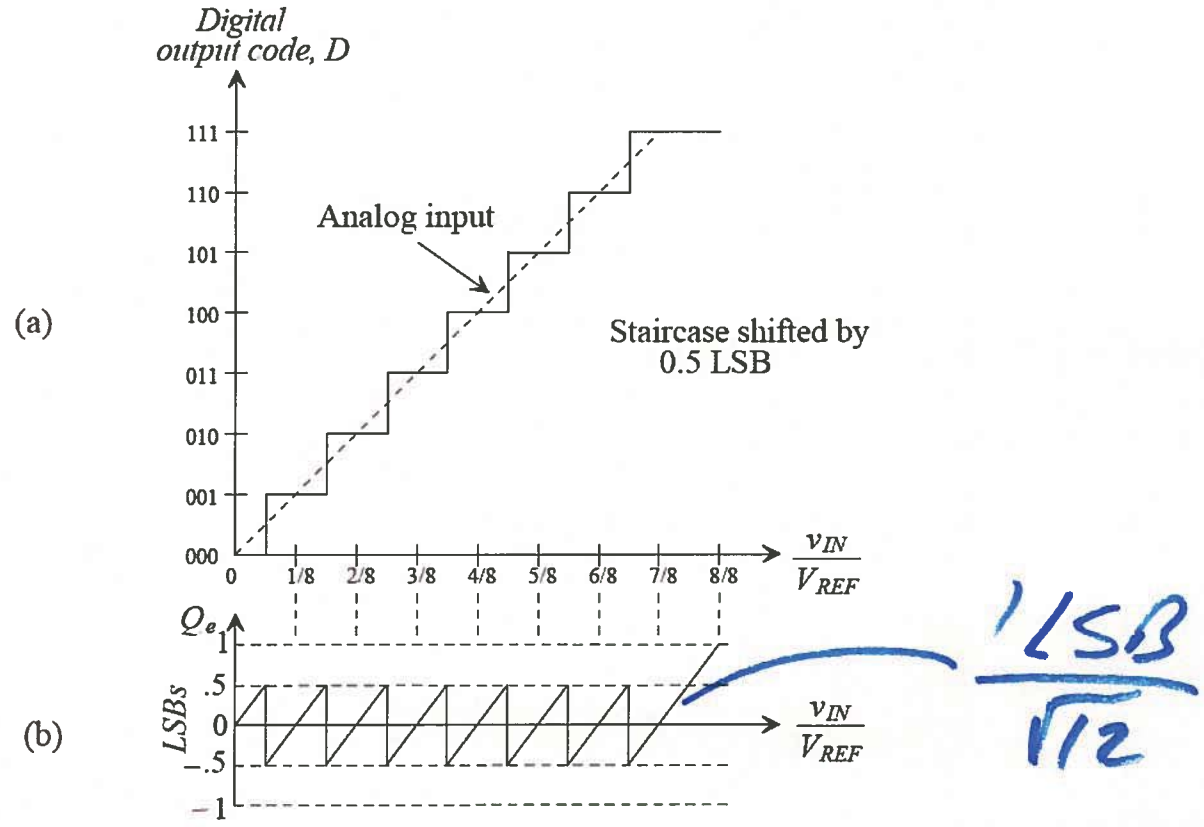
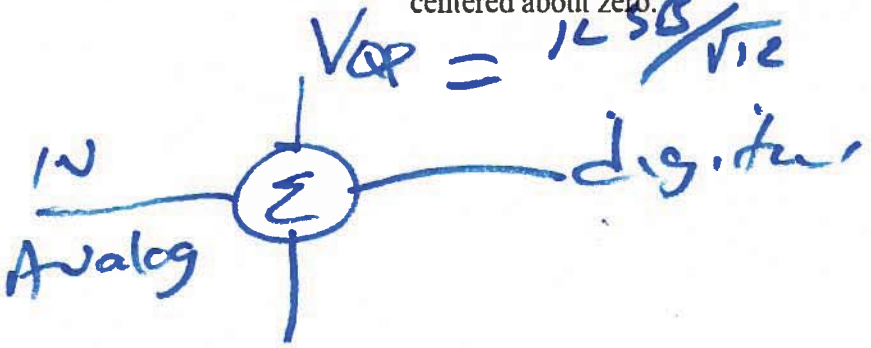


Figure 28.20 (a) Transfer curve for an ideal 3-bit ADC with (b) quantization error centered about zero.



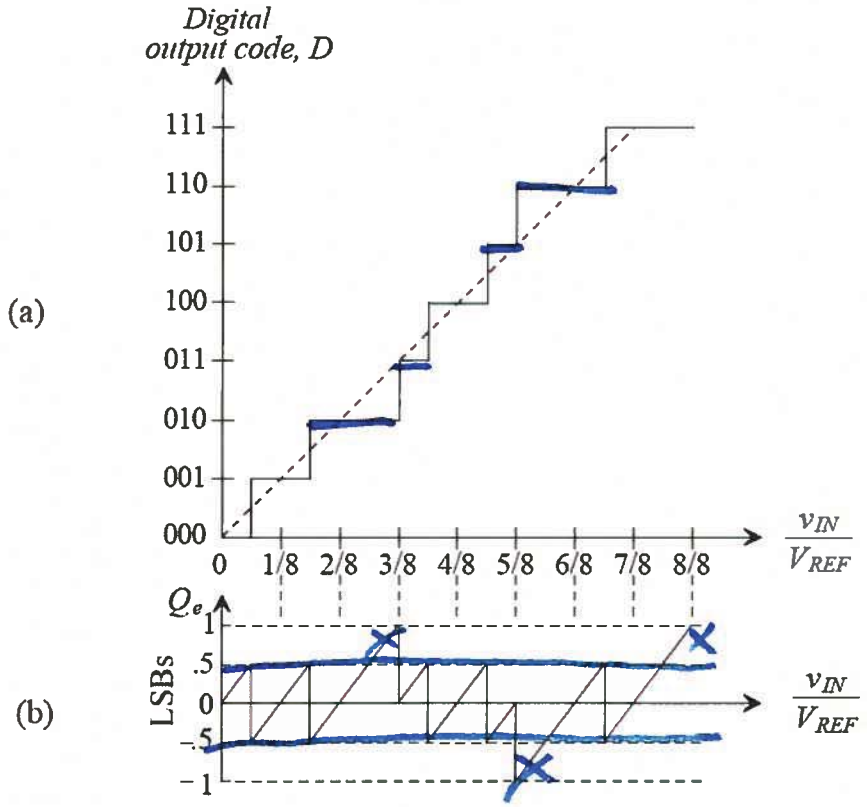


Figure 28.21 (a) Transfer curve for a nonideal 3-bit ADC used in Ex. 28.4 with (b) quantization error illustrating differential nonlinearity.

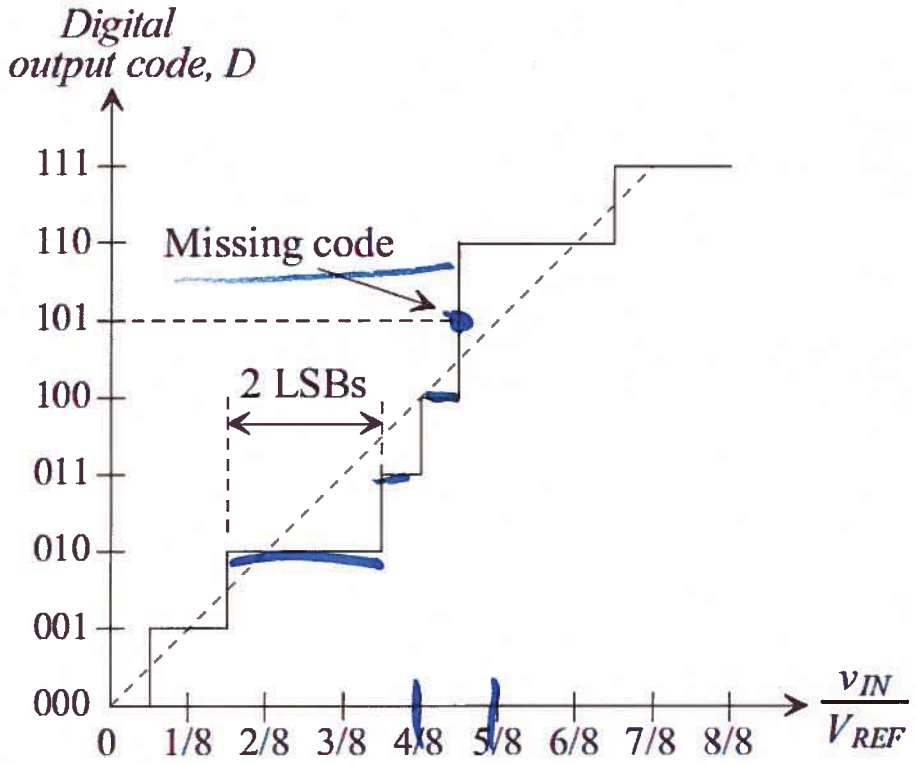


Figure 28.22 Transfer curve for a nonideal 3-bit ADC with a missing code.

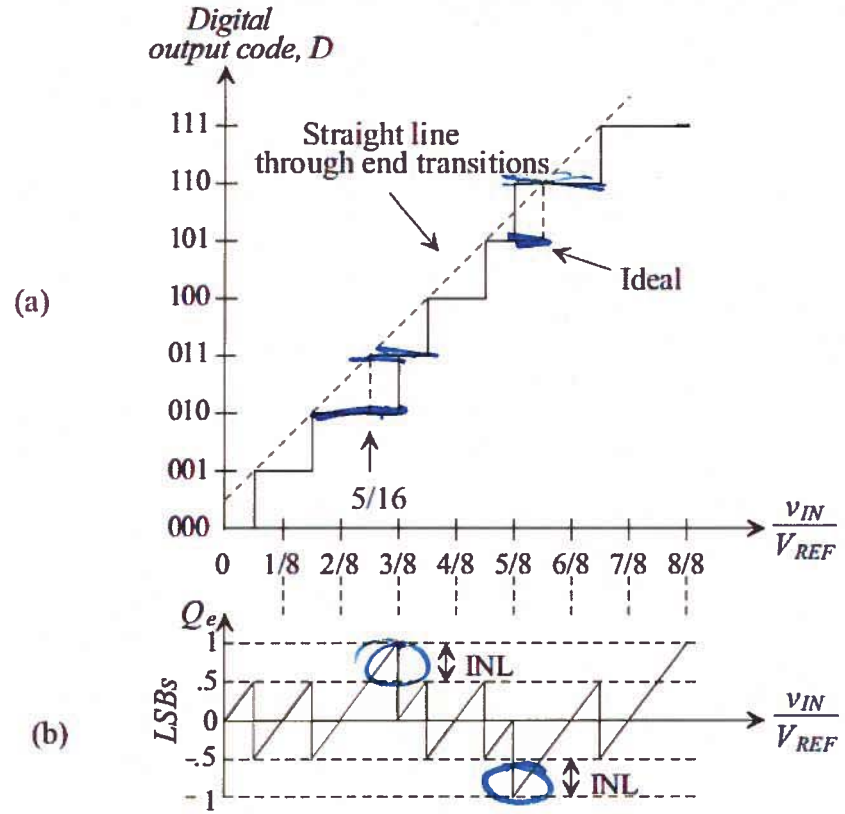


Figure 28.23 (a) Transfer curve of a nonideal 3-bit ADC and (b) its quantization error illustrating INL.

23)

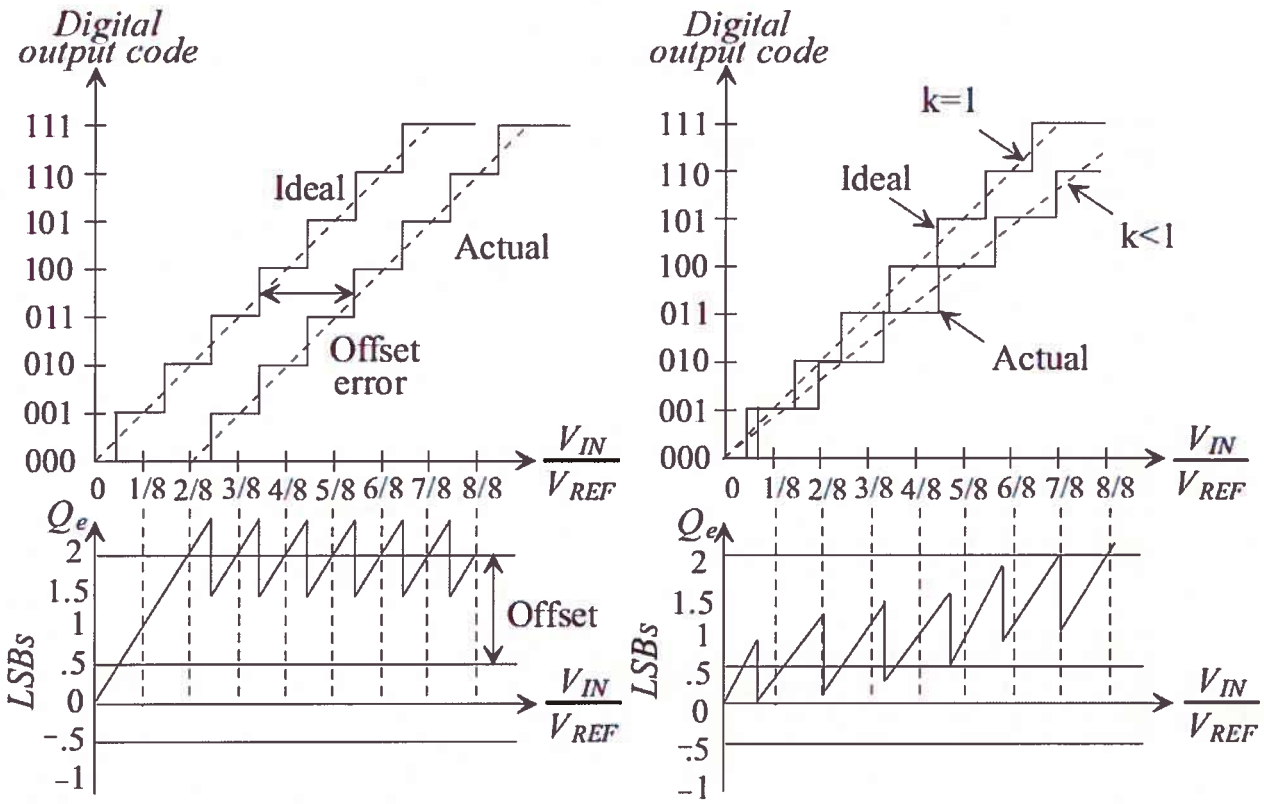


Figure 28.24 Transfer curve illustrating (a) offset error and (b) gain error.

24)

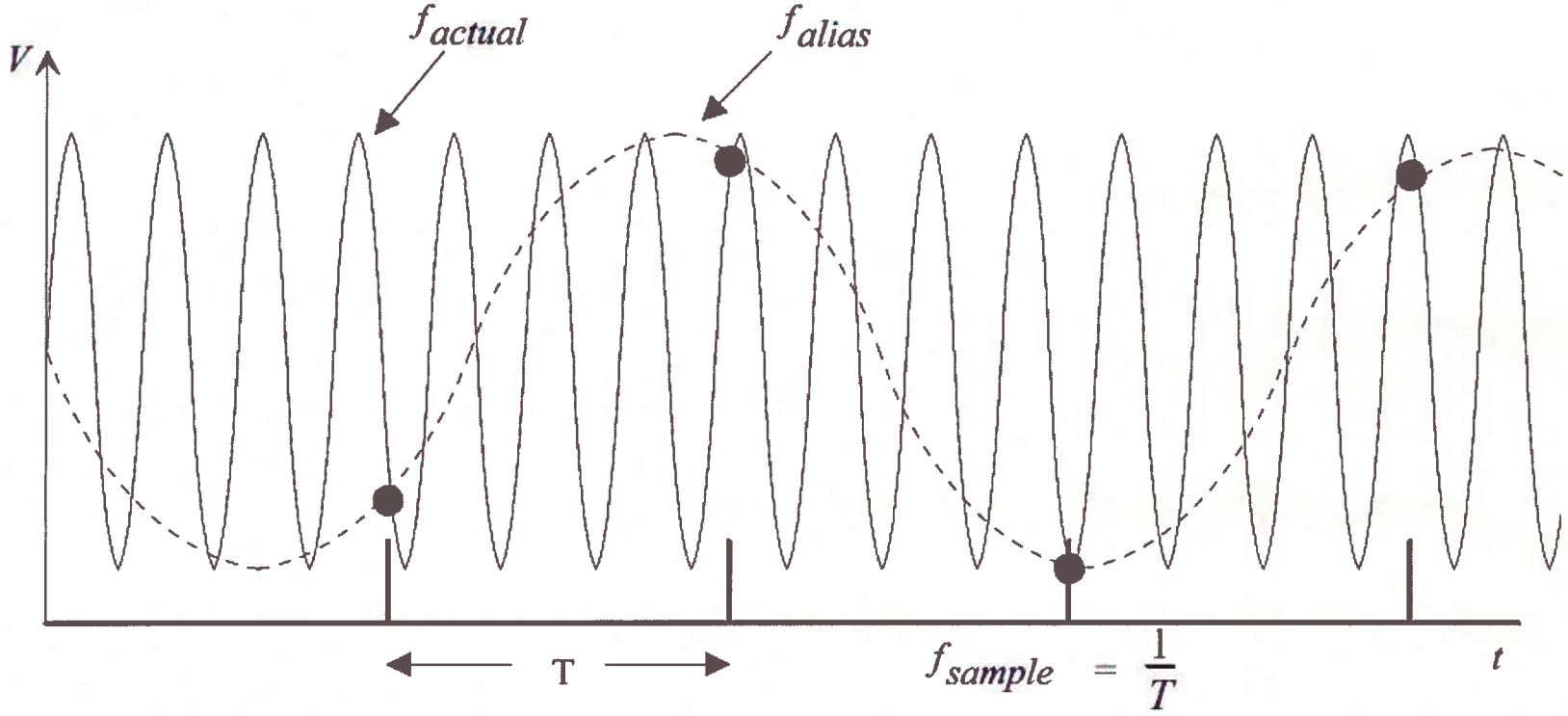


Figure 28.25 Aliasing caused by undersampling.

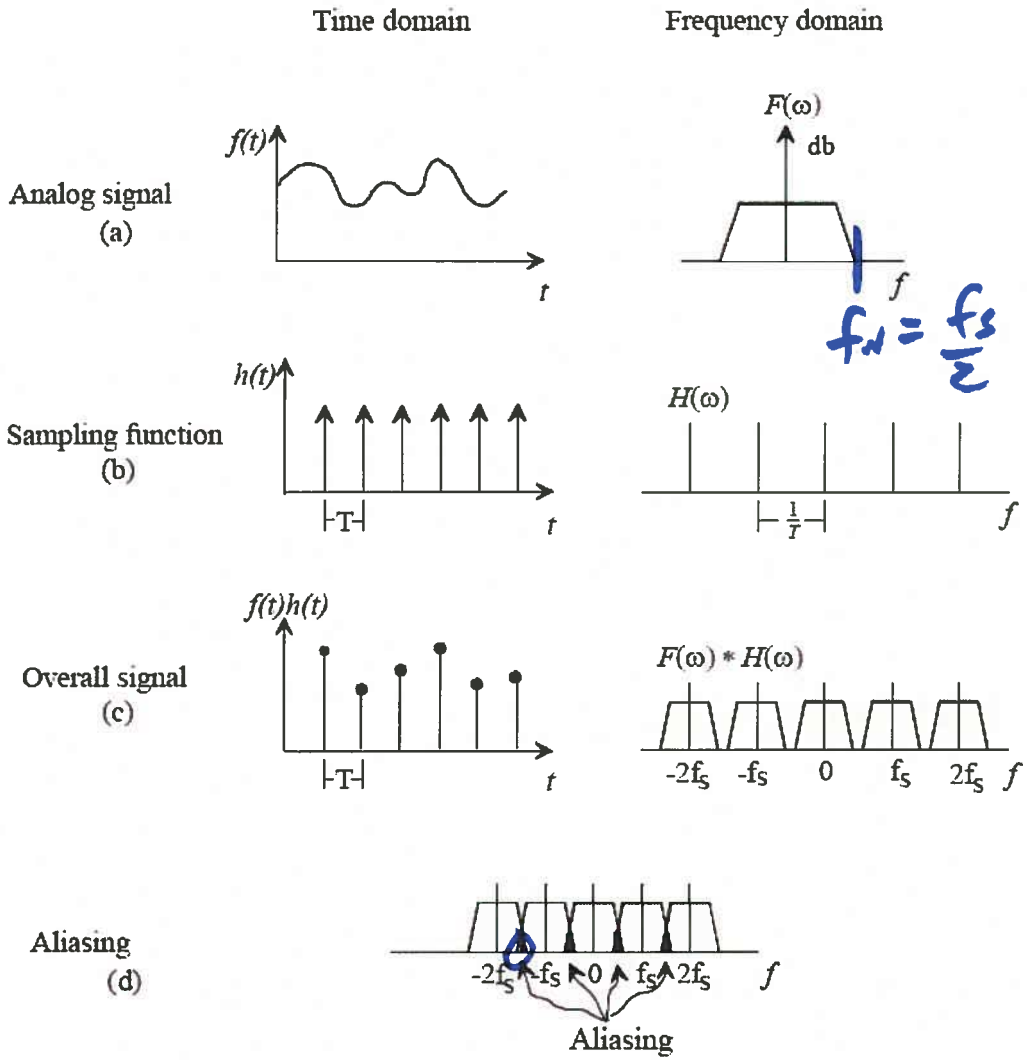


Figure 28.26 Illustration of aliasing in the time and frequency domain. (a) The analog signal; (b) the sampling function; (c) the overall signal; and (d) aliasing in the frequency domain.

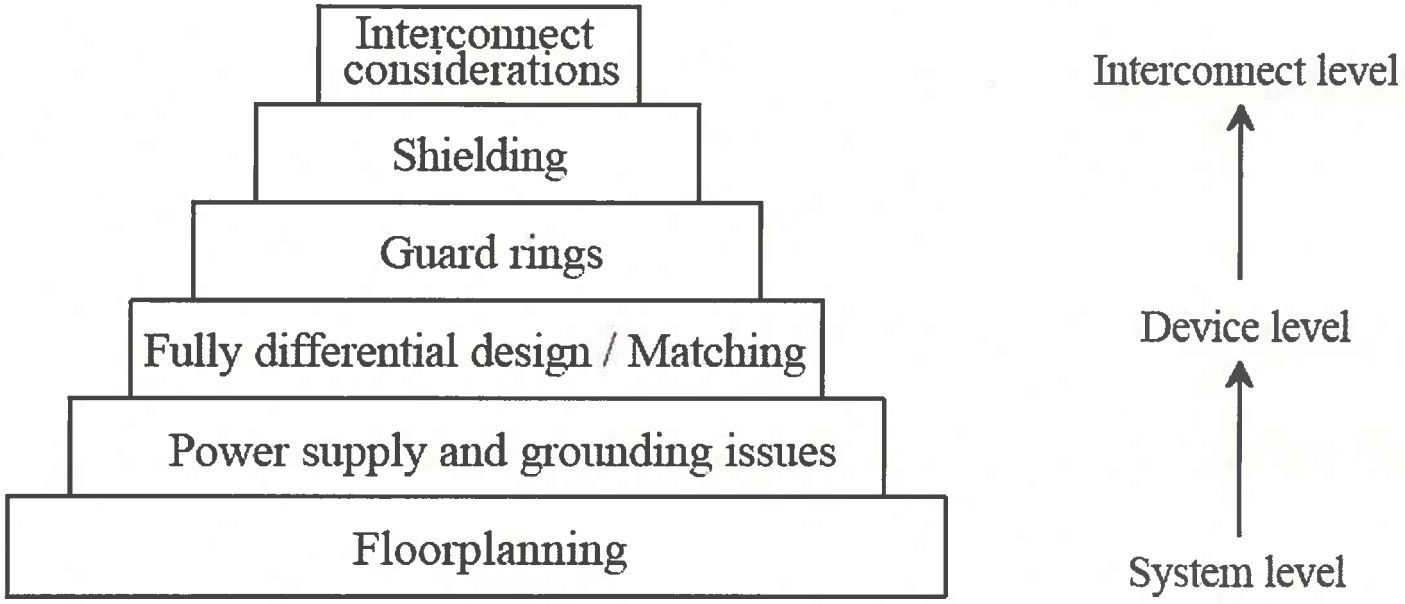


Figure 28.27 Mixed-signal layout strategy.

22
Analog

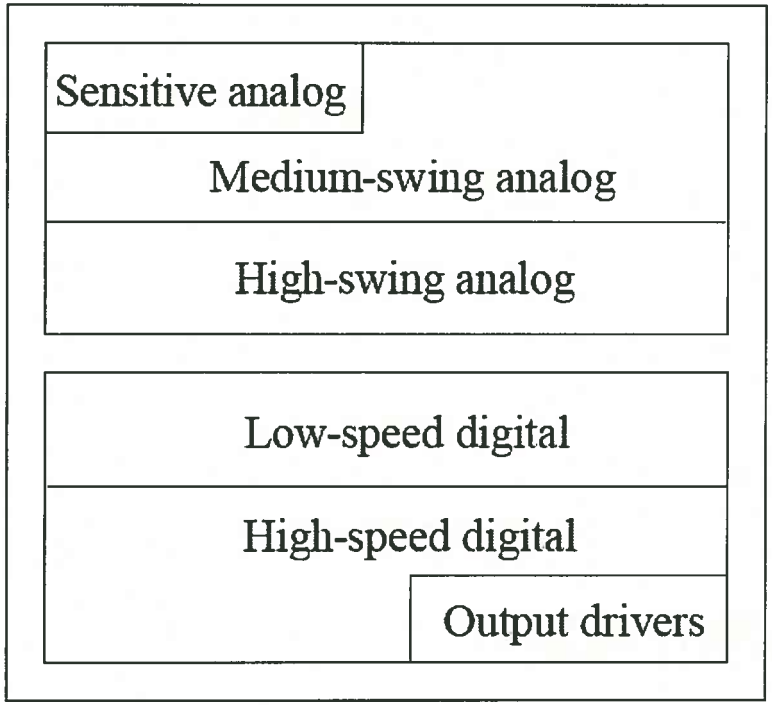


Figure 28.28 Example of a mixed-signal floorplan [1].

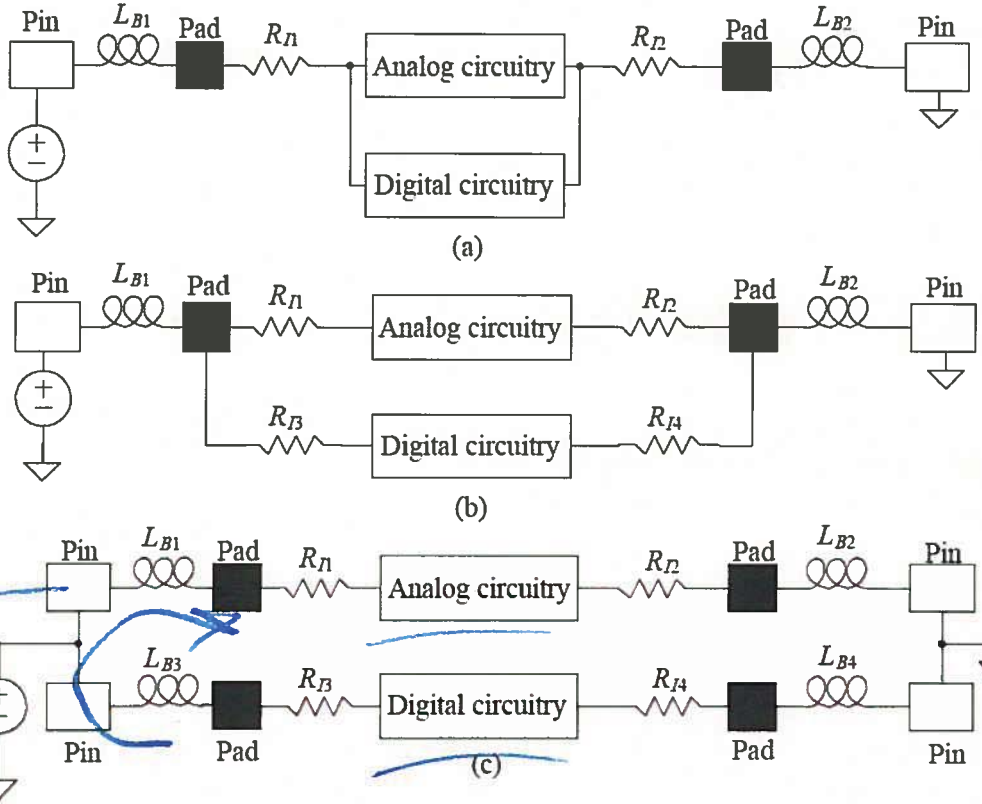


Figure 28.29 Power and ground connection examples. (a) poor noise immunity and (b) better noise immunity, and (c) using separate power and ground pins to achieve even better immunity.