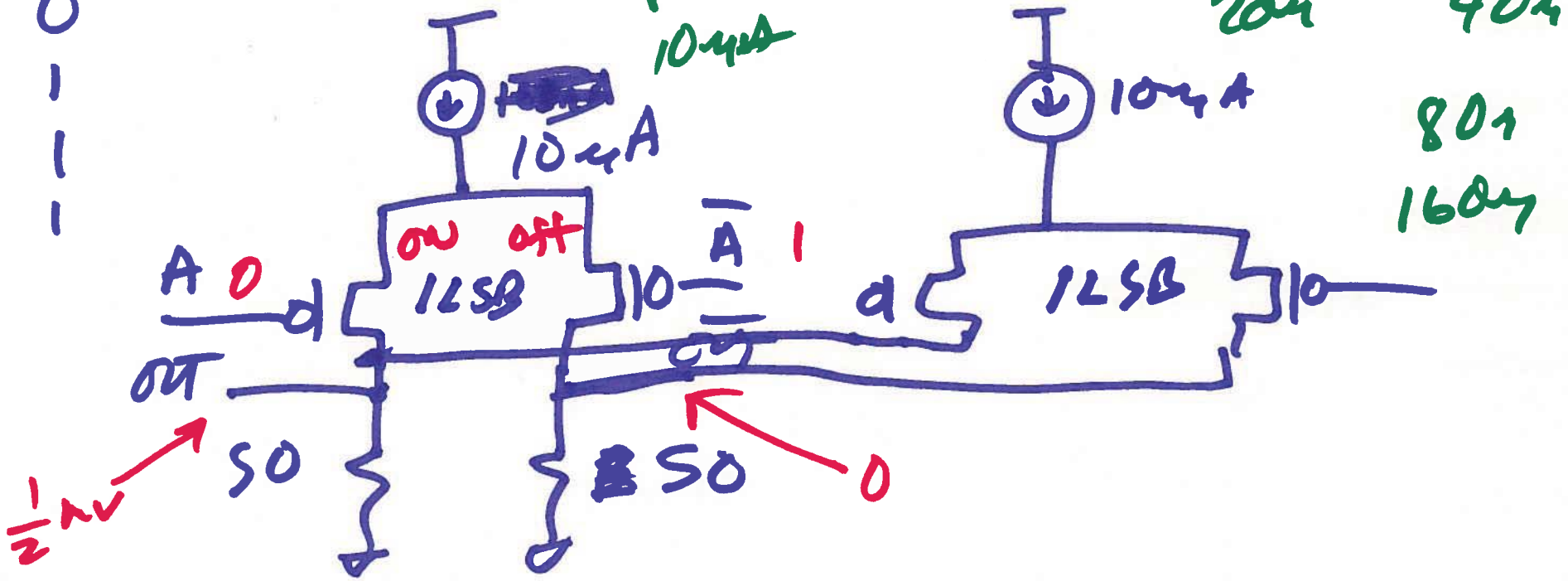
ECG 720
Advanced Analog IC Design
Spring 2016
April 12, 2016



1)

Decimal	Binary	Thermometer	Gray	Two's Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

Figure 29.1 Comparison of digital input codes.

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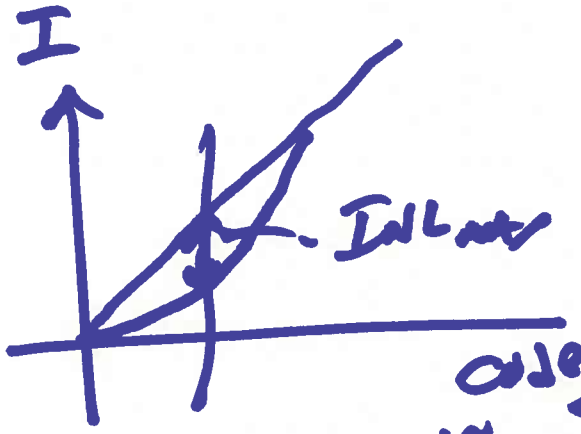
Each current source is

$$I + \Delta I_k \qquad k = 1, 2, 3 \ldots 2^N - 1$$

$$\sum_{k=1}^{2^N-1} \Delta I_k = 0$$

$$I_{out} = \sum_{k=1}^{2^N-1} (I + \Delta I_k) = I \cdot 2^{N-1} + 2^{N-1} \cdot \Delta I_{max}$$

$$= 2^{N-1} \Delta I_{LSB\,max}$$



$$\Delta I_{LSB\,max} = \frac{I}{2^N}$$

$$I_{LSB} = \frac{1}{2} I_{SB} = \frac{I}{2^1}$$

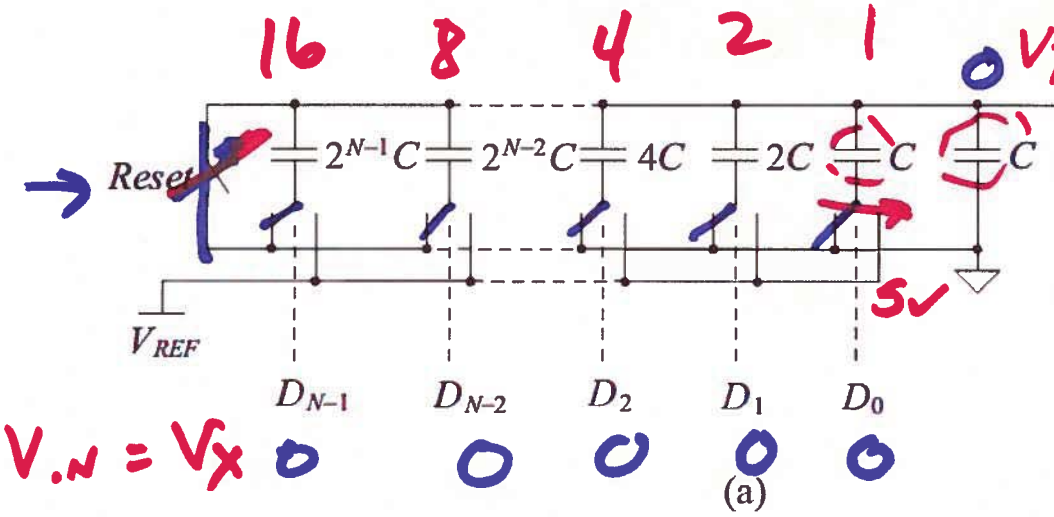
DNL

$$I_{OUT} - I_{OUT(N-1)} = I_K + |\Delta I_{max}|_{DNL}$$

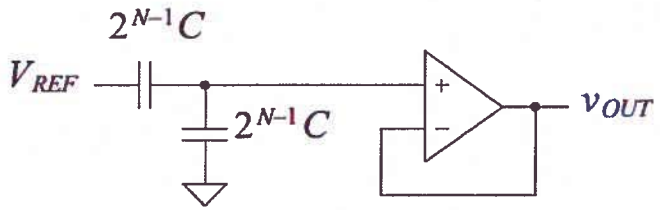
$$DNL_{MAX} = I_K + |\Delta I_{max}|_{DNL} - I_K$$

$$\Delta I_{MAX,DNL} = \frac{1}{2} LSB = \boxed{\frac{I}{2}}$$

DNL_{max}



(a)



(b)

Figure 29.12 (a) A charge-scaling DAC, (b) the equivalent circuit with the MSB = 1, and all other bits set to zero.

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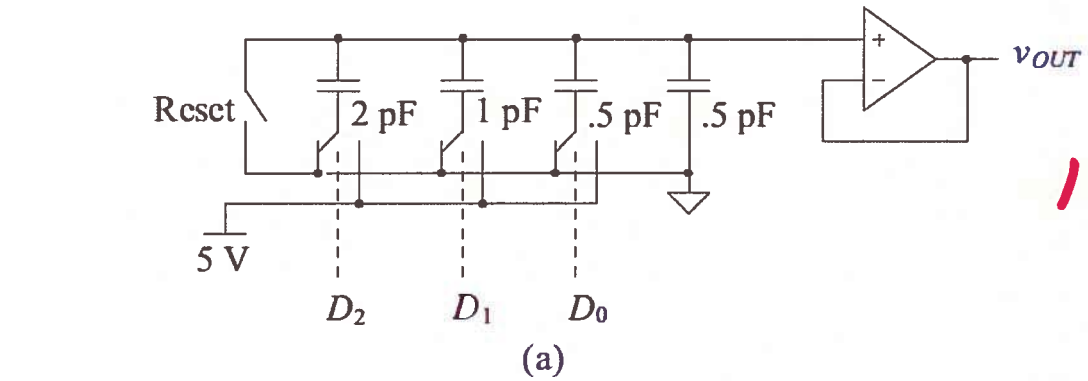

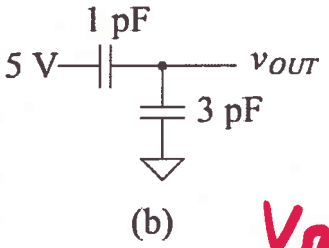

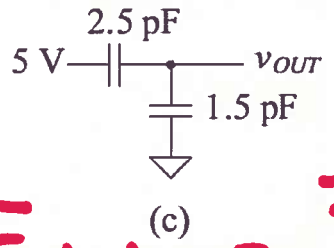

Figure 29.13 (a) A 3-bit charge-scaling DAC used in Ex. 29.6 and the equivalent circuits inputs equal to (b) 010 (c) 101.

N = 3

1LSB = 5/8

$V_{out} = 5 \cdot \frac{.5}{.5+.5+1+2} = 5 \cdot \frac{.5}{4}$

$= \frac{5}{8}$

1LSB

b)

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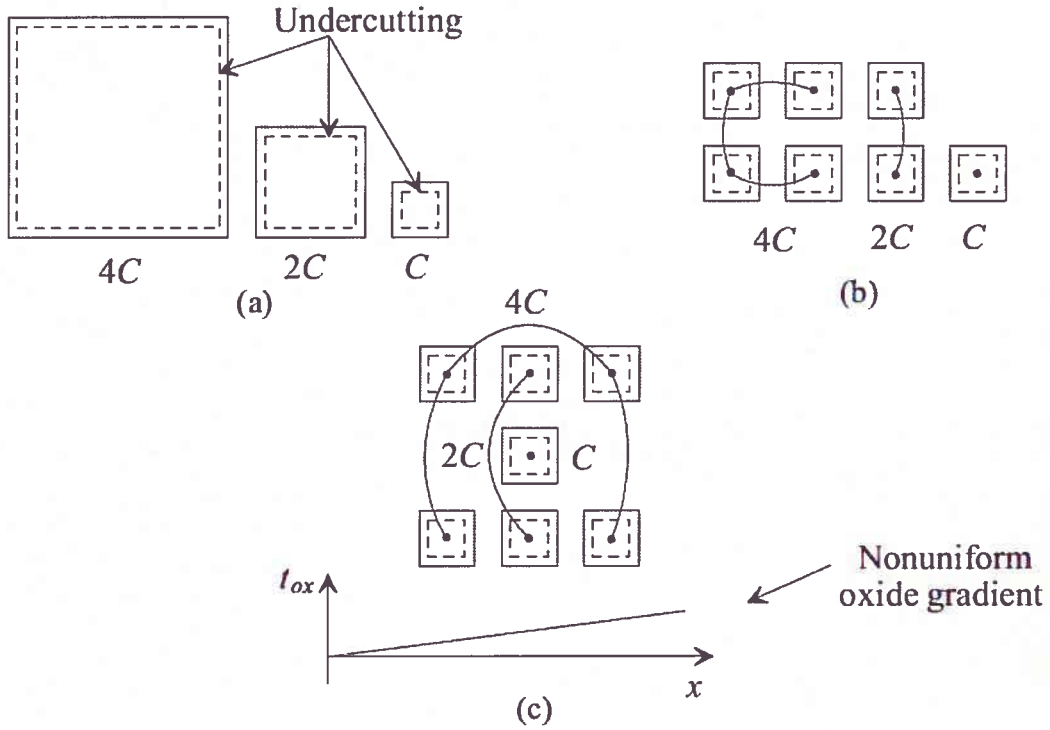

Figure 29.14 Layout of a binary-weighted capacitor array using (a) single capacitors (b) unit capacitors to minimize undercutting effect, and (c) common-centroid to minimize oxide gradients.

Matching

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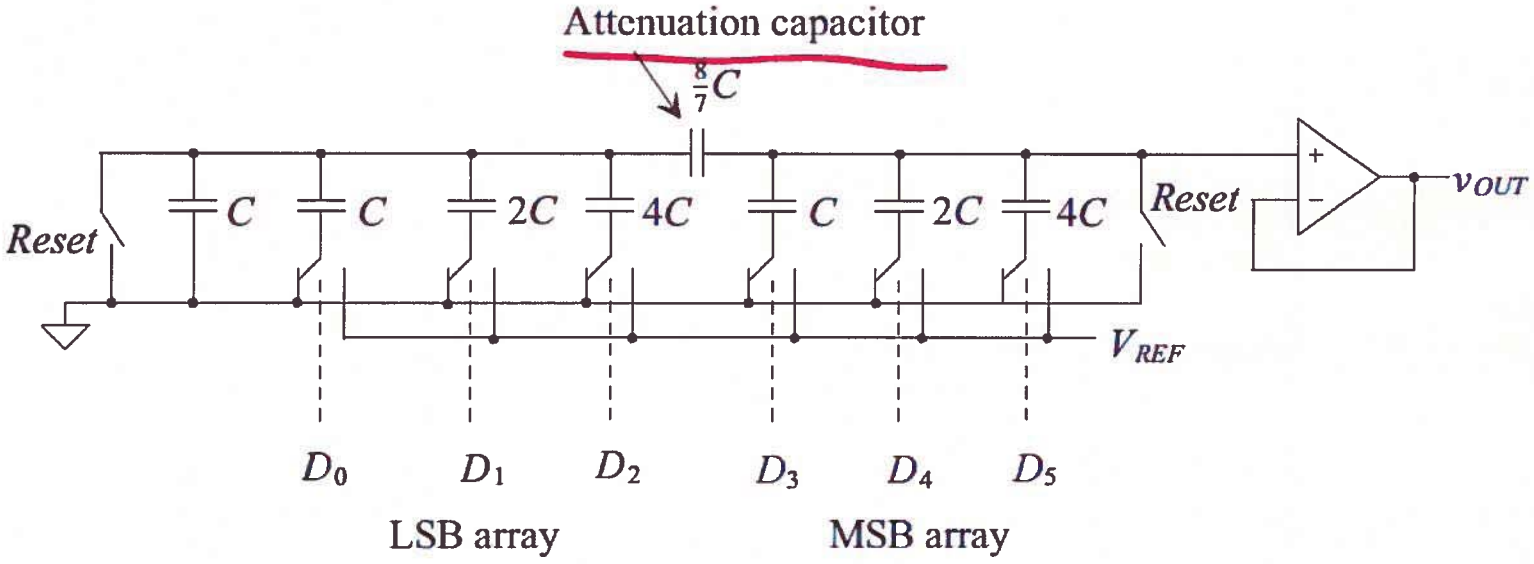

Figure 29.15 A charge-scaling DAC using a split array.

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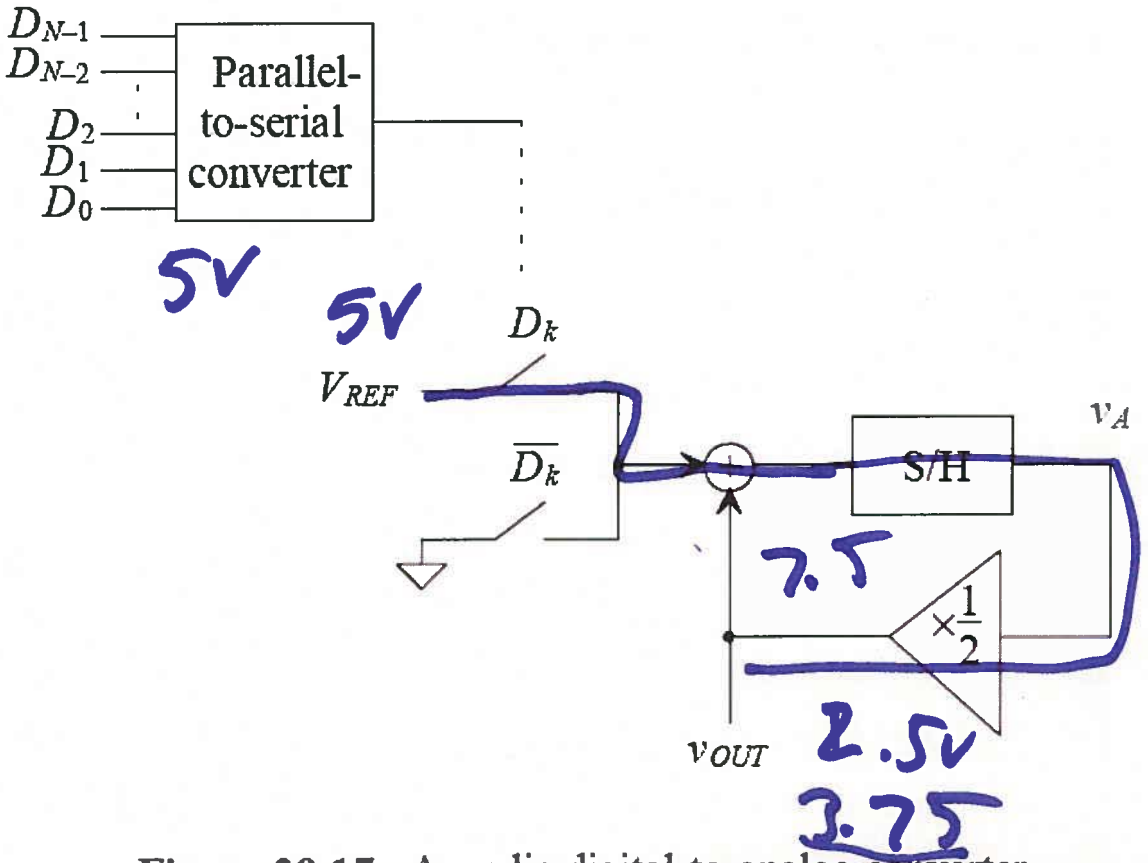

Figure 29.17 A cyclic digital-to-analog converter.

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9)

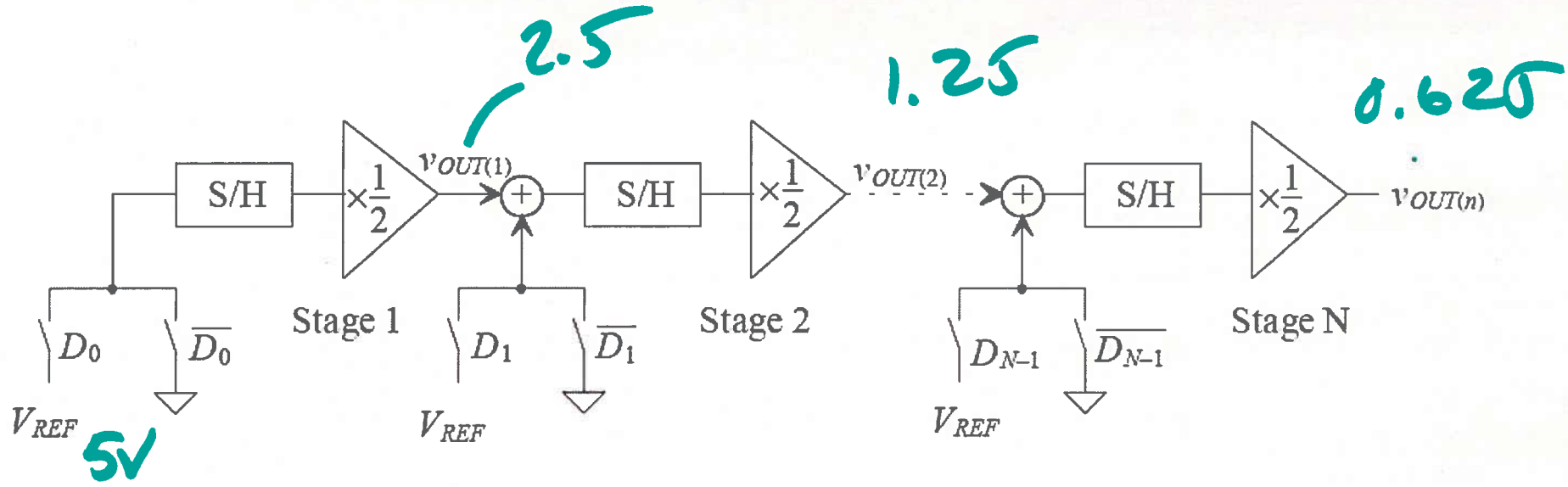
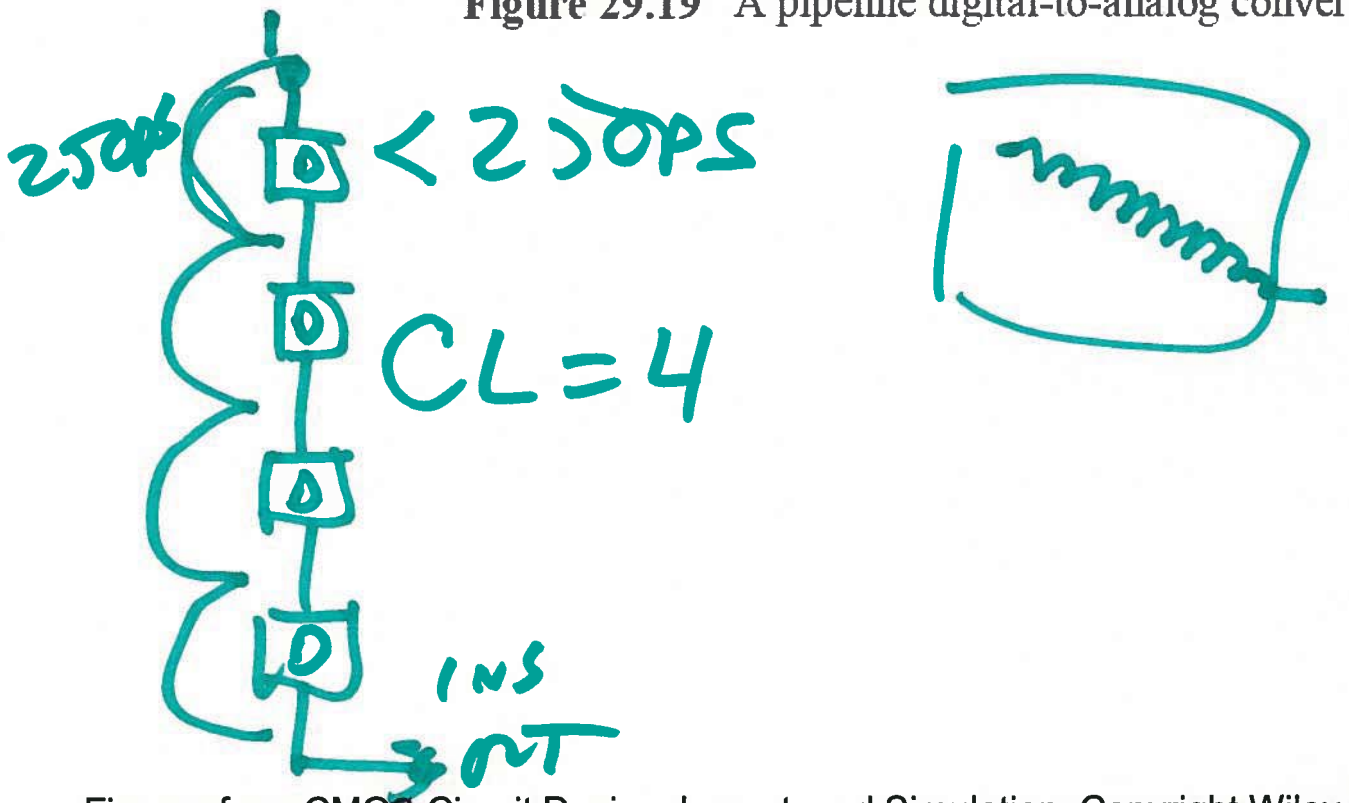


Figure 29.19 A pipeline digital-to-analog converter.



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10)

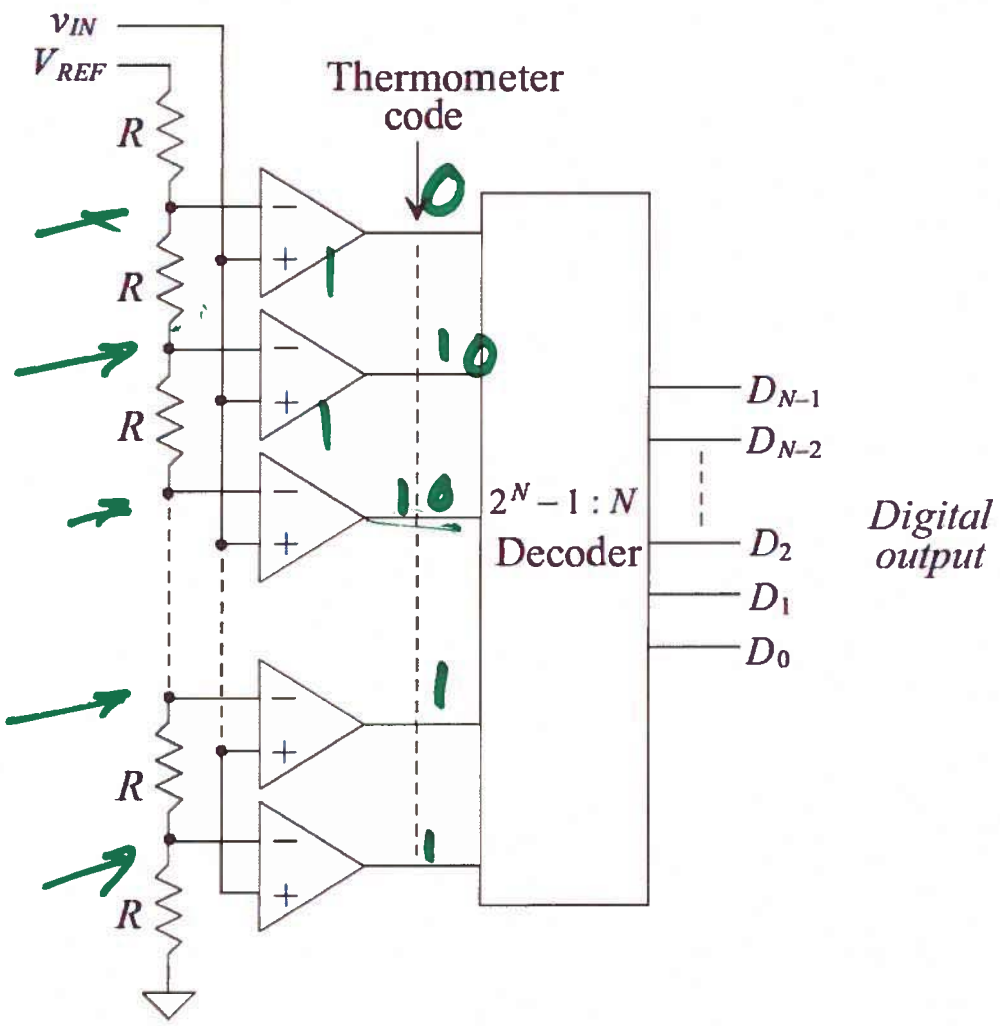

Figure 29.21 Block diagram of a Flash ADC.

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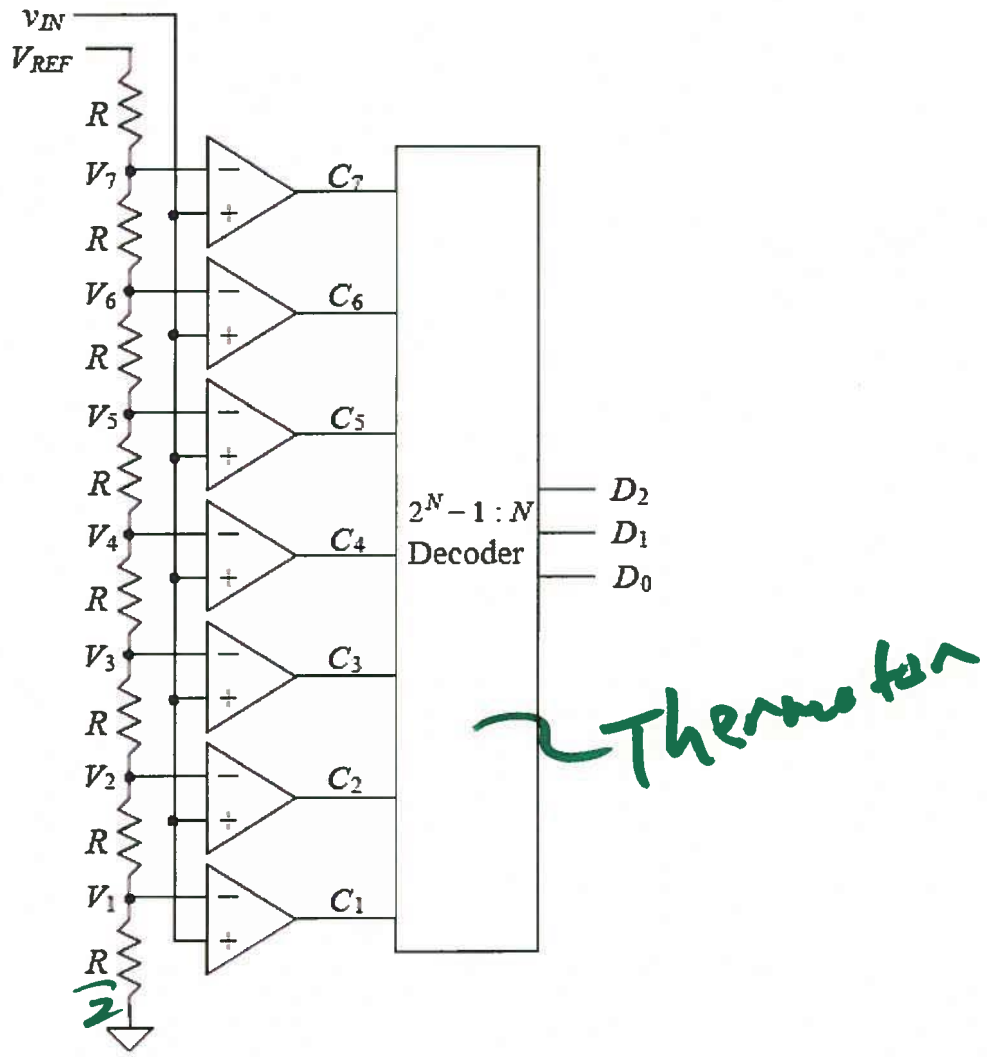

Figure 29.22 Three-bit Flash A/D converter to be used in Ex. 29.10.

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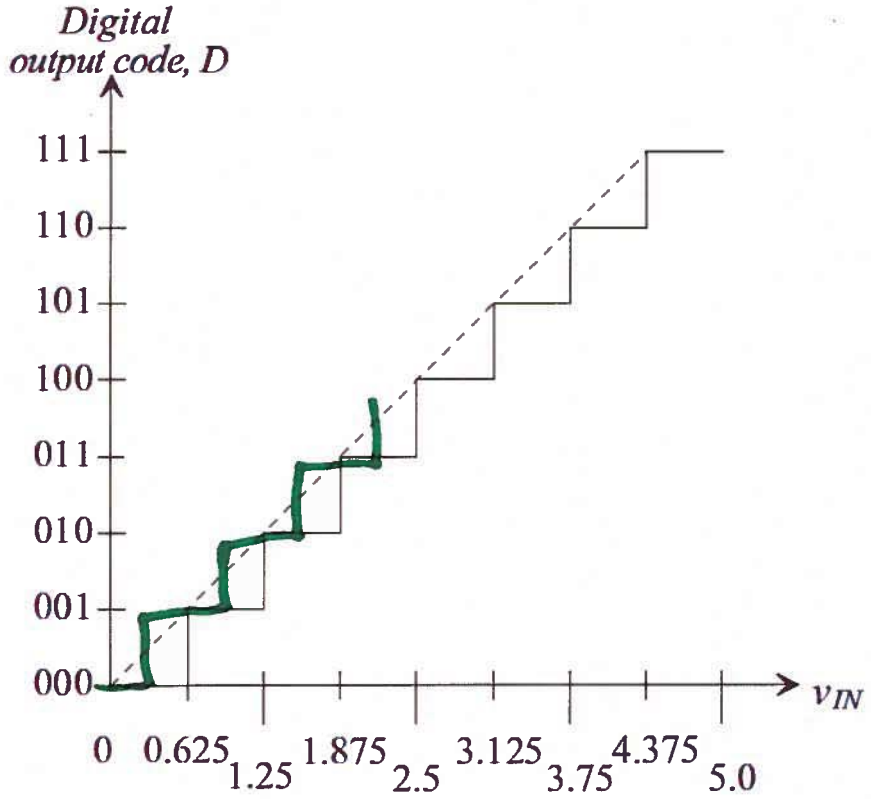

Figure 29.23 Transfer curve for the 3-bit Flash converter in Example 29.10.

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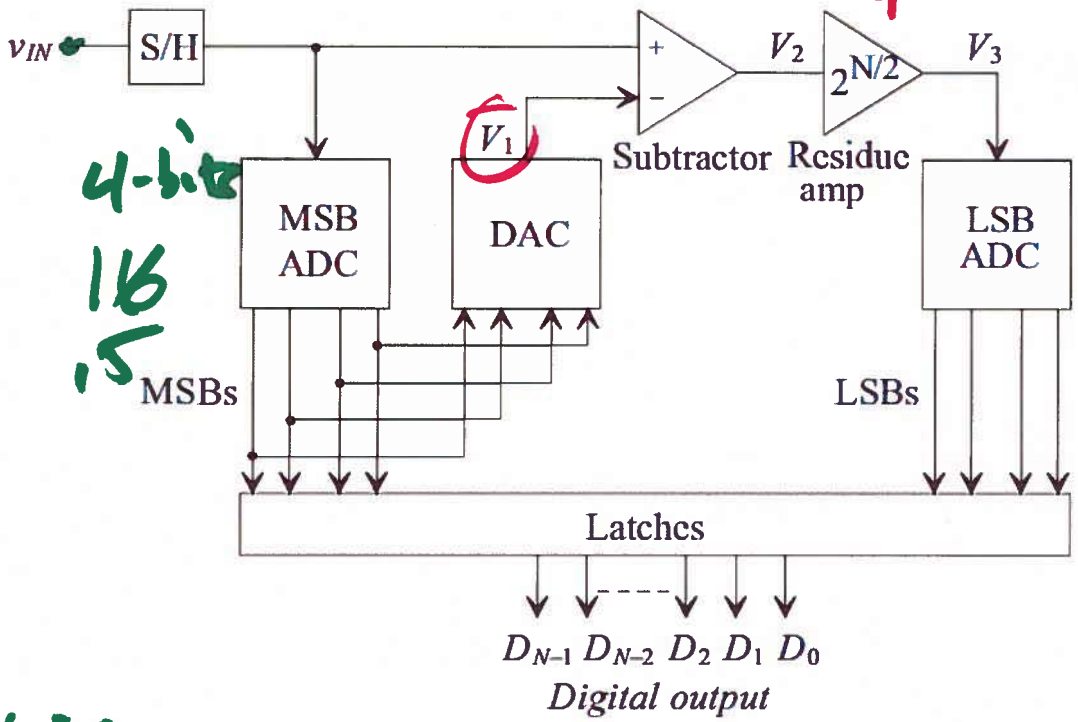

Figure 29.26 Block diagram of a two-step Flash ADC.

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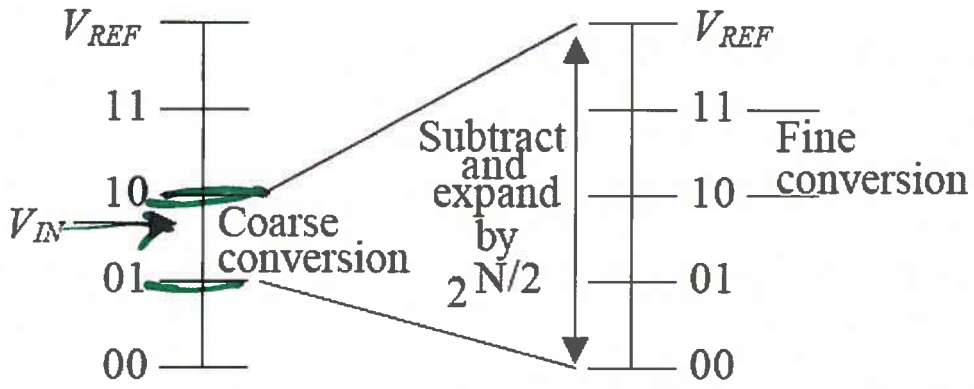

Figure 29.27 Coarse and fine conversions using a two-step ADC.

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V_{IN}	D_3D_2 (MSBs)	V_1	V_2	V_3	D_1D_0 (LSBs)
2	00	0	2	8	10
4	01	4	0	0	00
9	10	8	1	4	01
15	11	12	3	12	11

Figure 29.28 Output for the Flash ADC used in Ex. 29.12.

4-bit
2-step
flash ADC

0010

VDD=16

N=2

$2^{N/2}$

$= 4$

0 ⇒ 4 00

4 ⇒ 8 01

8 ⇒ 12 10

12 ⇒ 16 11

VREF=16

LSB =

$\frac{16}{2^4} = 1V$

0010

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What A_{OL} do I need for N-bit resolution?

$N = 8$

$$A_{OL} \simeq \frac{2^{N+1}}{\beta \to \frac{1}{2}}$$

$A_{OL} > 2^{10}$

1024

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} = \frac{1}{\beta} - \Delta A$$

Assume we WANT $\frac{1}{2}$ LSB Accuracy

$$\Delta A = \frac{\frac{1}{\beta}}{2^{N+1}} = \frac{\frac{1}{\beta \cdot 2^N}}{2}$$

$$A_{CL} = \frac{1}{\beta}\left(1 - \frac{1}{2^{N+1}}\right)$$

$A_{CL} < \frac{1}{2}$ LSB