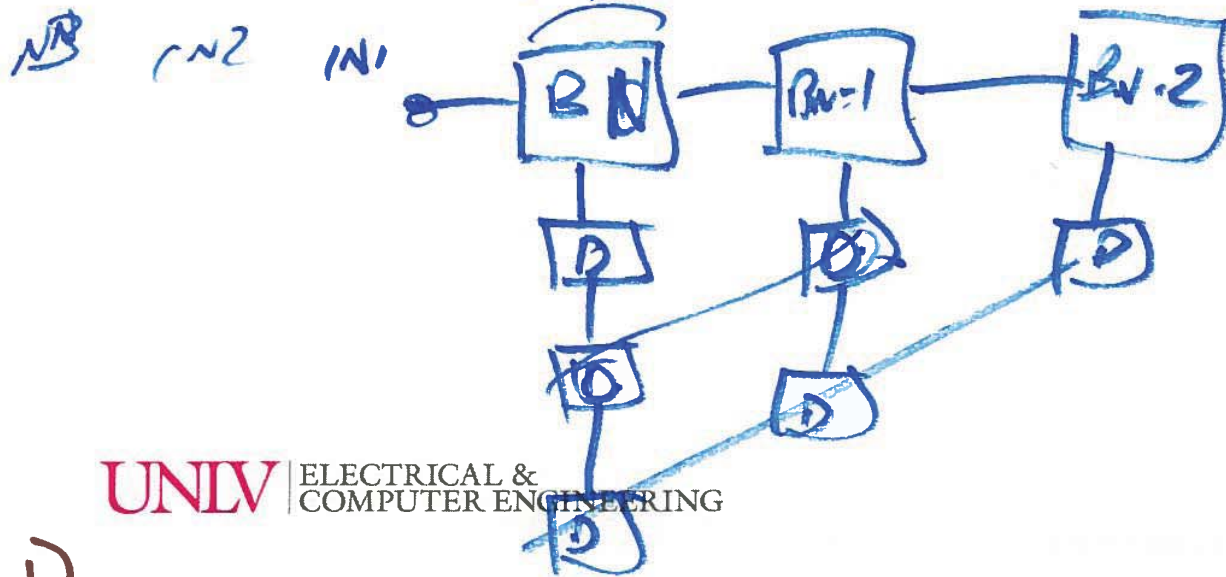


EEG 720 Advanced Analog IC Design

April 19, 2016

Lecture 24

Pipeline ADC



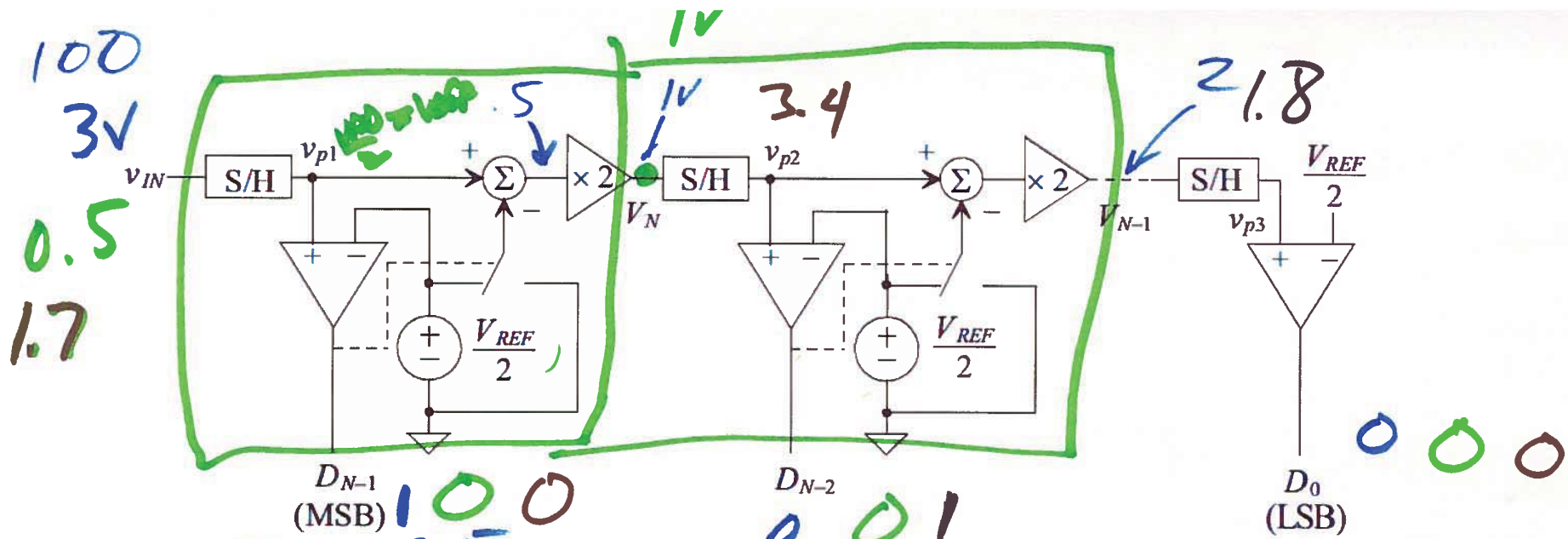
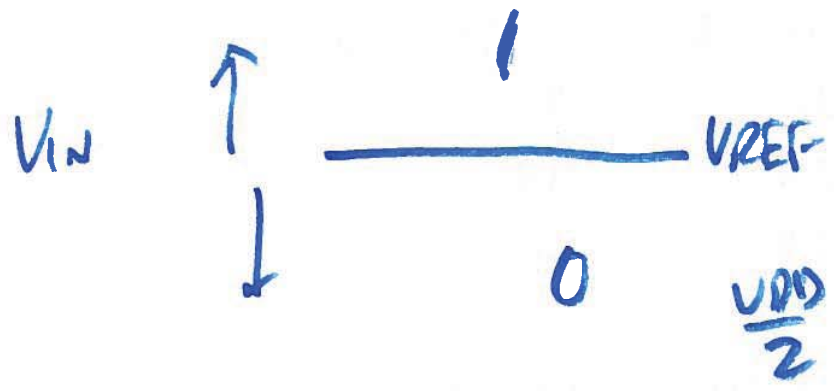


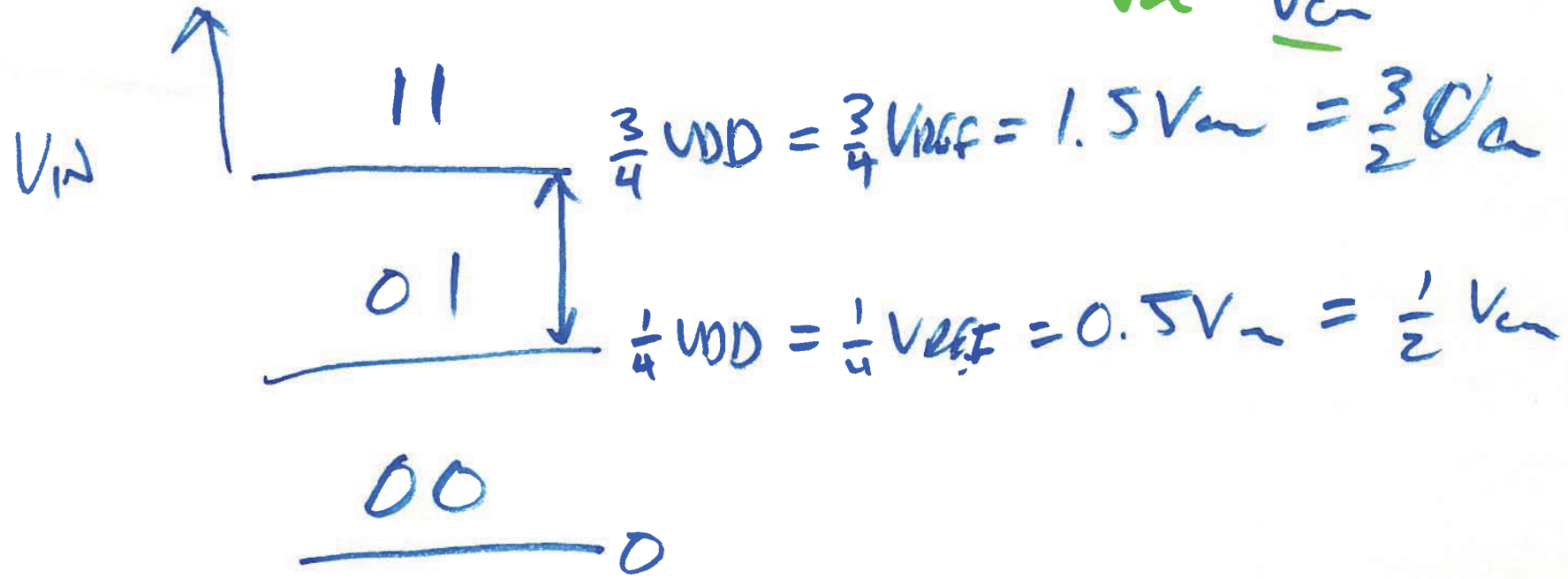
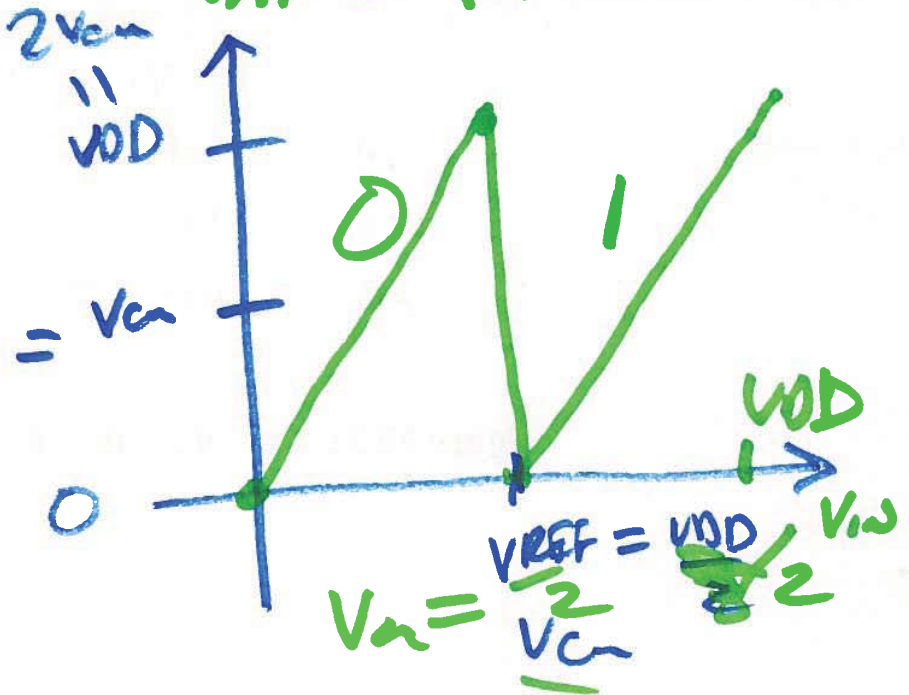
Figure 29.30 Block diagram of a pipeline ADC.

$5V = V_{REF}$
 $LSB = \frac{5}{8} = 0.625$

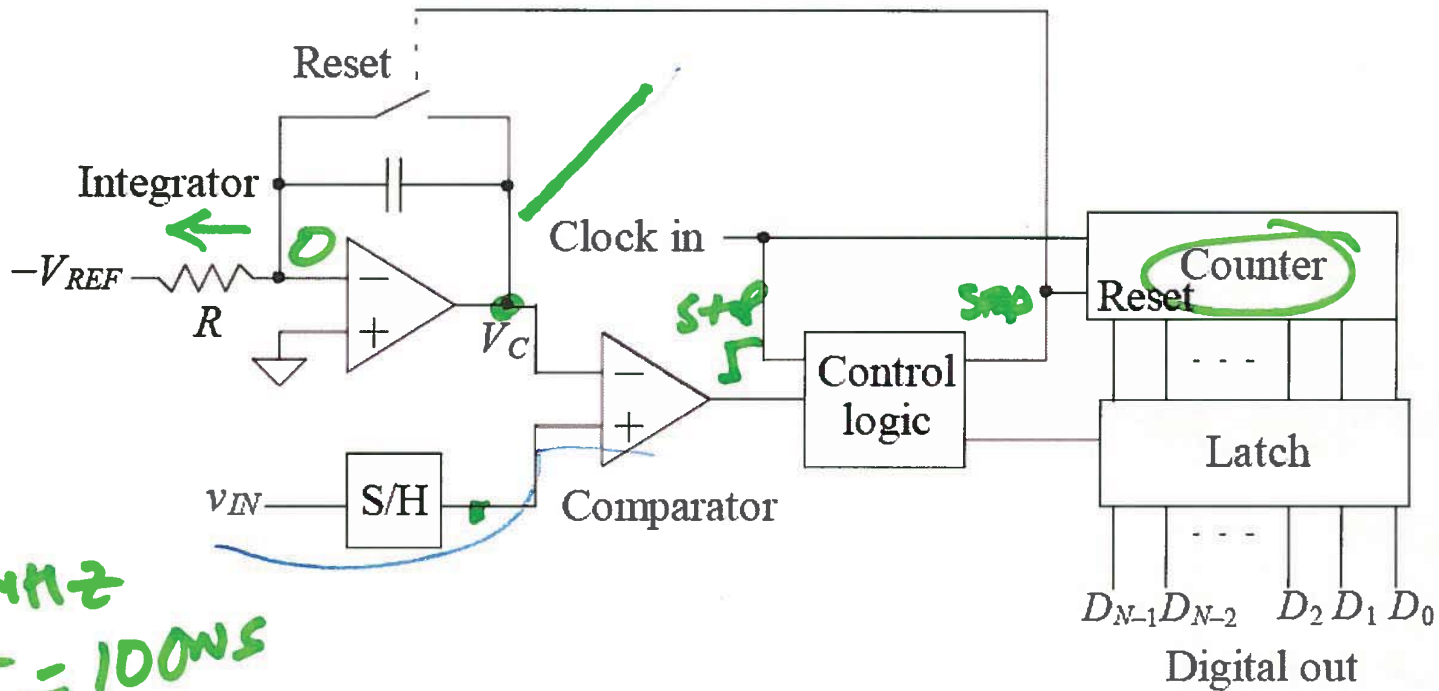
2.)



VNT of pipeline stage

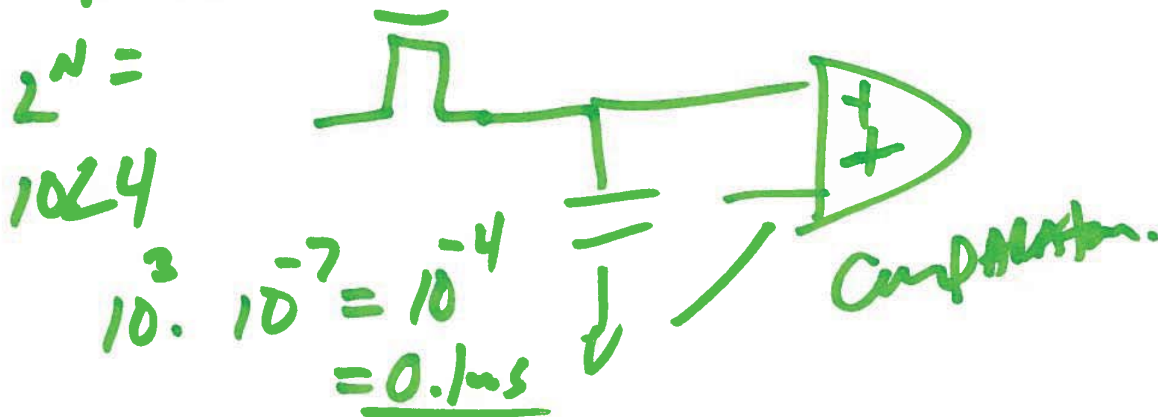


3)



10 MHz
 $T = 100\text{ns}$
 $N = 10\text{ bits}$

Figure 29.32 Block diagram of a single-slope ADC.



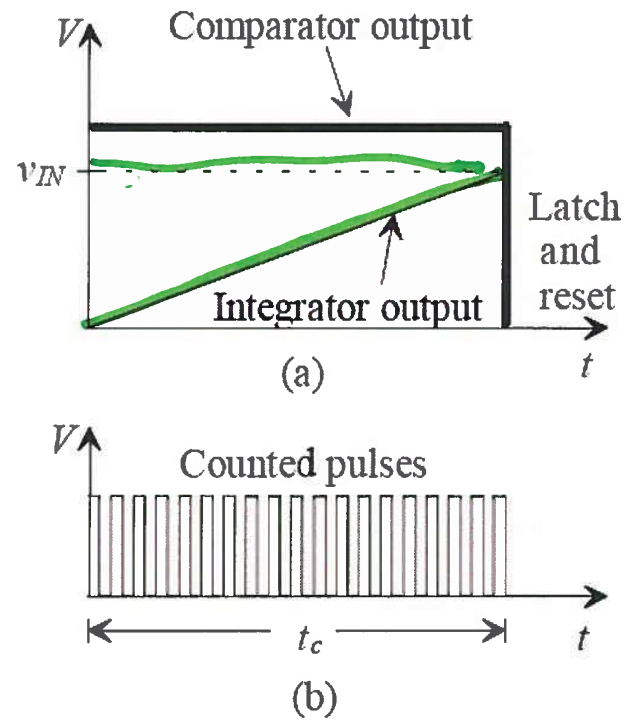


Figure 29.33 Single-slope ADC timing diagrams for (a) the comparator inputs and outputs and (b) the resulting counted pulses.

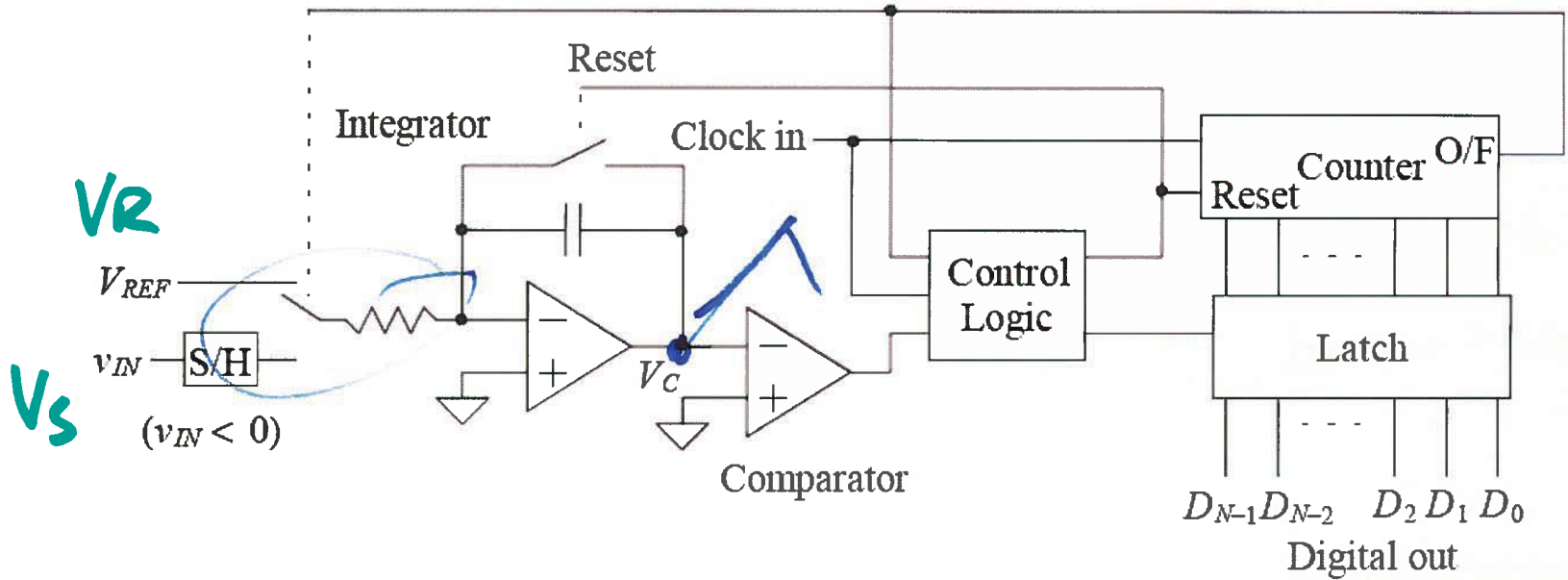
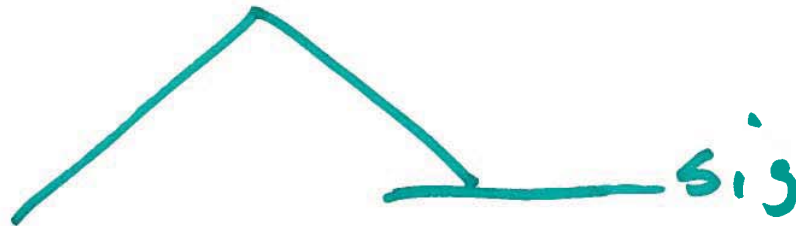


Figure 29.34 Block diagram of a dual-slope ADC.



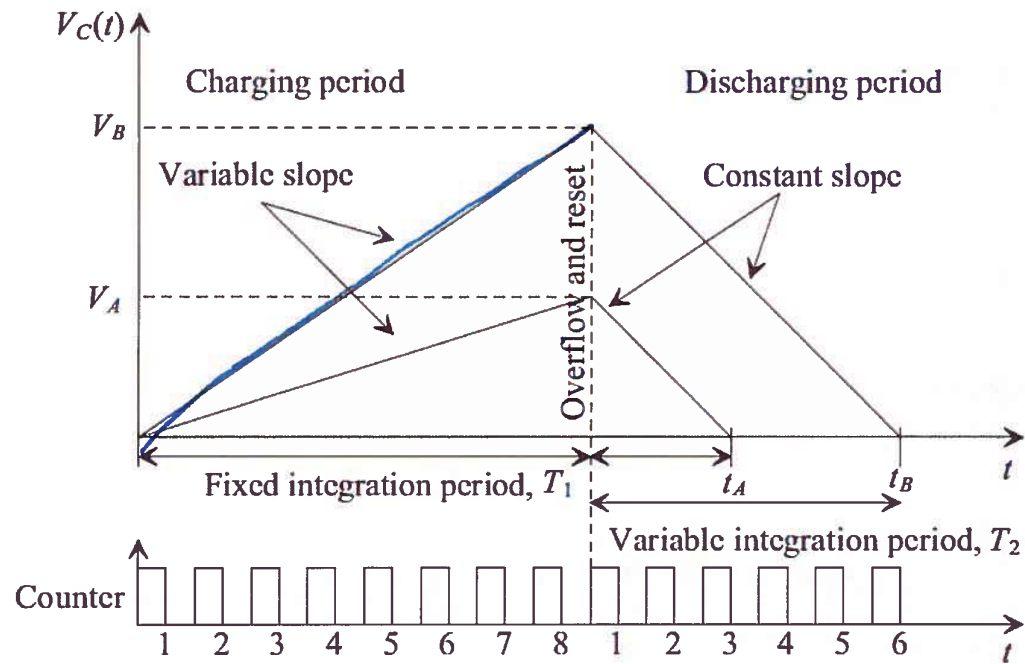


Figure 29.35 Integration periods and counter output for two separate samples of a 3-bit dual-slope ADC.



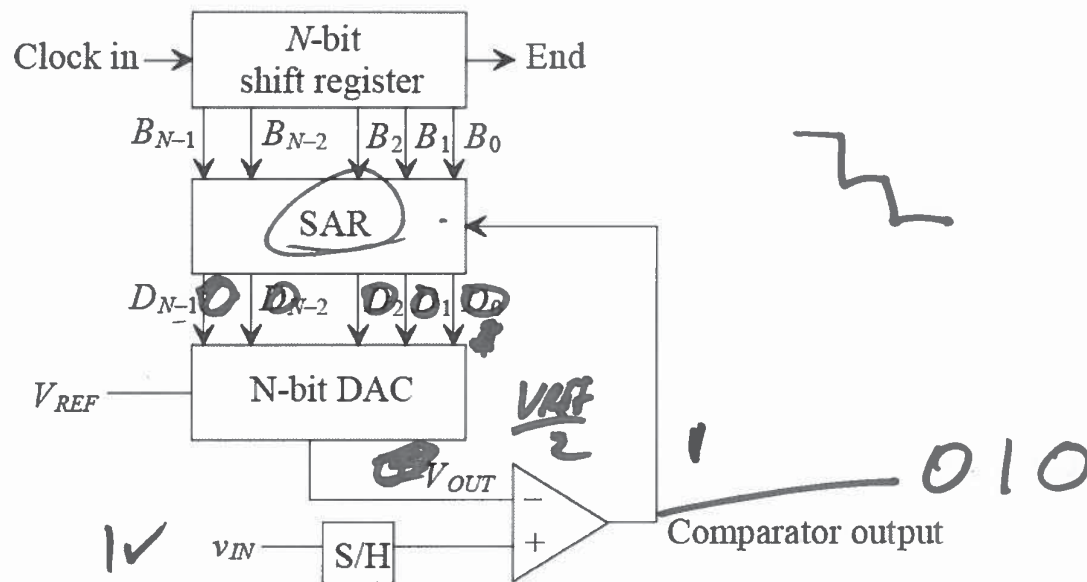


Figure 29.36 Block diagram of the successive approximation ADC.

1000 0000
 0100 0000
 0110 0000
 0101 0000

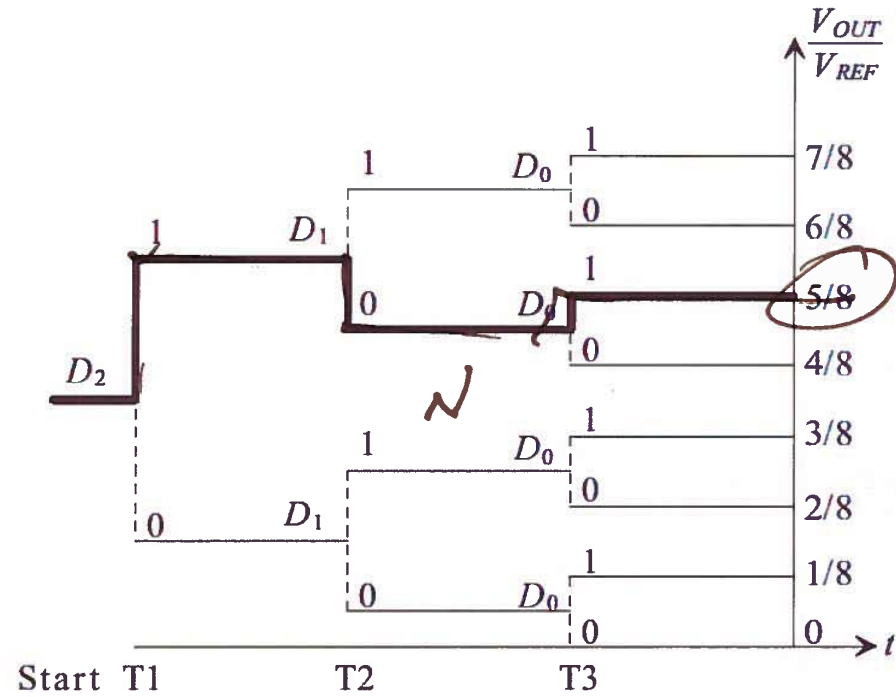


Figure 29.37 Binary search performed by a 3-bit successive approximation ADC for $D=101$.

a)

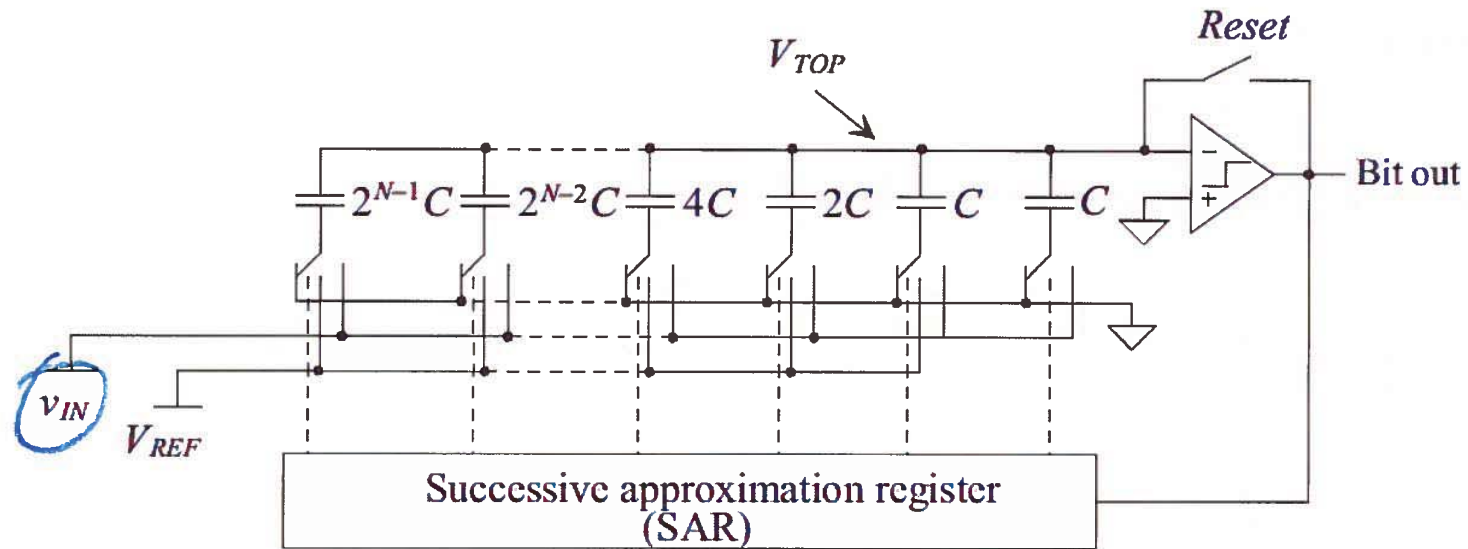


Figure 29.39 A charge redistribution ADC using a binary-weighted capacitor array DAC.

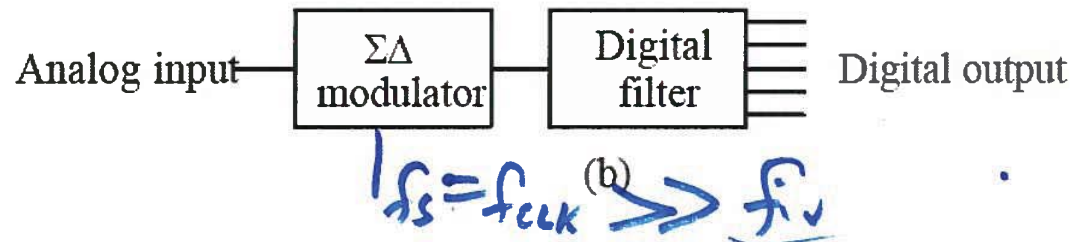
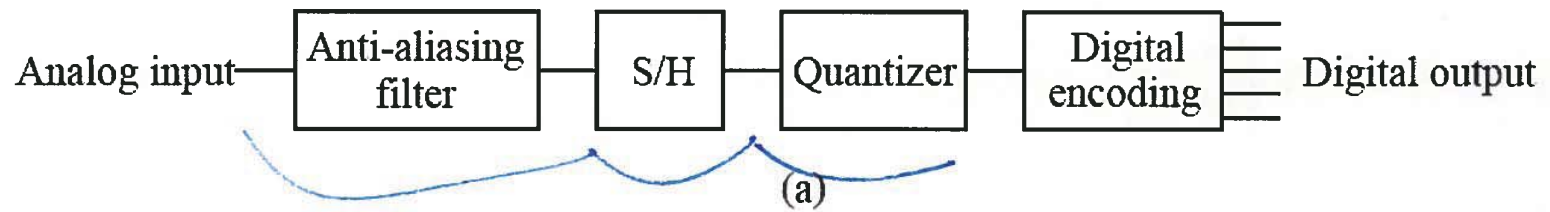
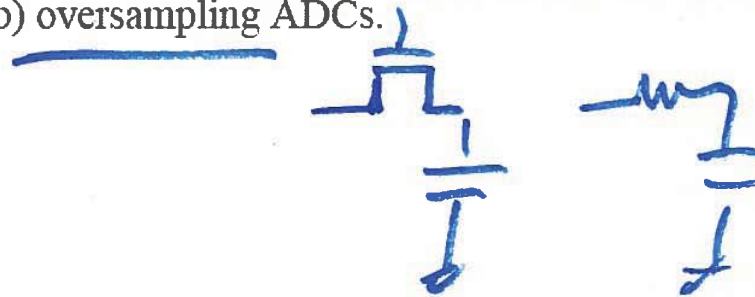
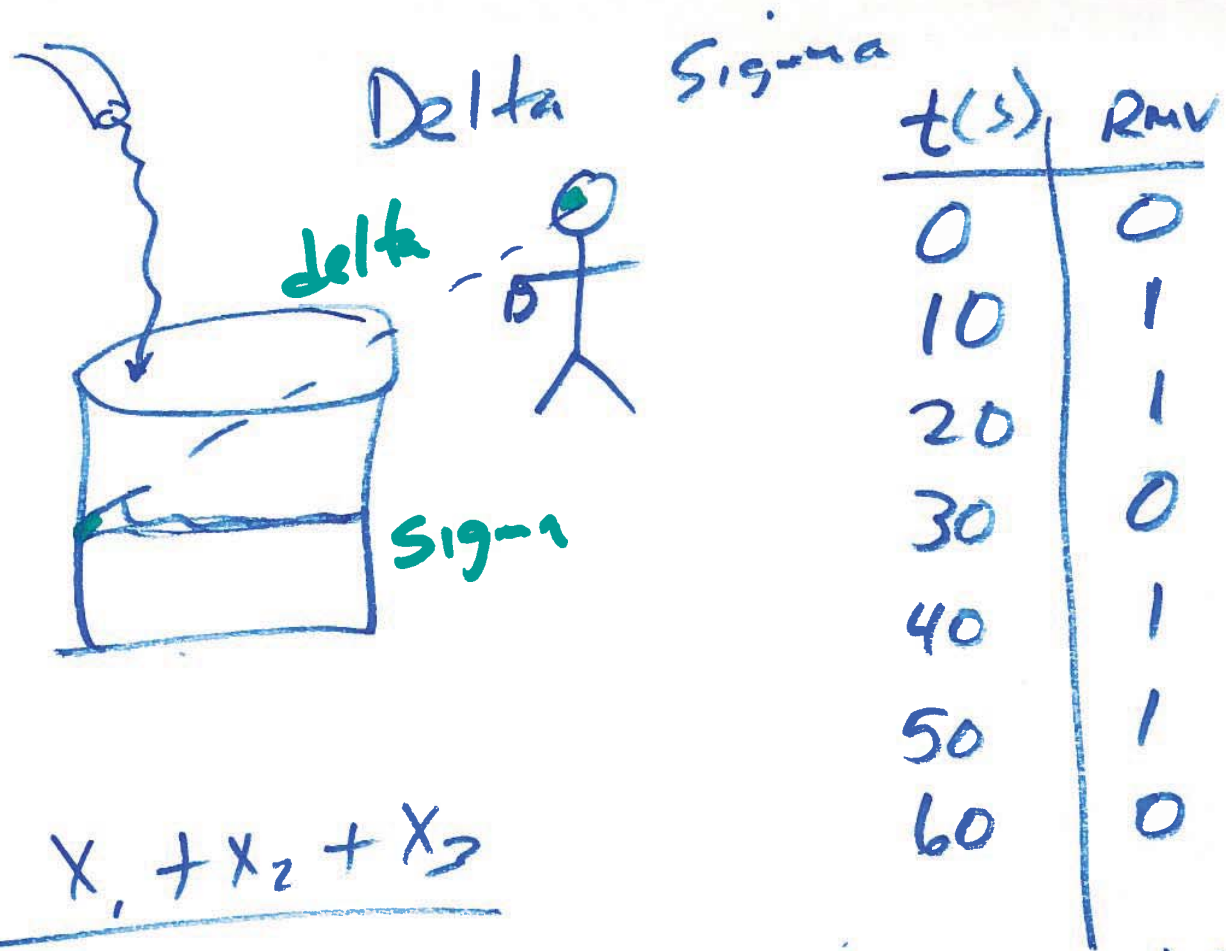


Figure 29.41 Typical block diagram for (a) Nyquist rate converters and (b) oversampling ADCs.





$\frac{2 \text{ cups}}{30 \text{ sec}} = \text{flow}$

$$\frac{X_1 + X_2 + X_3}{3}$$

$$1$$

$$\frac{X_2 + X_3 + X_4}{3}$$

$$2$$

digital filter

moving average filter

12)

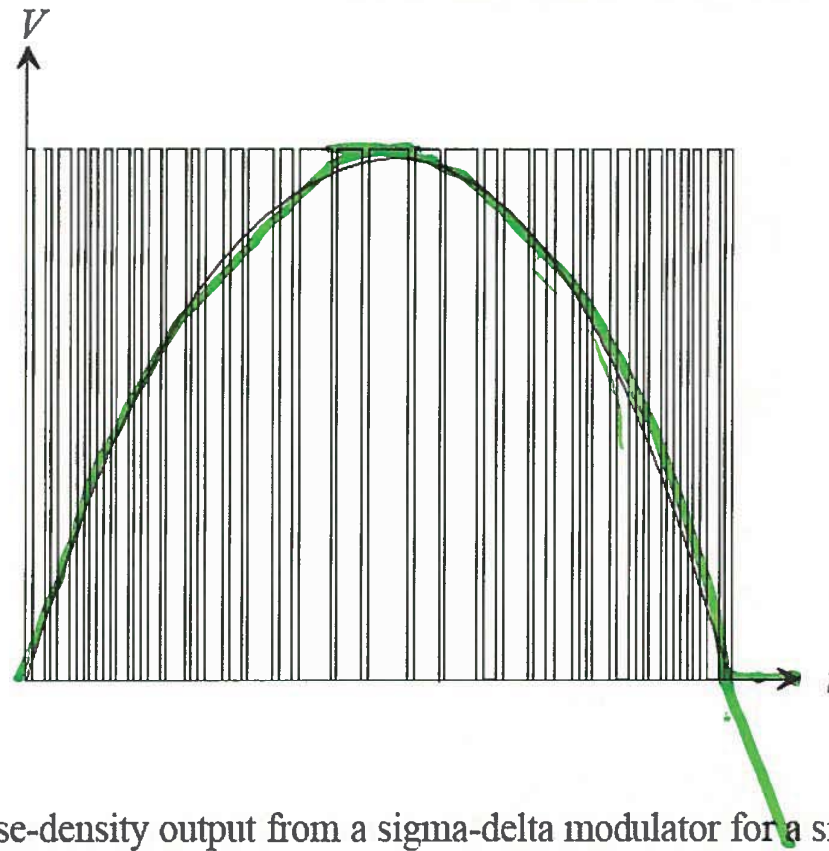


Figure 29.43 Pulse-density output from a sigma-delta modulator for a sine wave input.

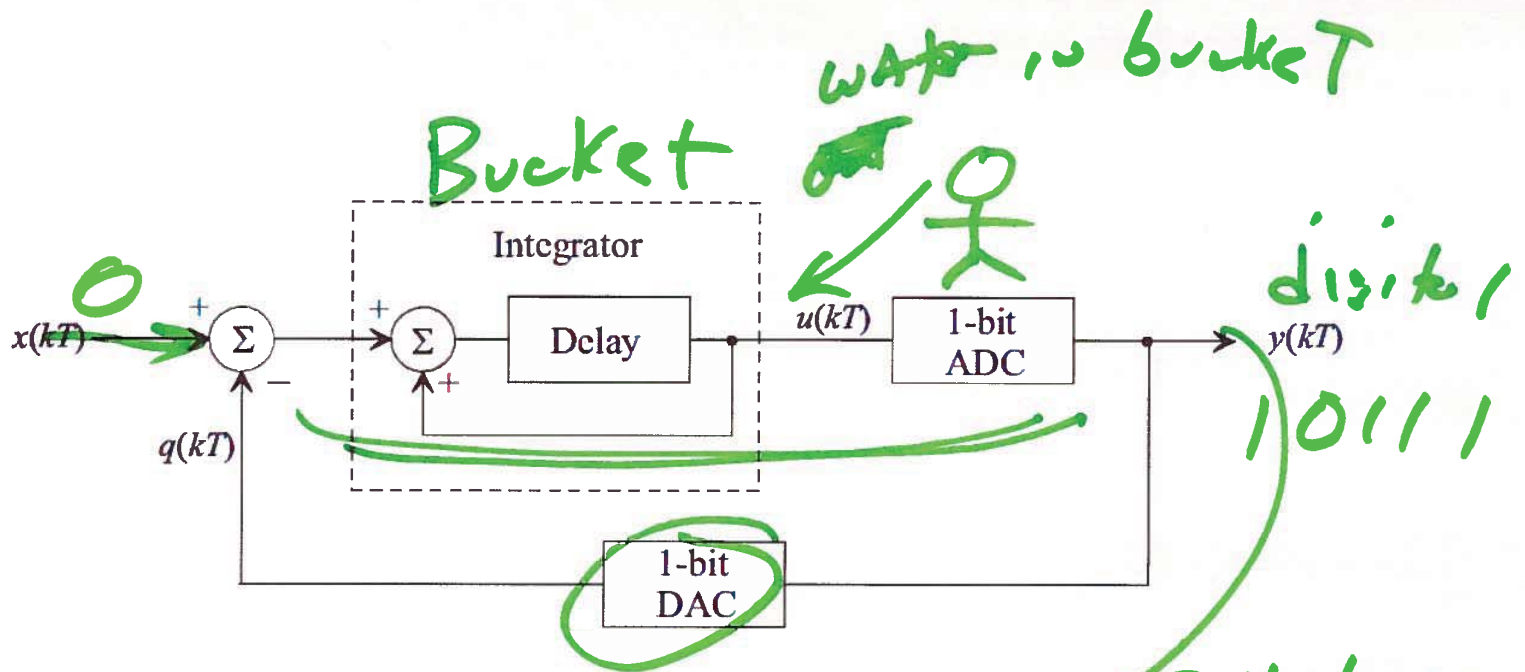
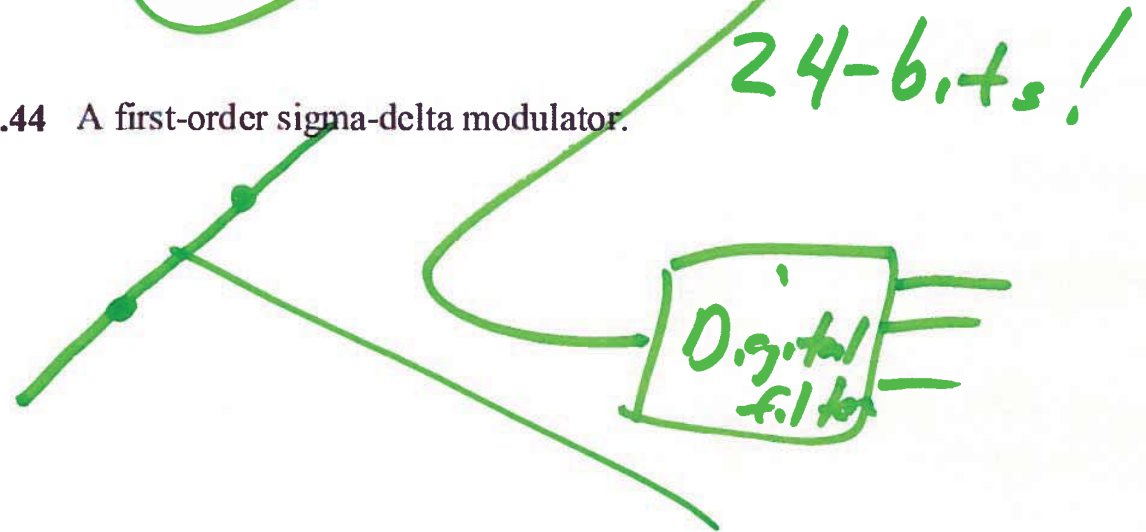


Figure 29.44 A first-order sigma-delta modulator.

$$\begin{aligned}
 & A_{OL} \\
 \hline
 & 1 + A_{OL} \cdot \beta \\
 & = \frac{1}{\frac{1}{A_{OL}} + \beta}
 \end{aligned}$$



14)

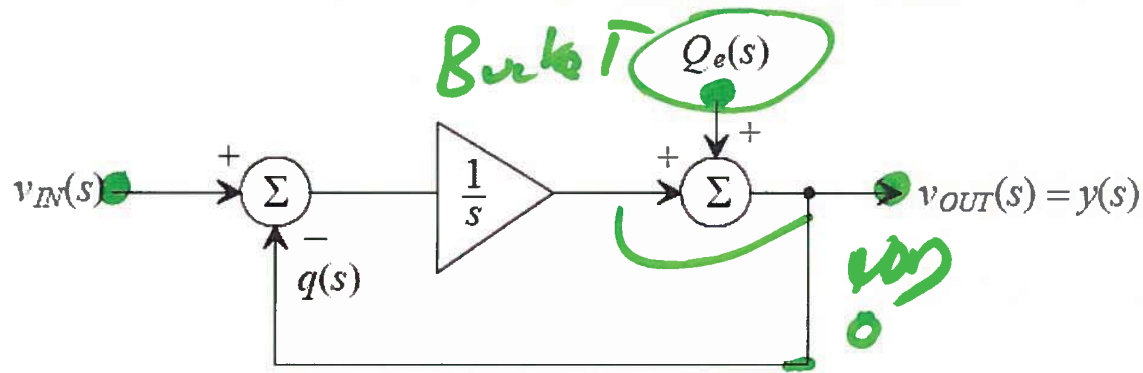
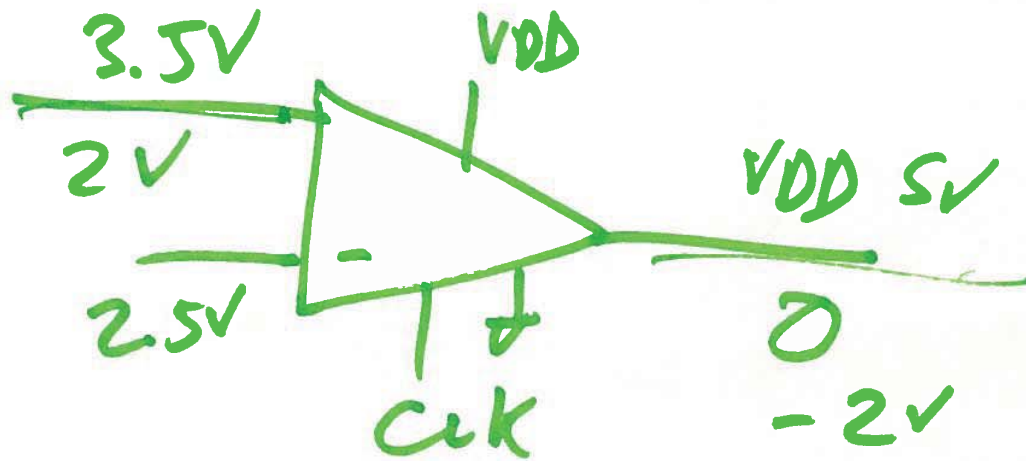


Figure 29.45 A frequency domain model for the first-order sigma-delta modulator.



$$STF = \frac{WNT}{2uN}$$

$$NTF = \frac{WNT}{Q_e}$$

15)

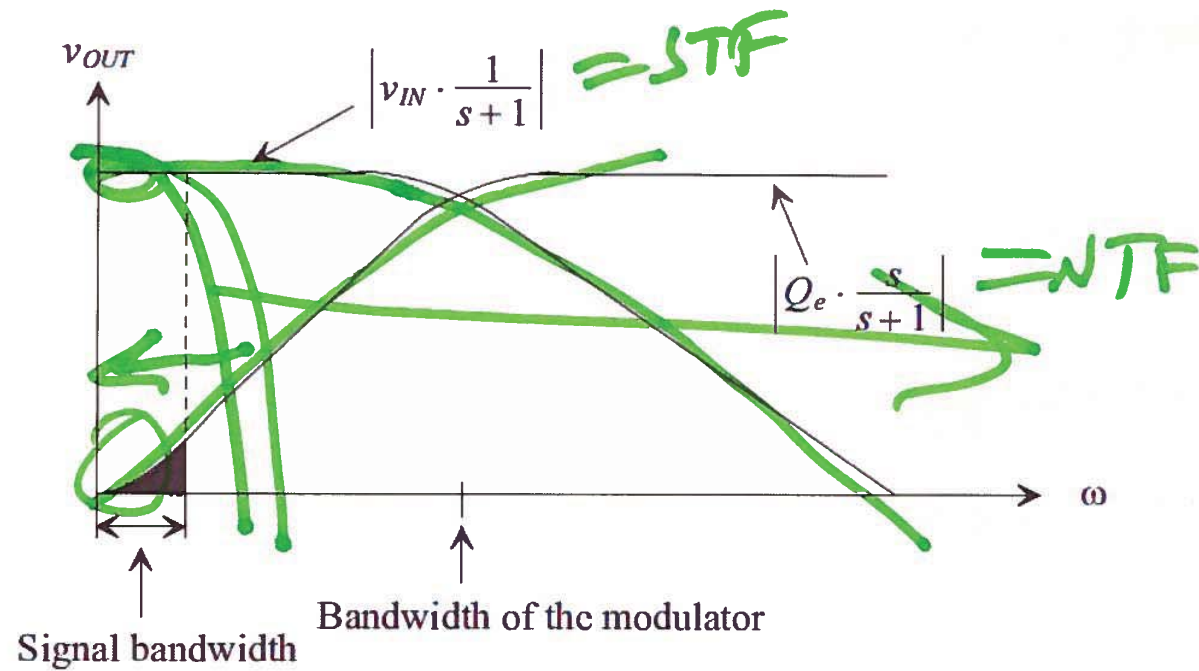


Figure 29.46 Frequency response of the first-order sigma-delta modulator.

$N =$

16)

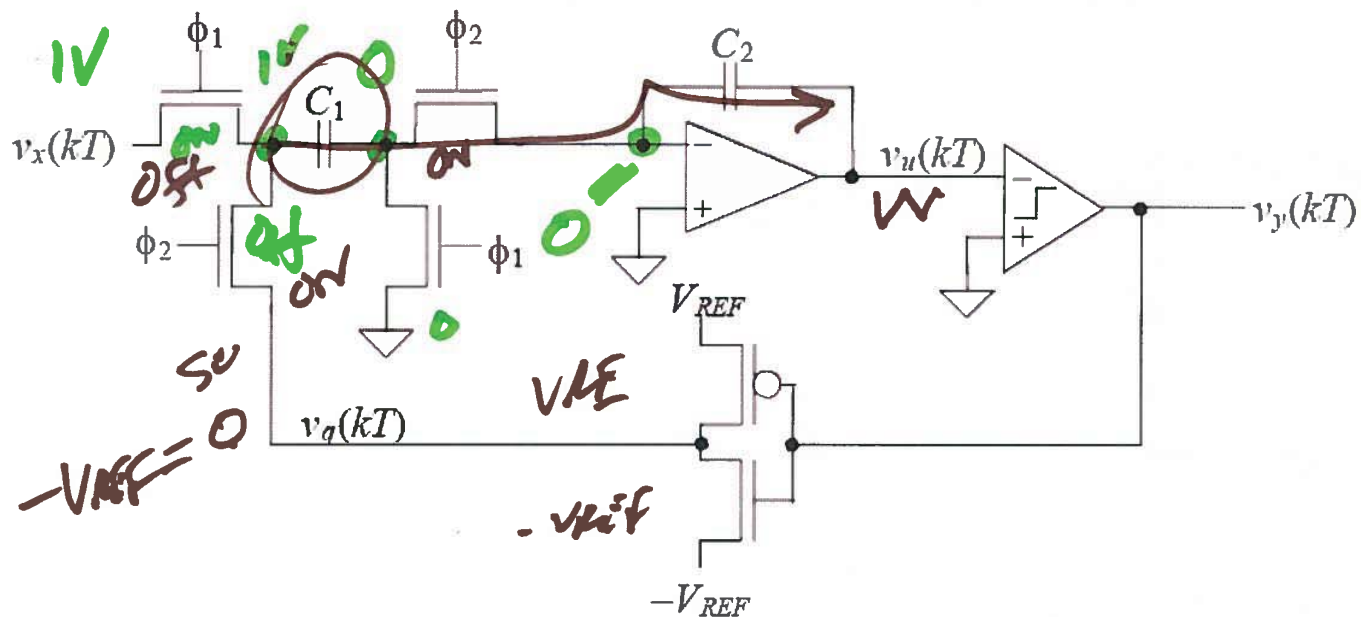


Figure 29.47 Implementation of a first-order sigma-delta modulator using a switched capacitor integrator.