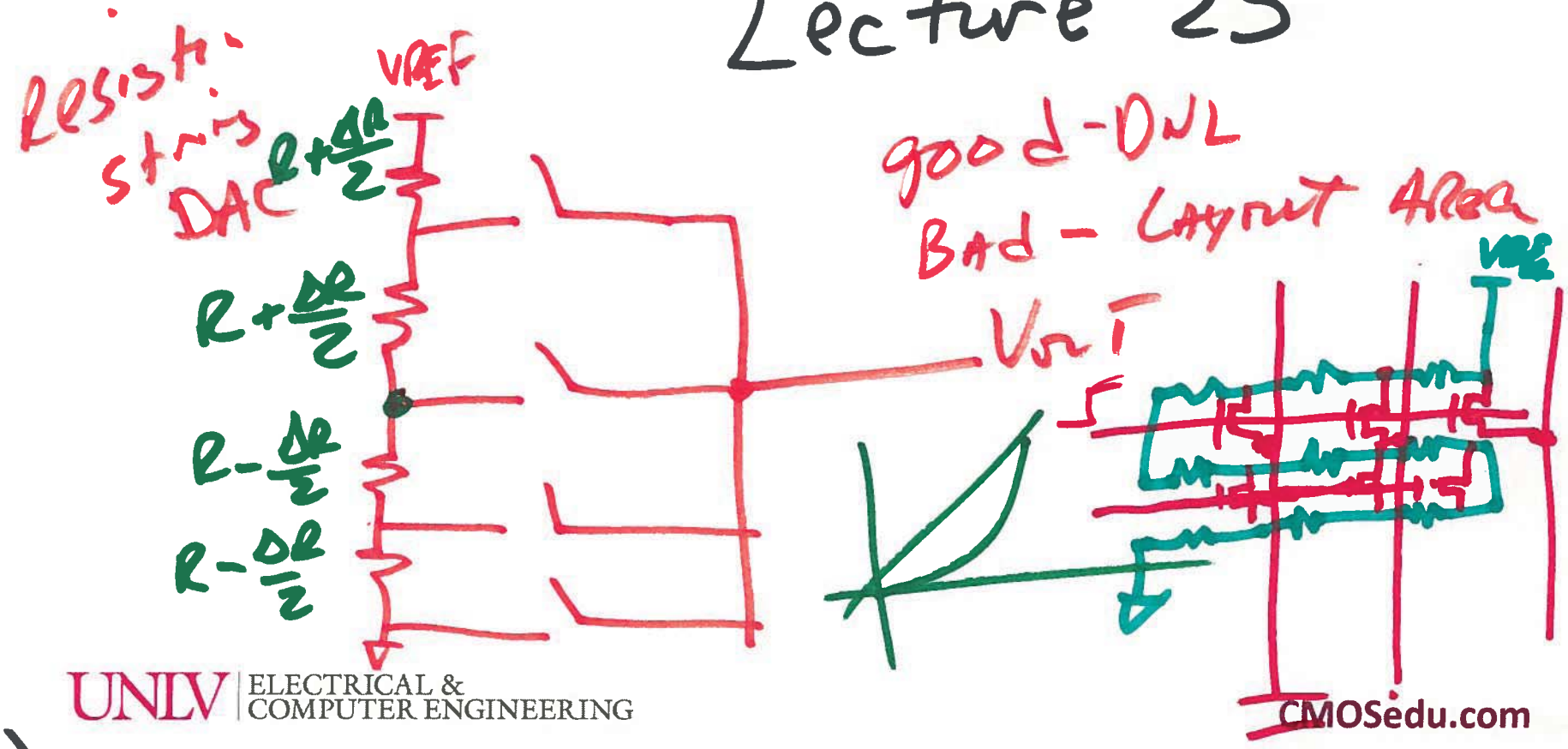
EEG720 Advanced Analog IC Design

April 21, 2016

Lecture 25



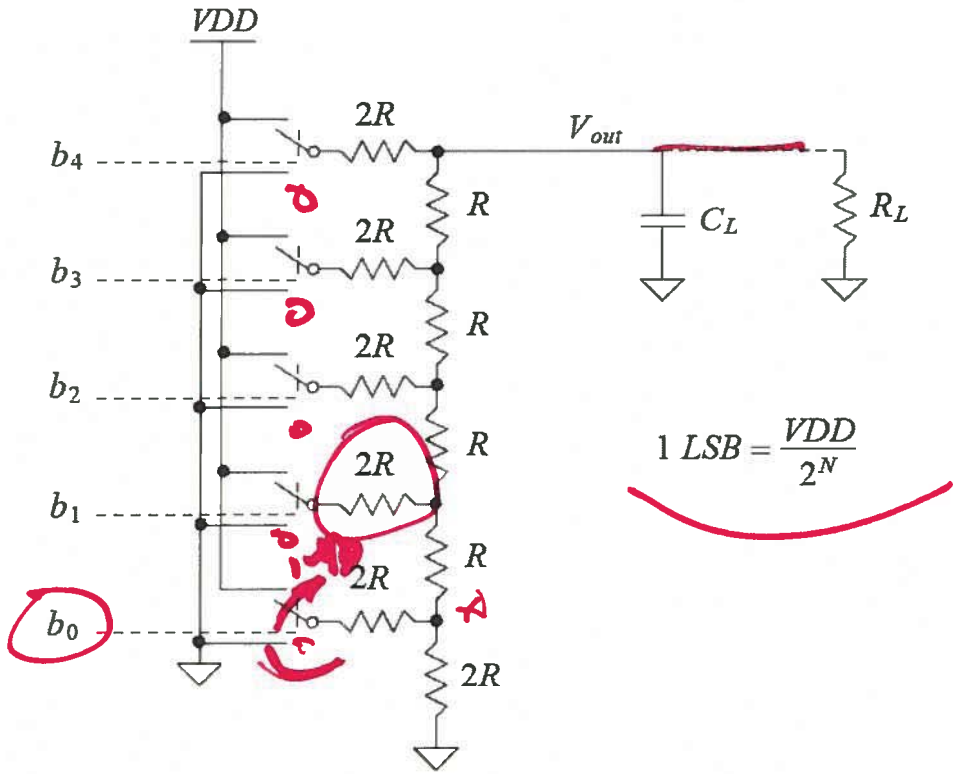


Figure 30.14 Voltage-mode (5-bit) DAC without an op-amp.

POOR MAN'S DAC

- To be added

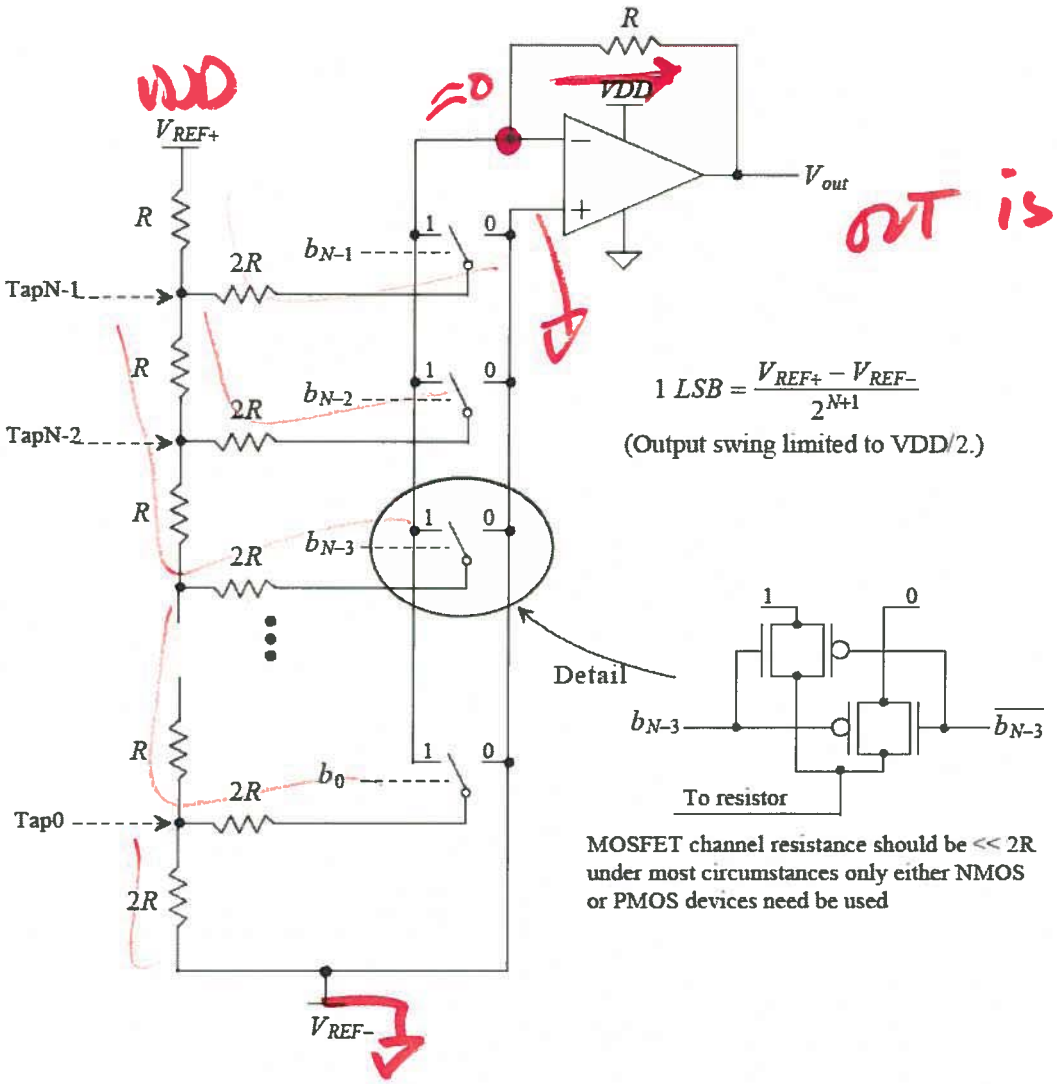


Figure 30.1 Traditional current-mode R-2R DAC.

- To be added

OT is always negative (BAD!)

Figures from CMOS Circuit Design, Layout, and Simulation, Copyright Wiley-IEEE, CMOSedu.com

- To be added

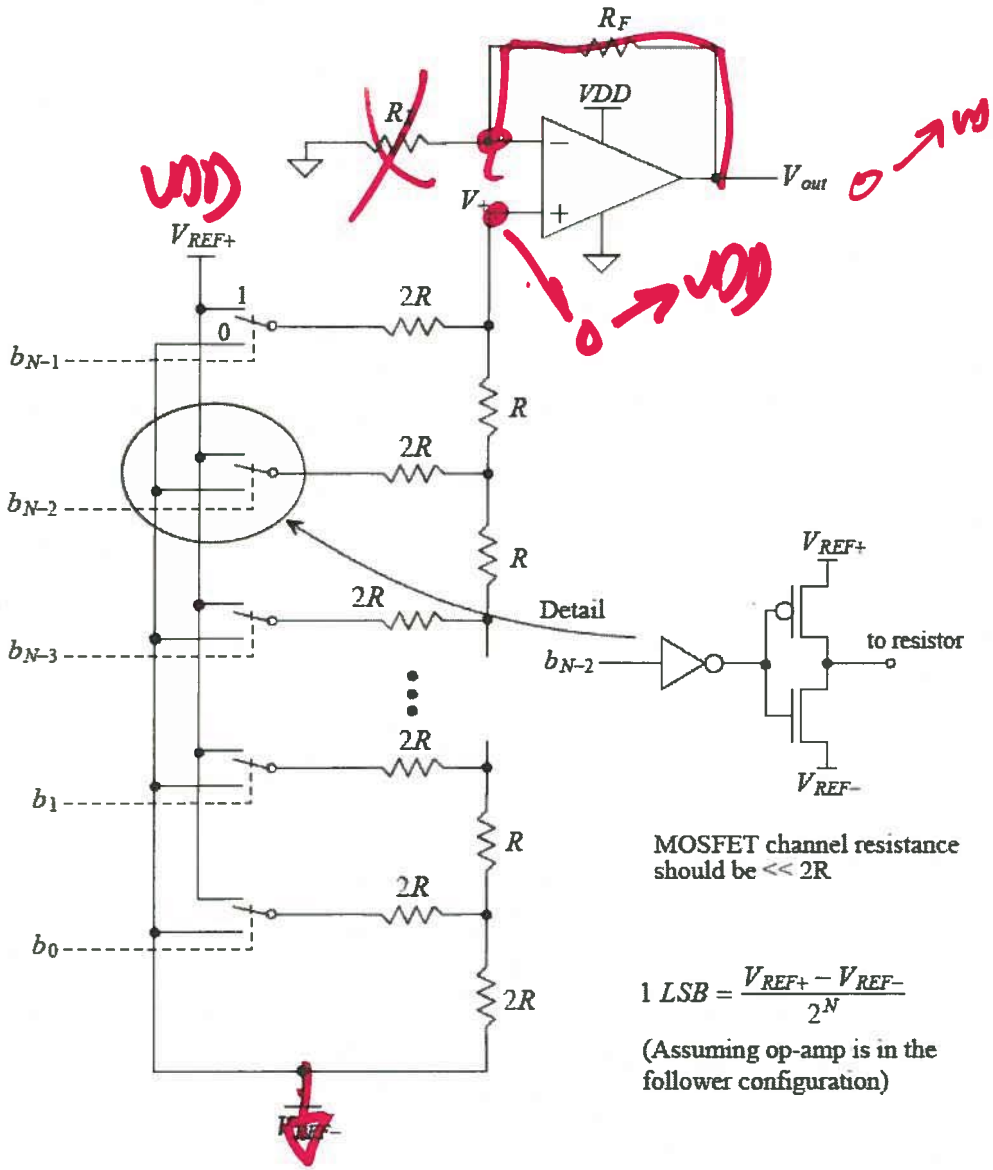


Figure 30.2 Traditional voltage-mode R-2R DAC.

Figures from CMOS Circuit Design, Layout, and Simulation, Copyright Wiley-IEEE, CMOSedu.com

4)

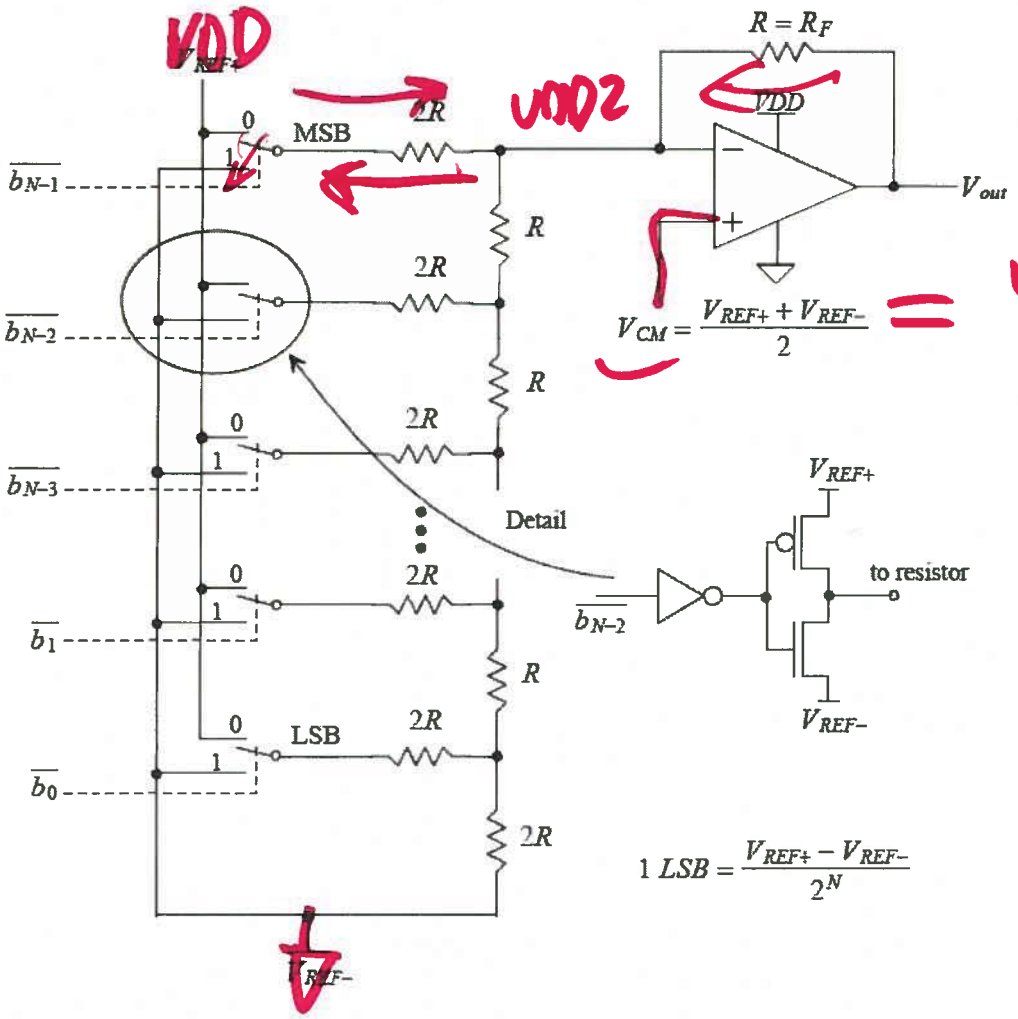


Figure 30.3 Wide-swing current-mode R-2R DAC.

- To be added

VDD → LSB

$\frac{VDD}{2}$

5)

Table 30.1 Summary of experimental results.

	8-bit	10-bit	12-bit
DNL (LSB)	0.150	0.450	2.000
INL (LSB)	0.200	1.000	3.000
Settling time	200 ns		
Power	3.88 mW (driving a 1k load)		
Area (mm^2)	0.045		
$f_{clk,max}$	4 MHz		
Output swing	$0 < V_{out} < VDD\ (= 1.8\ V)$		

matching of Resistors ~1%

- To be added

6)

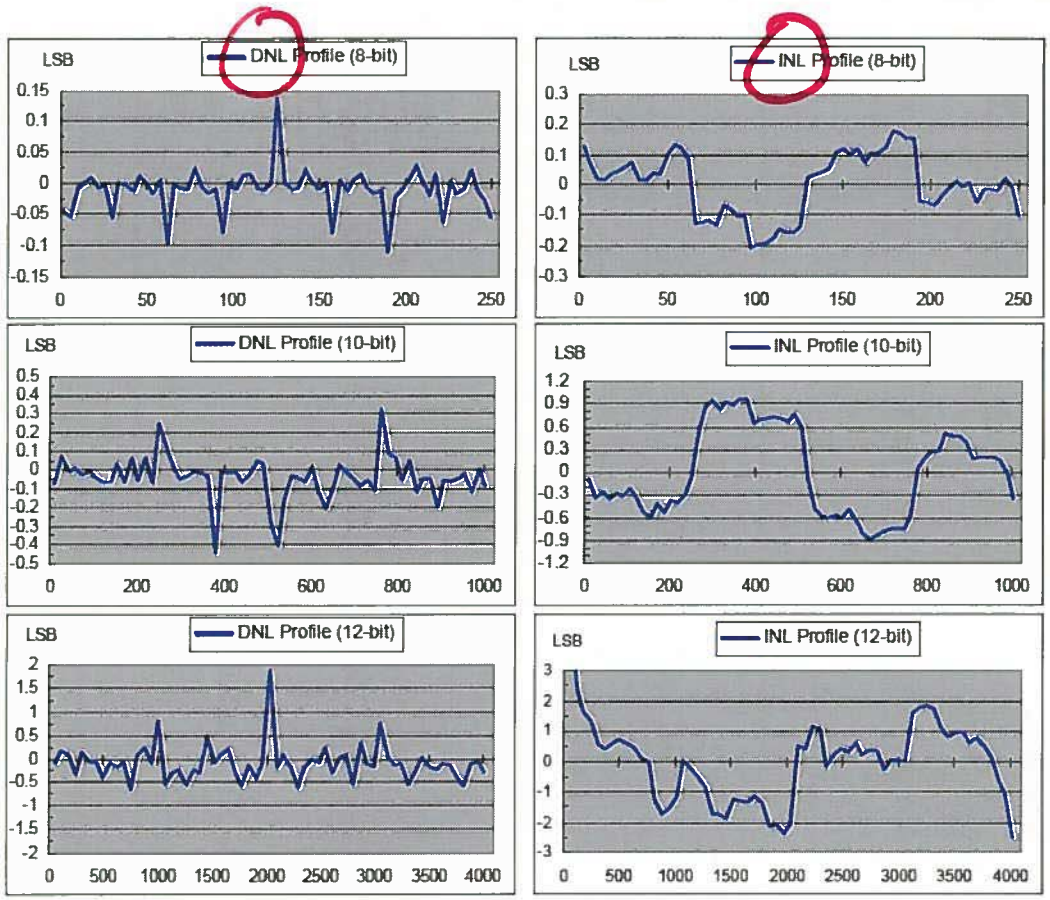


Figure 30.4 Experimental results for the wide-swing DAC of Fig. 30.3.

- To be added

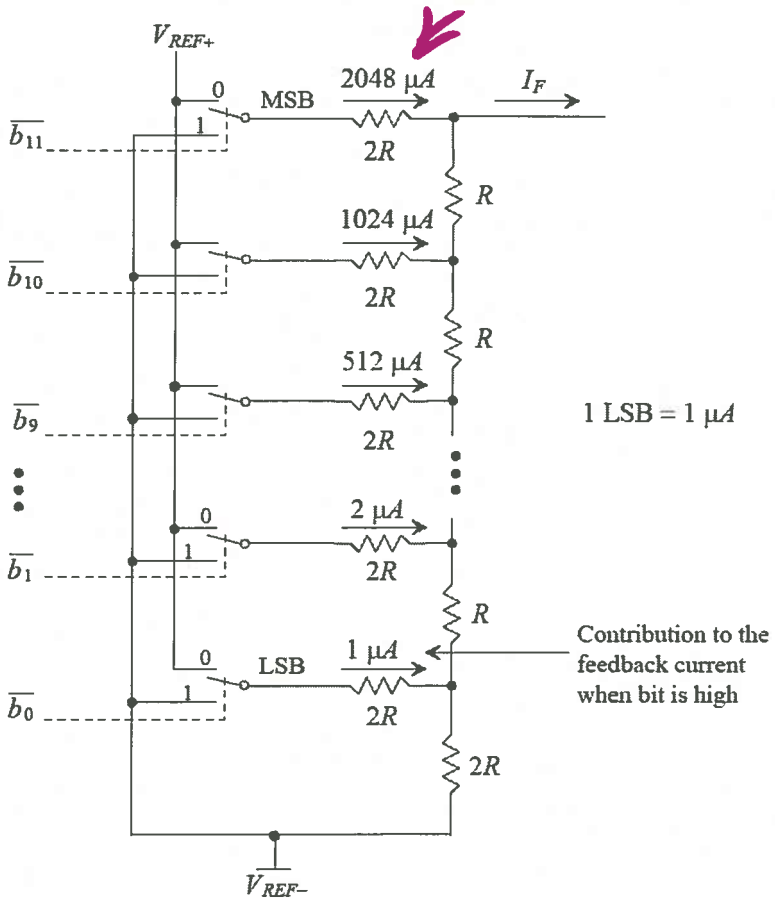


Figure 30.5 Showing how currents sum into the feedback current.

2047
↓
2048

- To be added

8)

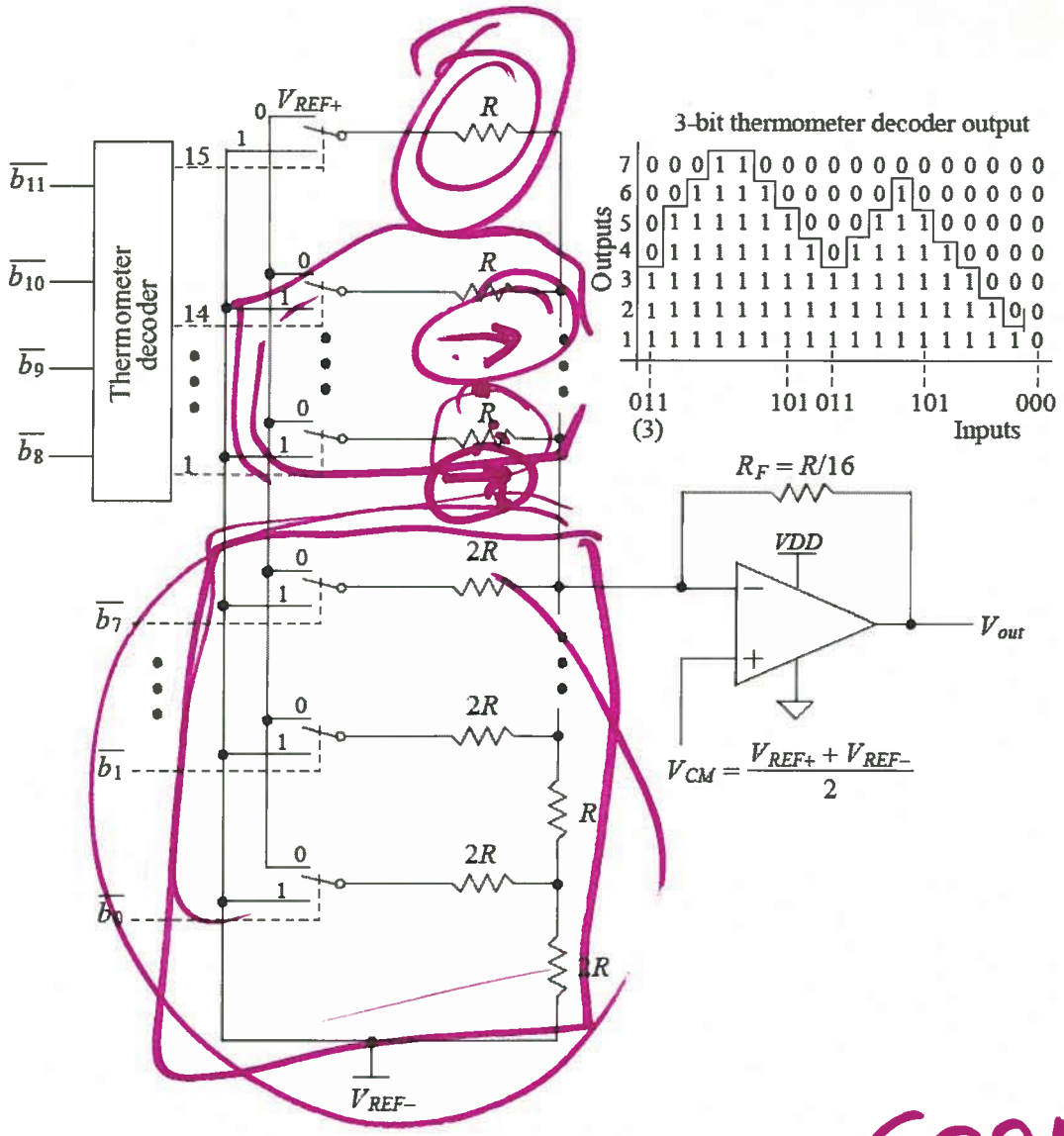


Figure 30.6 Segmentation in a wide-swing R-2R DAC.

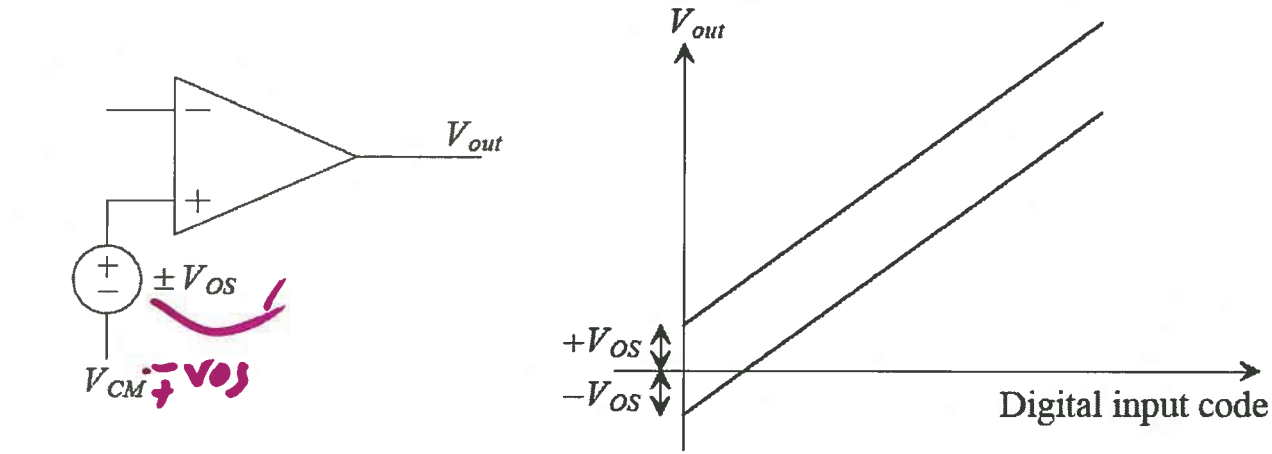
- To be added

128 → 14 /128
127

255 → 256

Segmentations

9)

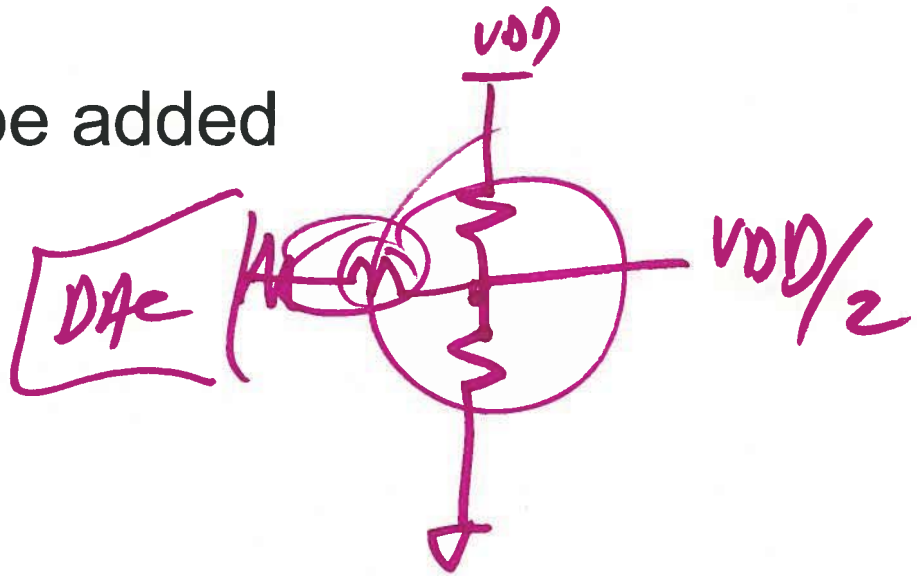


(a) Showing offset voltage in an op-amp.

(b) DAC transfer curves showing offset.

Figure 30.7 Showing how an op-amp offset affects the DACs transfer curves.

- To be added



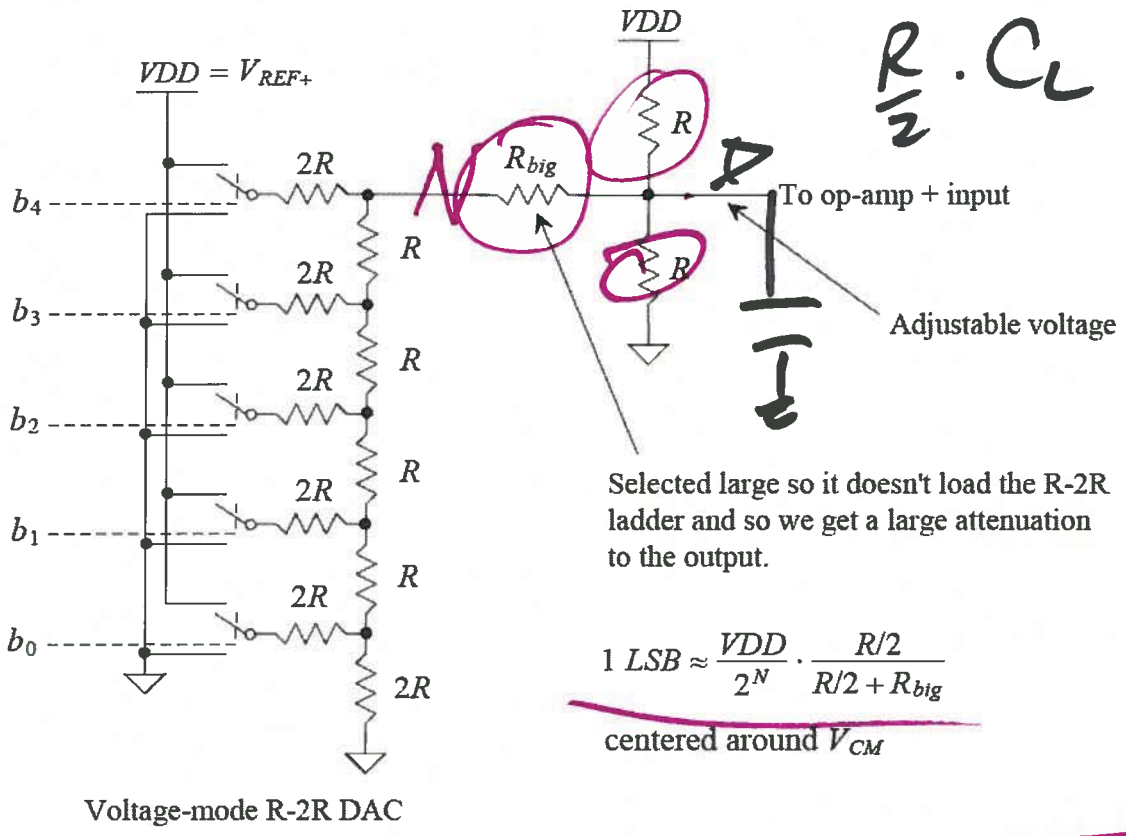
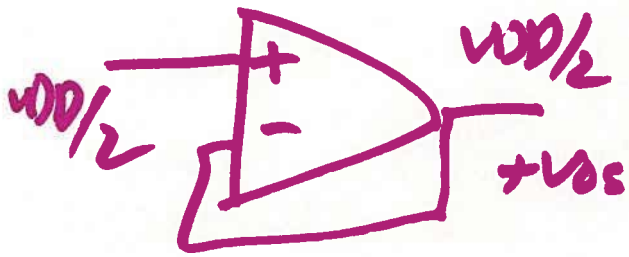
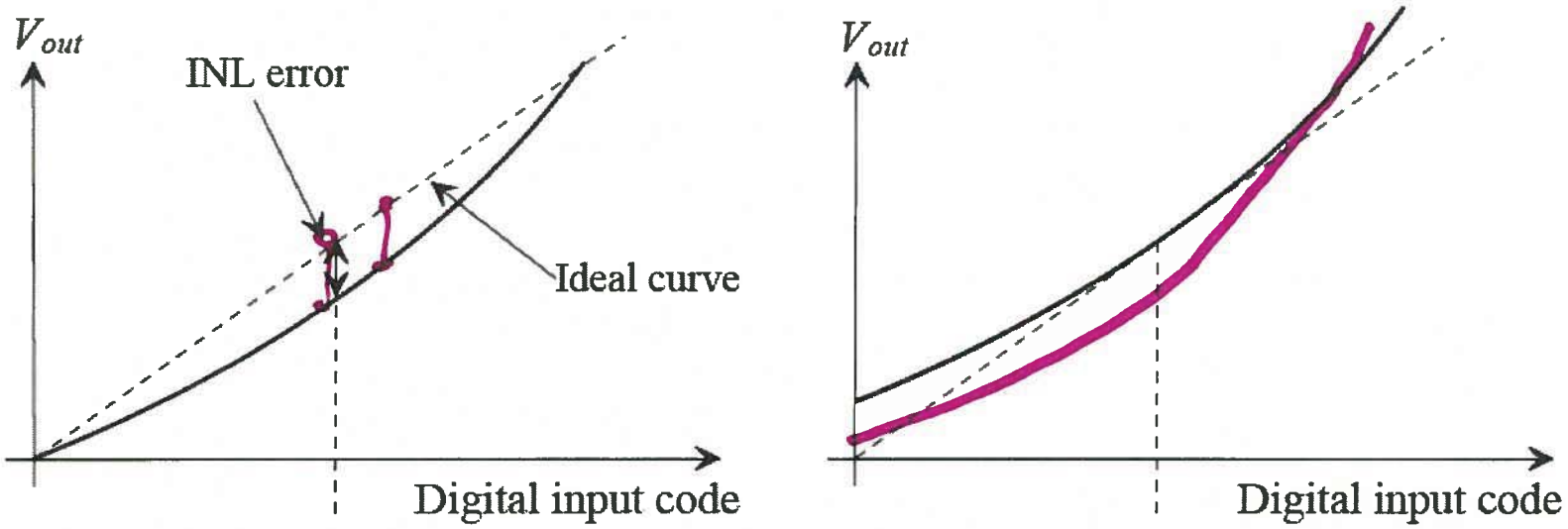


Figure 30.8 Trimming circuit for DAC offset.



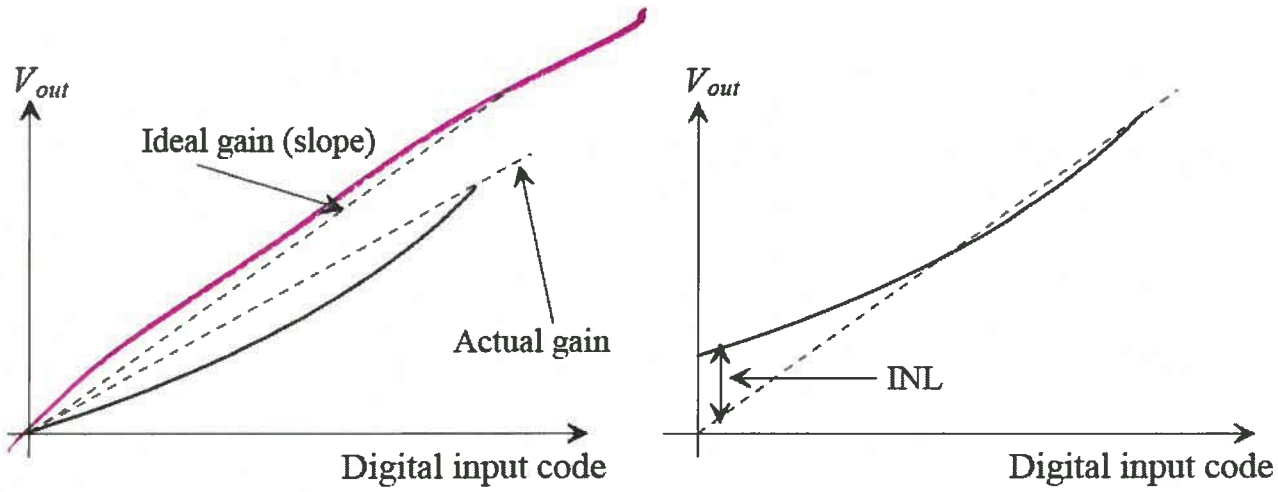
- To be added



(a) DAC transfer curves before calibration. (b) DAC transfer curves after offset calibration

Figure 30.10 Showing how INL can be seen as an offset error.

- To be added



(a) DAC transfer curves with gain error.

(b) DAC transfer curves after offset calibration with gain error.

Figure 30.11 Showing gain error and how it can cause problems in an offset calibration.

- To be added

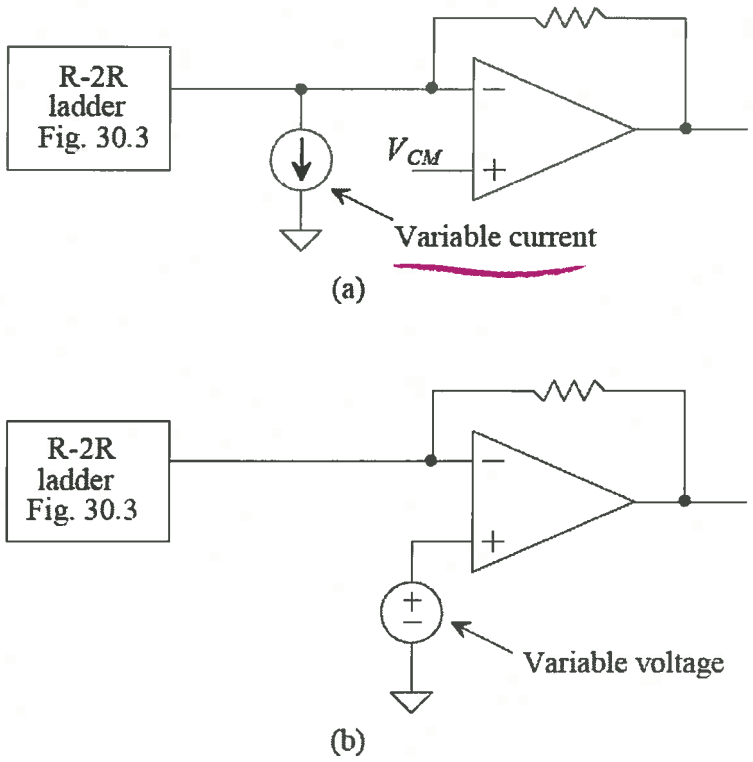


Figure 30.12 Trimming the output of the DAC using (a) current and (b) voltage.

- To be added

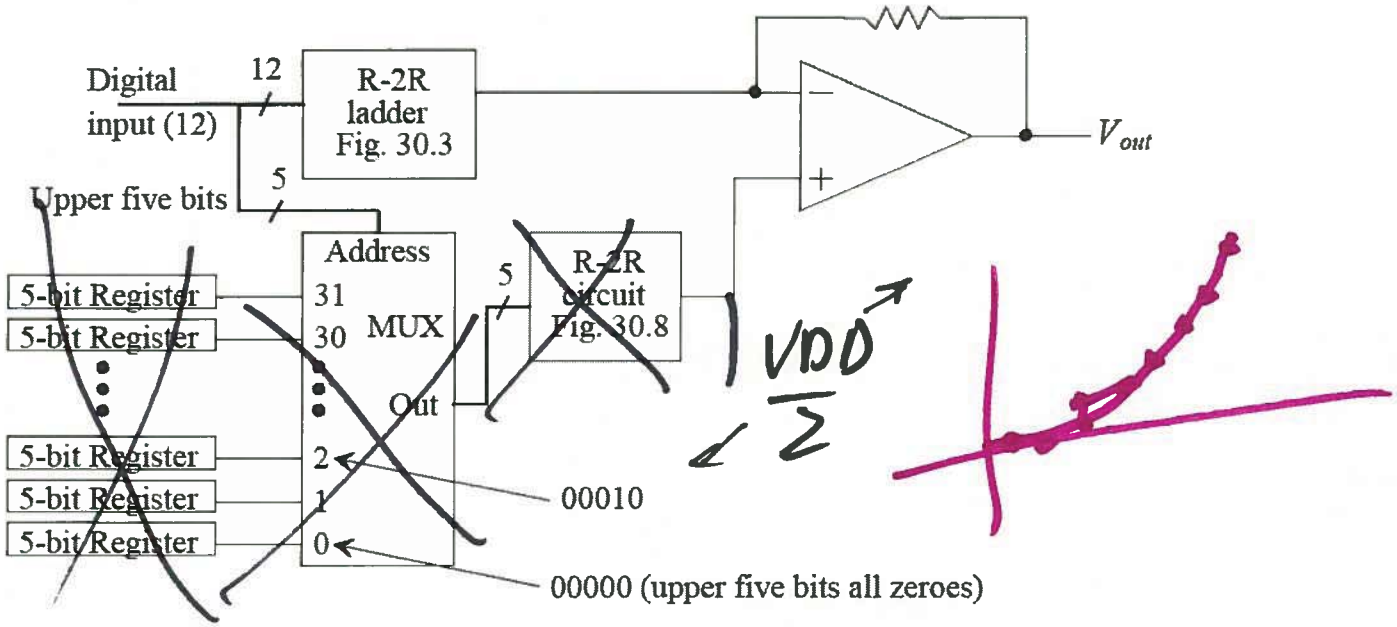
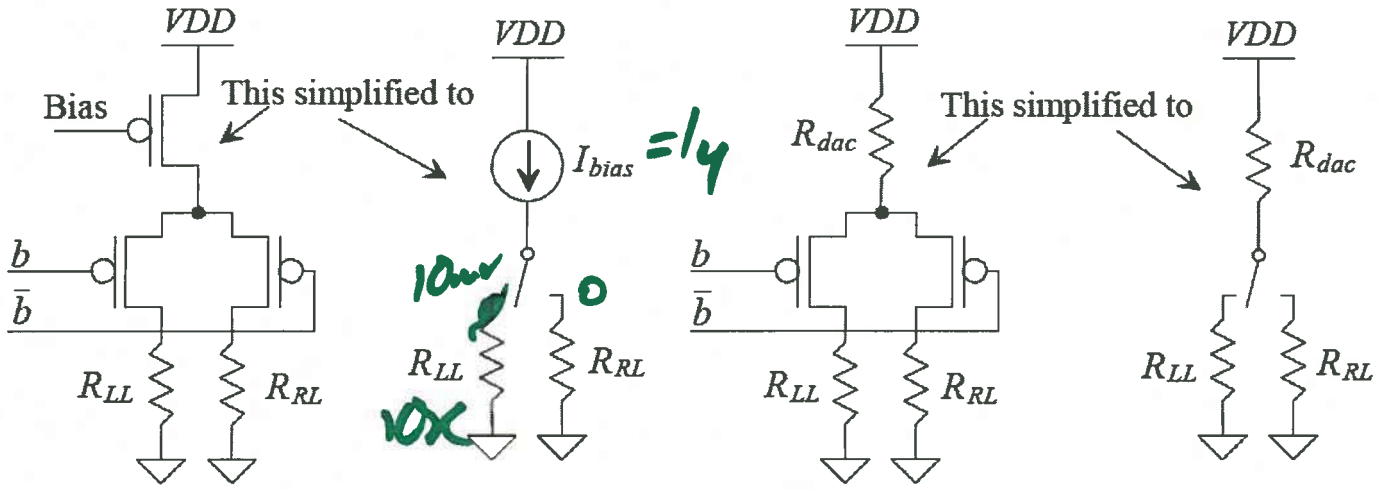


Figure 30.13 Calibration scheme for 12-bit DAC.

- To be added



Current-source-based cell. Resistor-based cell.

Figure 30.18 Basic cell used in a current-mode DAC.

- To be added

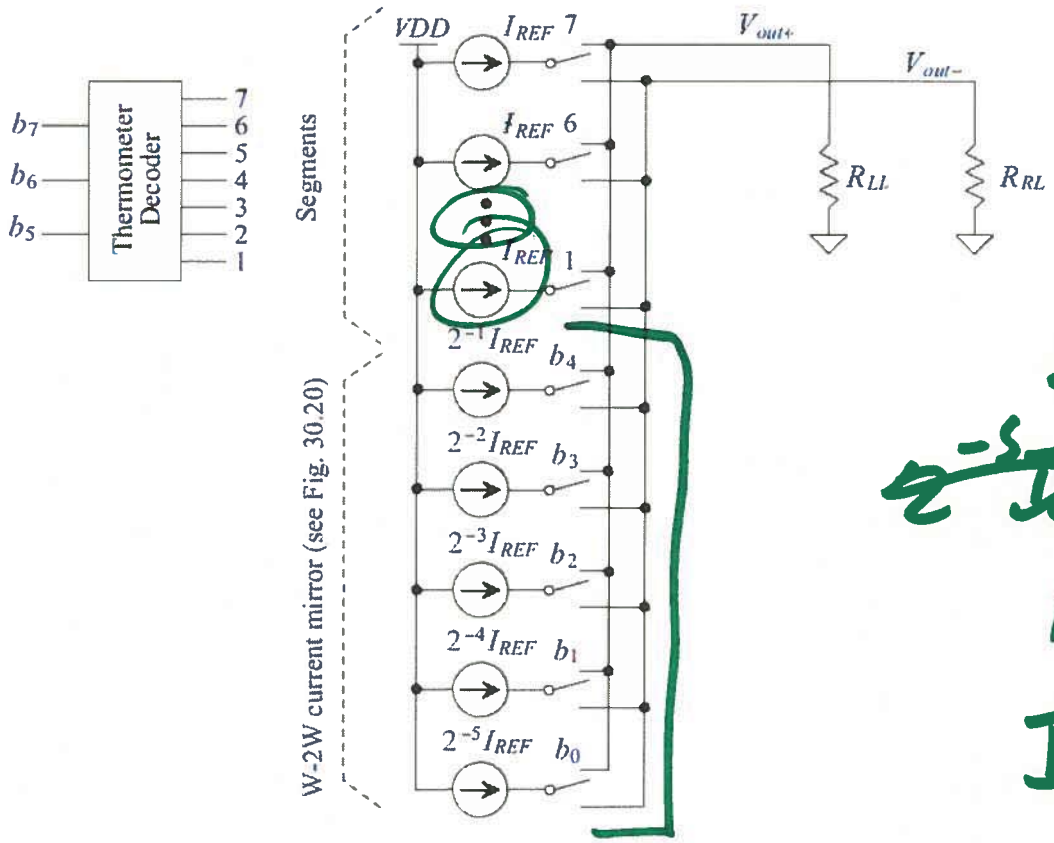


Figure 30.19 Implementation of a current-mode DAC.

$I_{REF} = 10\,mA = 10^{-2}$

$LSB = 2^{-5} \cdot I_{REF}$

$= 0.14\,A$

- To be added

Figures from CMOS Circuit Design, Layout, and Simulation, Copyright Wiley-IEEE, CMOSedu.com

n)

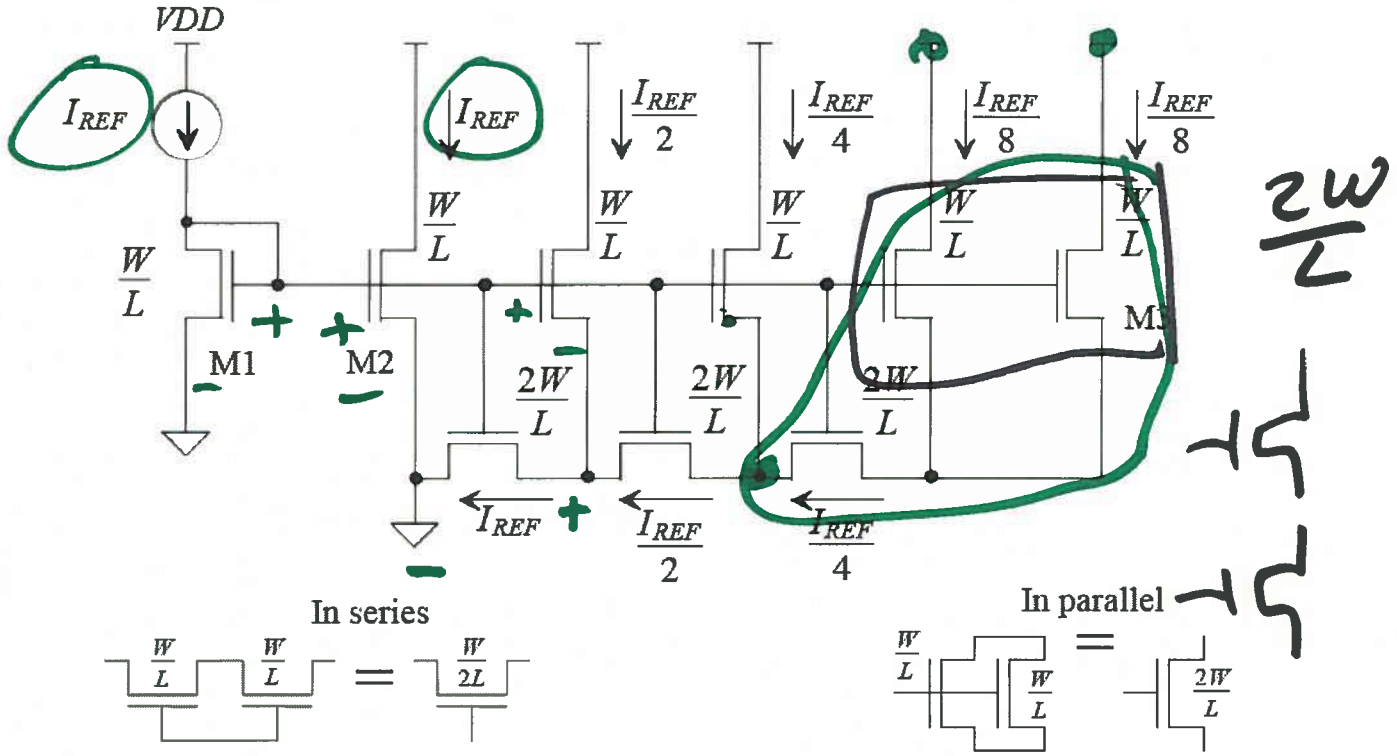
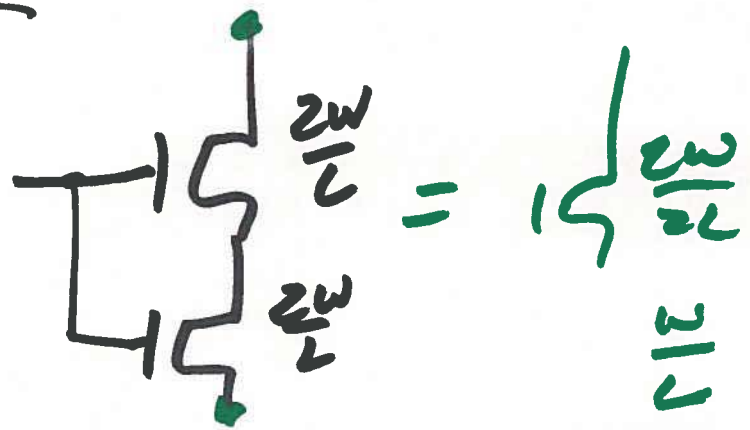


Figure 30.20 W-2W current mirror.

- To be added



Figures from CMOS Circuit Design, Layout, and Simulation, Copyright Wiley-IEEE, CMOSedu.com