ECG 720 Advanced Anclog IC Design April 26, 2016 Leature 26 ELECTRICAL & COMPUTER ENGINEERING CMOSedu.com

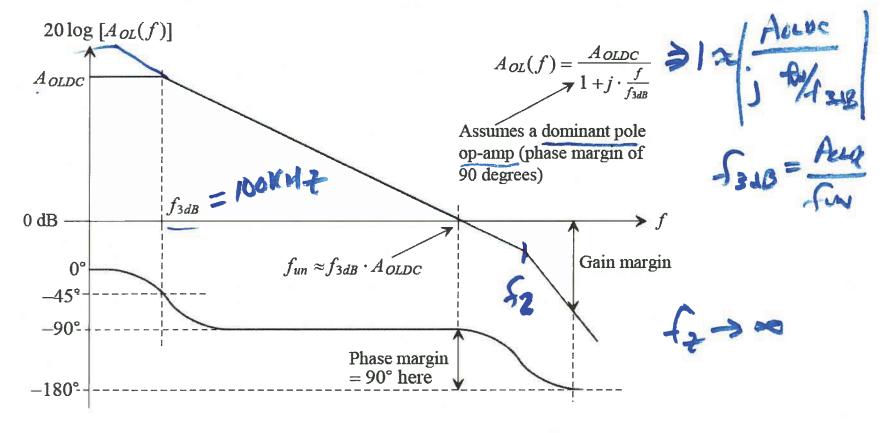


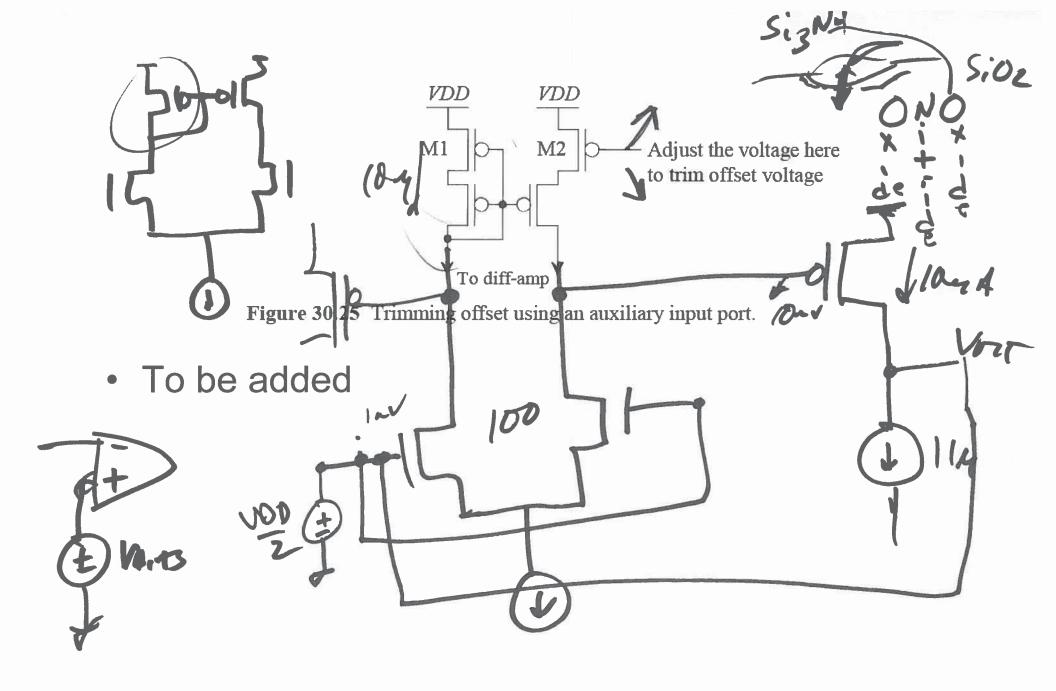
Figure 30.21 Magnitude and phase responses of an op-amp.

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VREF = 5V 10-bit converter AOLDC Needed so that error due to fivite Ancoe << \frac{1}{2} LSB VPEF-1LSO 125B = = = 5mV MAY NT error to be << 2.5~v = 115B. 2 = 1/258.2 1+ BADL

AOLOC Aproc > VINT = Vortfinal (1 - 1/2 ) = 2017final (1-e+/4) fu>> 0.44. (N+1) CMOSedu.com



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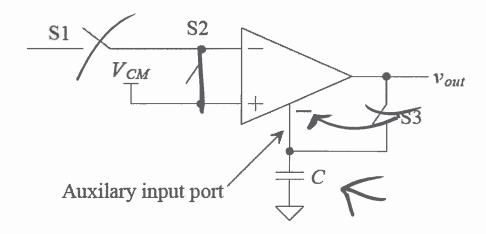


Figure 30.26 Using an auxiliary input port to lower offset.



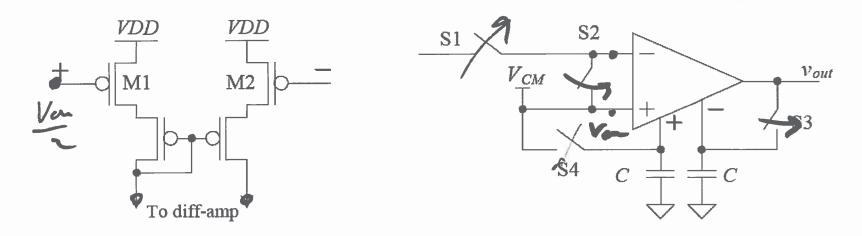


Figure 30.27 Using an auxiliary input port to lower offset (two terminals).

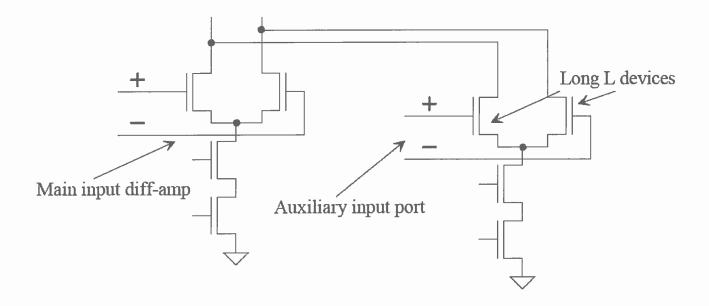


Figure 30.28 Using an auxiliary diff-amp for balancing current in an op-amp's input.



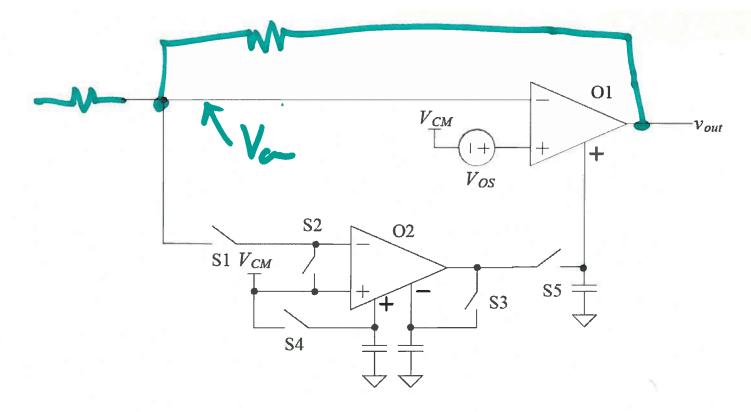


Figure 30.29 Continuous-time offset removal.

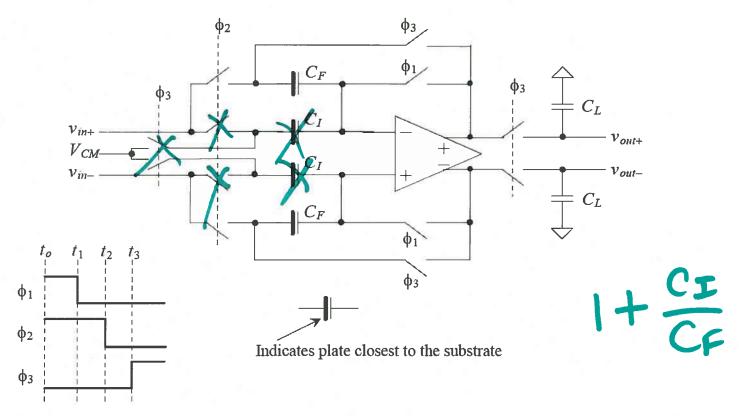
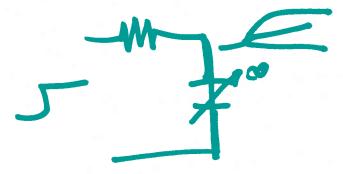
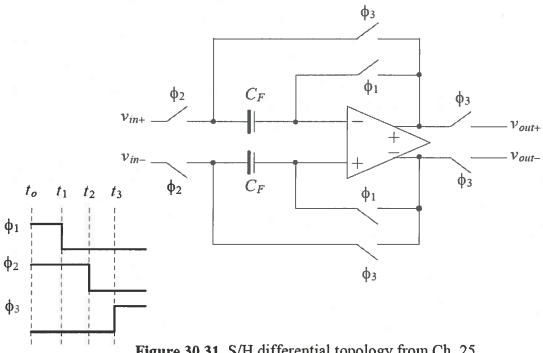


Figure 30.30 Data converter S/H building block.







#### Figure 30.31 S/H differential topology from Ch. 25.



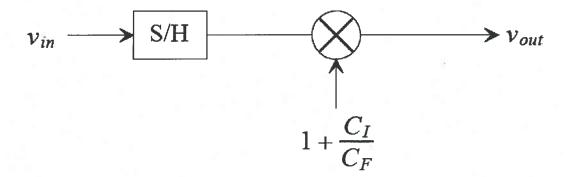


Figure 30.32 Block diagram for the S/H of Fig. 30.30.



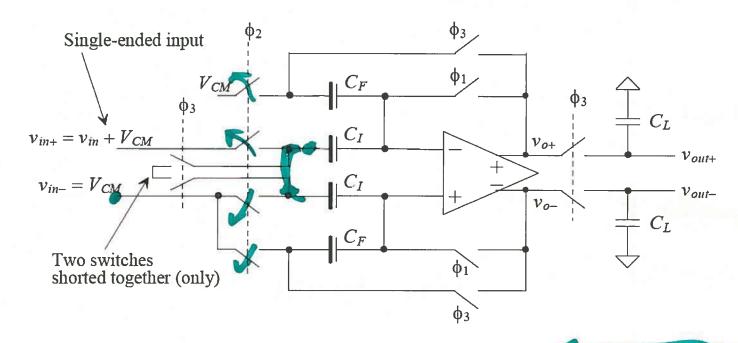


Figure 30.34 Single-ended to differential S/H.

Practical way to

