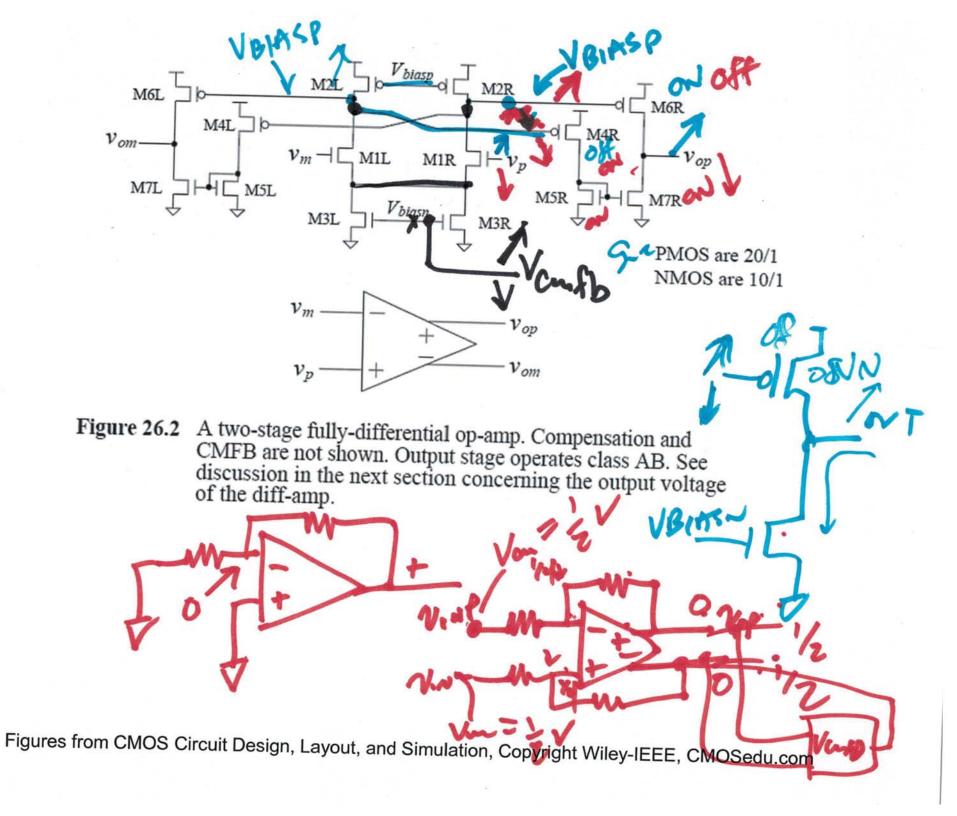
Lecture 9 Advanced W VGS L -> Speed LA speed V

gaint

gaint

gaint NW = 10> - NUH2 ≈ 20 µA I_D ≈ 20 µA Figure 26.1 Gate-source voltages plotted against drain currents.

Figures from CMOS Circuit Design, Layout, and Simulation, Copyright Wiley-IEEE, CMOSedu.com



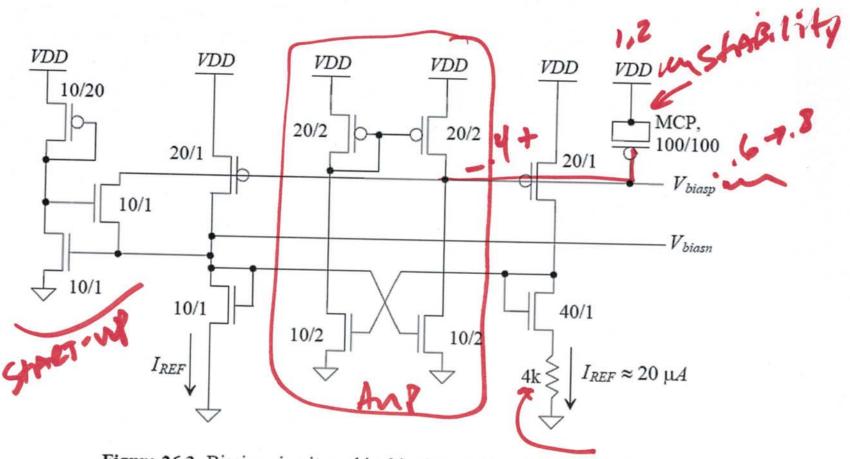
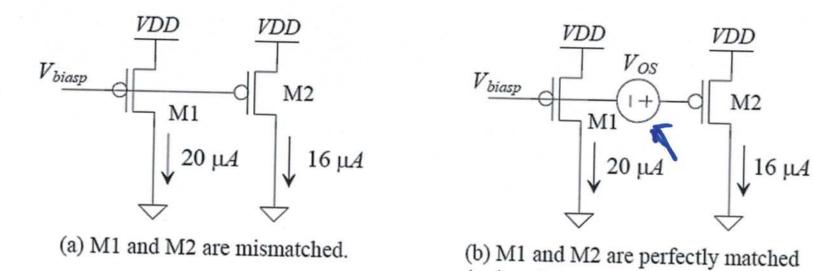


Figure 26.3 Biasing circuit used in this chapter. This bias circuit pulls approximately 50 microamps.





(as in a SPICE simulation).

Figure 26.5 How we add an offset into the circuit to model mismatch.



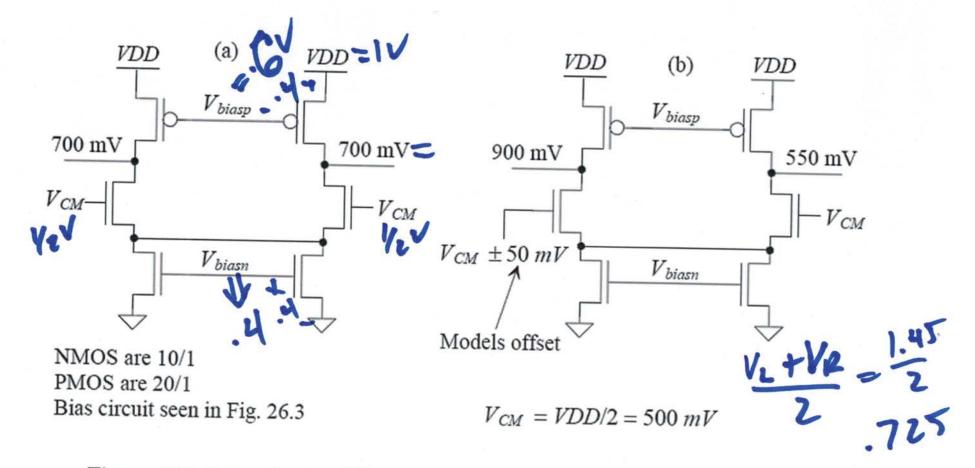


Figure 26.6 Comparing the diff-amp's output voltages with and without an offset.

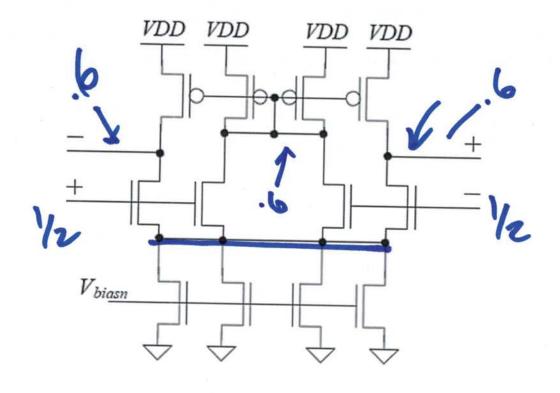


Figure 26.7 A fully-differential diff-amp that generates its own bias for the PMOS.



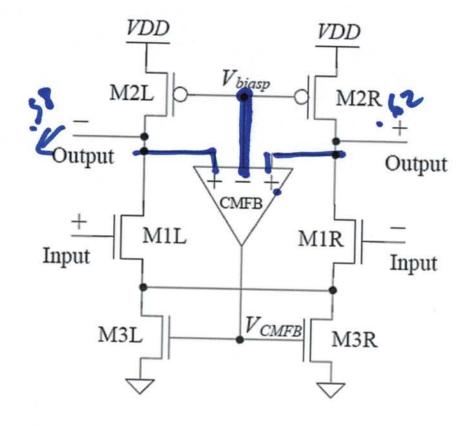


Figure 26.8 Using a common-mode feedback (CMFB) amplifier to set the output voltages.



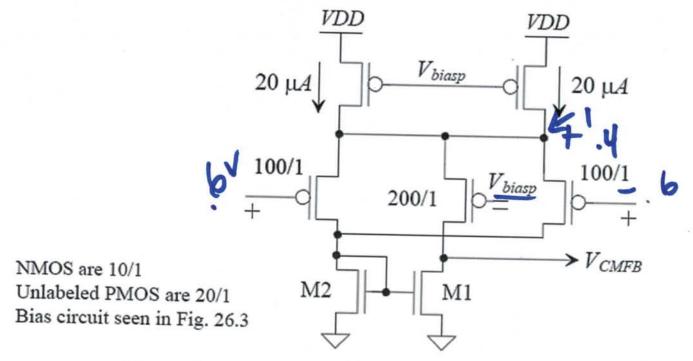
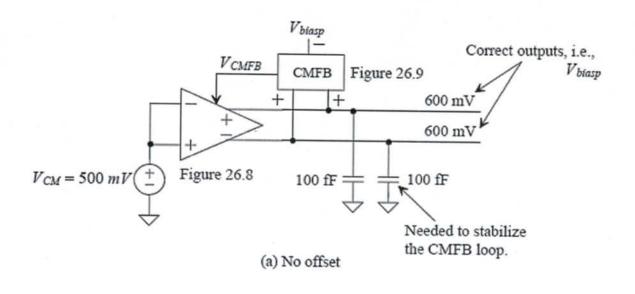
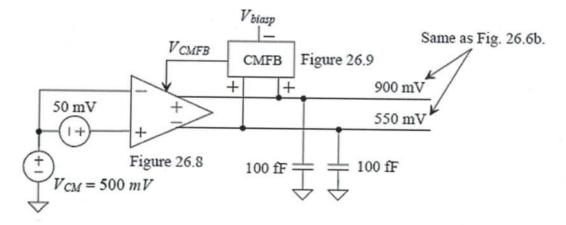


Figure 26.9 Implementation of the CMFB amplifier in Fig. 26.8.







(b) With a 50 mV offset. Note how the CMFB isn't doing anything.

Figure 26.10 Simulating the operation of the CMFB circuit in Fig. 26.9.



UNIV ELECTRICAL & COMPUTER ENGINEERING

CMOSedu.com

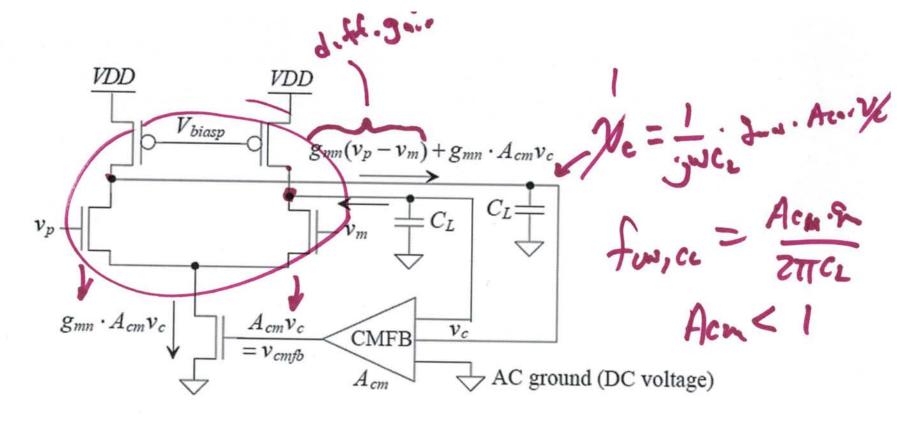


Figure 26.11 Schematic view of differential and CM feedback.







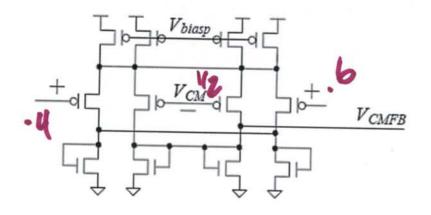
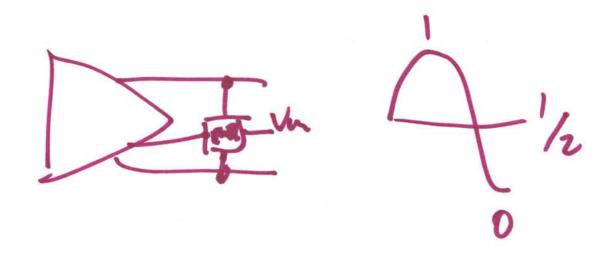


Figure 26.12 A CMFB amplifier with a gain of nominally unity.





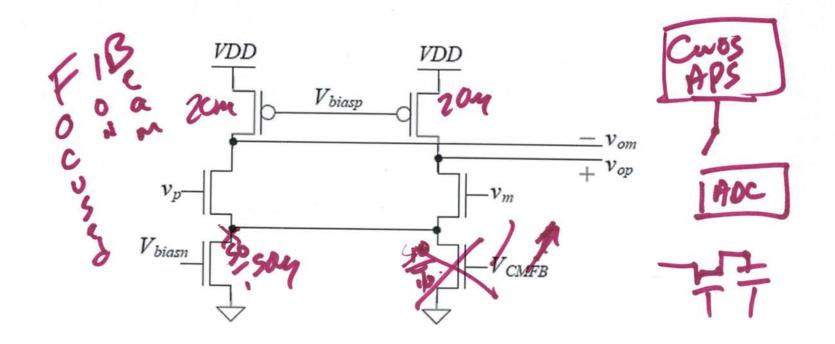


Figure 26.13 Reducing the forward gain of the CMFB loop.

