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Synchronous Mirror Delays

ECG 721 – Memory Circuit Design

Kevin Buck

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Introduction

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- A synchronous mirror delay (SMD) is a type of clock generation circuit
- Unlike DLLs and PLLs an SMD is an open loop system
  - ✓ No clock jitter due to feedback and voltage oscillation
- SMDs have both analog and digital implementations
- An SMD is useful because it only requires two clock cycles to generate an internal clock synchronized to the external clock
  - ✓ Useful for application such as DRAM
  - ✓ Eliminates idle power consumption
  - ✓ Startup time is 2 * T_{clk}
- A major drawback of SMDs is that they must be designed for a specific buffer and propagation delay

Digital Synchronous Mirror Delay

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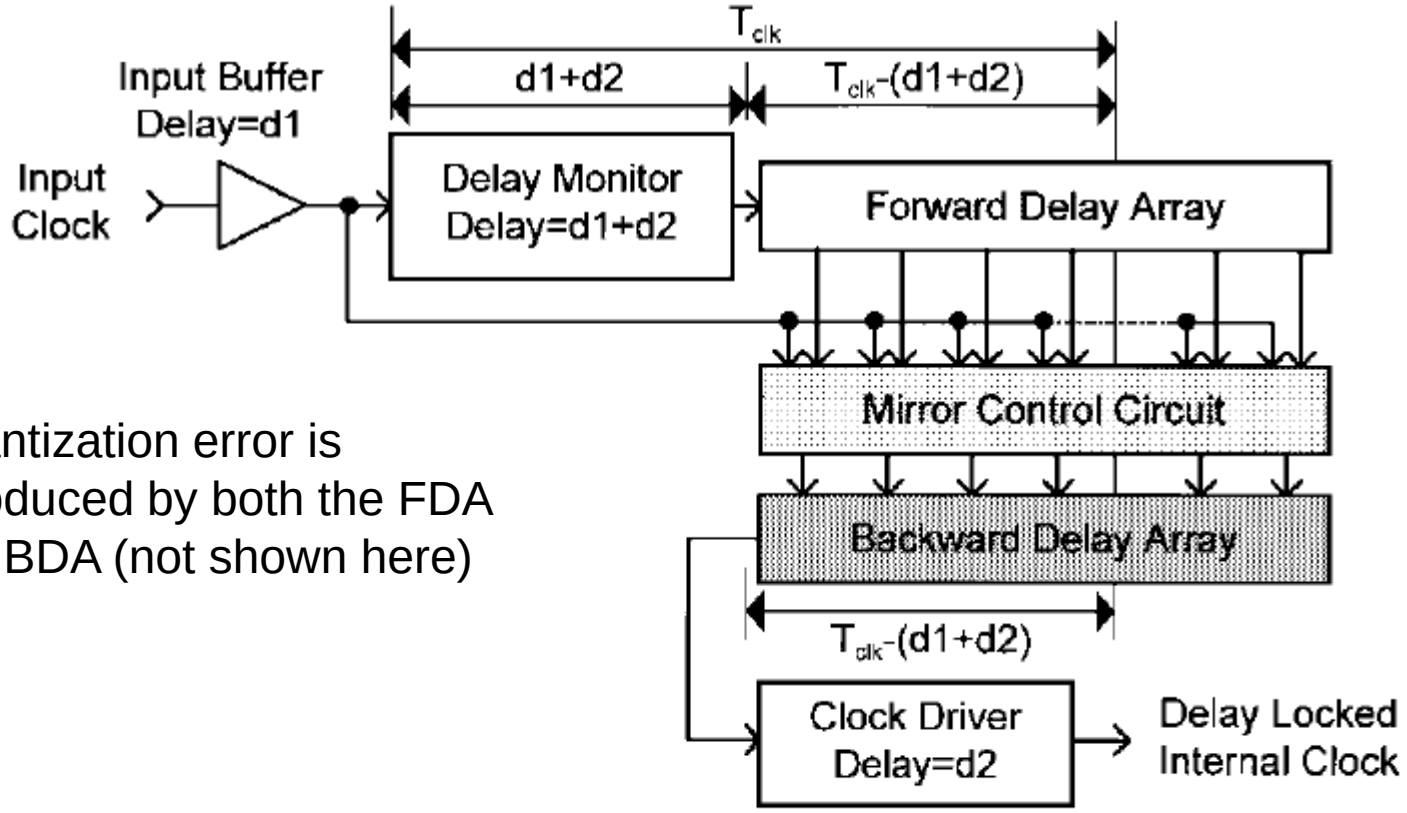
- The first type of implementation we will consider is the digital SMD (DSMD)
- The components of a DSMD are:
  - Input buffer
  - Delay monitor (DM)
  - Forward delay array (FDA)
  - Mirror control circuit (MCC)
  - Backward delay array (BDA)
  - Clock driver
- The circuit replicates the input clock by comparing the difference between the signal from the input buffer and the delay monitor

DSMD Block Diagram



Quantization error is introduced by both the FDA and BDA (not shown here)

DSMD Ideal Timing Diagram

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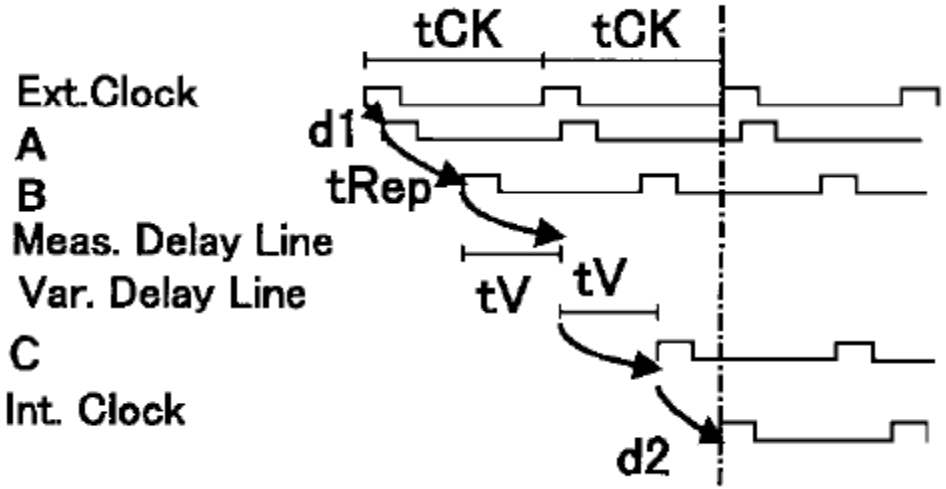

$$tV = T_{clk} - (d_1 + d_2)$$

DSMD Basic Circuit

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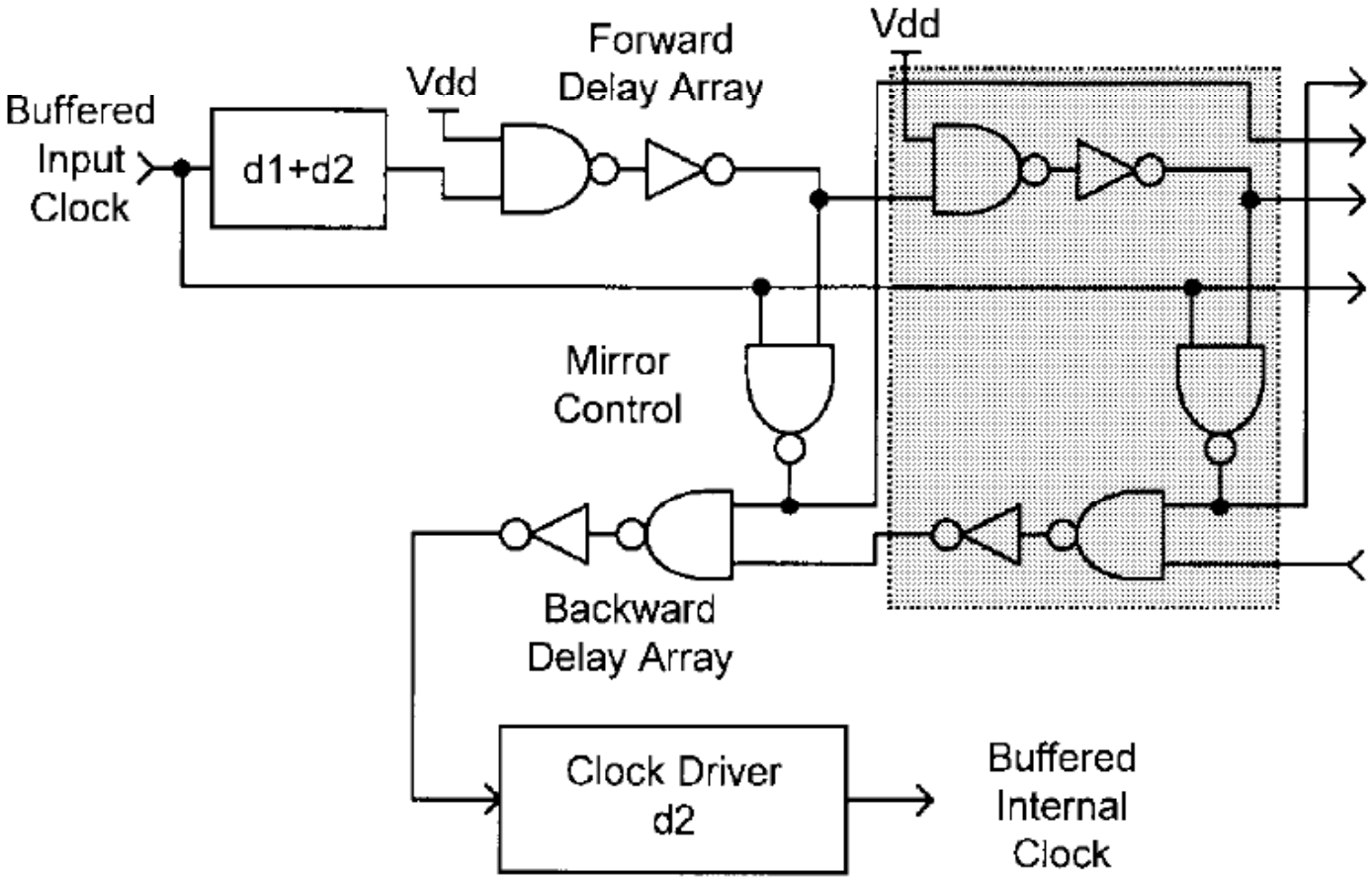

DSMD Calculations

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- Each delay element is a NAND gate and an inverter (an AND gate), the total array size can be determined by:
  - $T_{clk,max} = d_1 + d_2 + N * d_e$
  - $N = \dfrac{T_{clk,max} - (d_1 + d_2)}{d_e}$
- The total delay from the input to the output is:
  - $t_d = d_1 + (d_1 + d_2) + [T_{clk} - (d_1 + d_2) + t_{Qe}] + [T_{clk} - (d_1 + d_2) + t_{Qe}] + d_2 = 2(T_{clk} + t_{Qe})$
- The quantization error has a maximum value of one delay element (AND gate), this calculation ignores the delay from the NAND gate of the MCC.
- The clock period must be significantly larger than the delay monitor delay time (more specifically the width of the pulse must be larger than the delay time)

DSMD Calculations

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- The delay element should be the minimum possible delay to minimize phase quantization error, t_{Qe}
- The circuit on the next page has a d_e of 77 ps, the delay monitor ($d_1 + d_2$) is approximately 200 ps and it is designed for a minimum clock speed of 1 GHz ($T_{clk,max}$ = 1 ns) so N is 10.40 (11)
  - ✓ The circuit can actually operate at frequencies slightly lower than this as well due to the delay between the second and third delay elements
  - ✓ The output will begin to lead the input when it goes below the designed operating frequency
- For comparison a clock signal of 100 MHz would require N = 127.27 (128)!

DSMD 800 MHz – 1.4 GHz Operating Range

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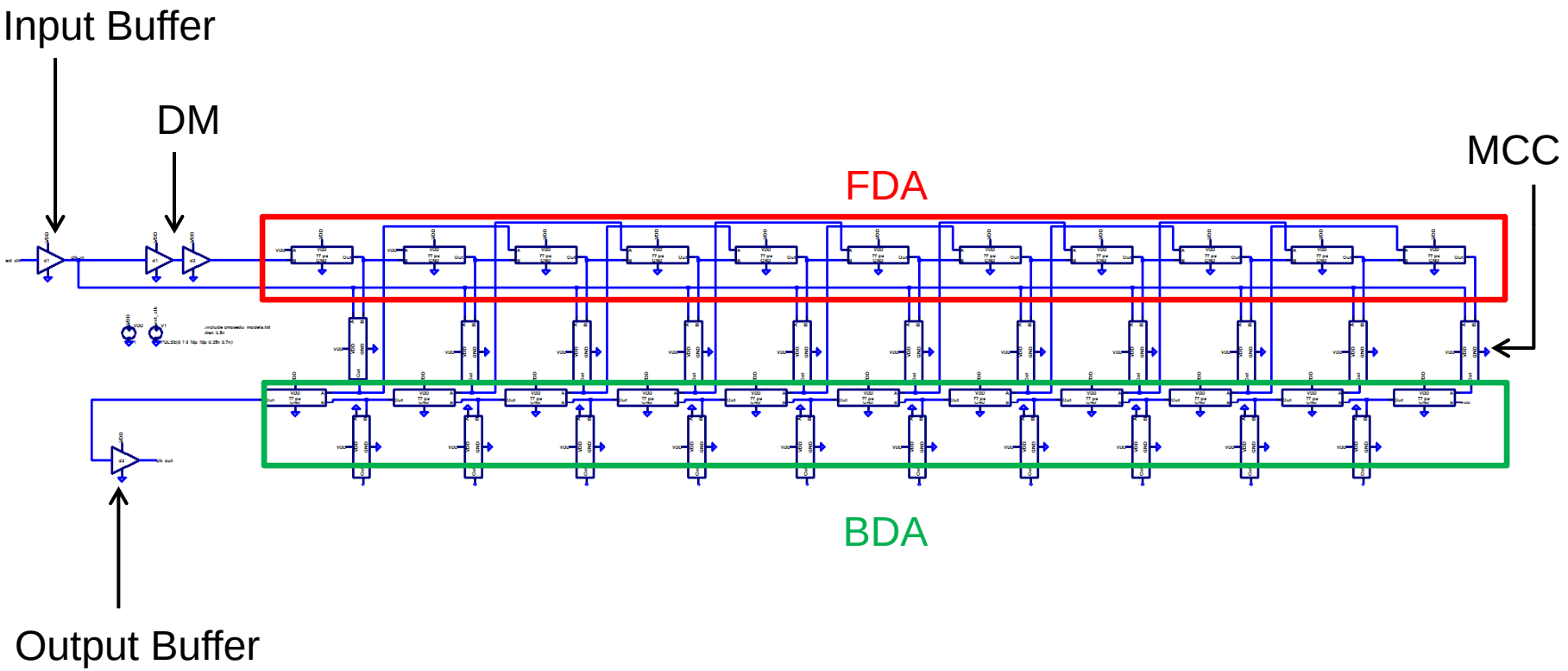

DSMD Simulation Results (800 MHz)

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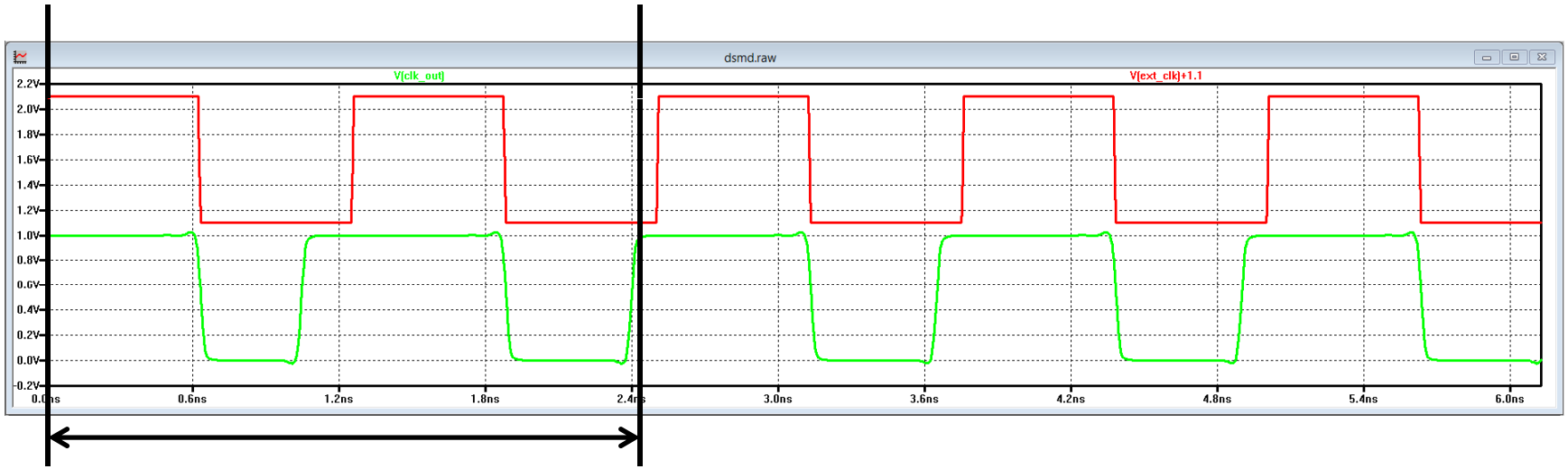

2 clock cycles

-107 ps phase error

DSMD Simulation Results (1 GHz)

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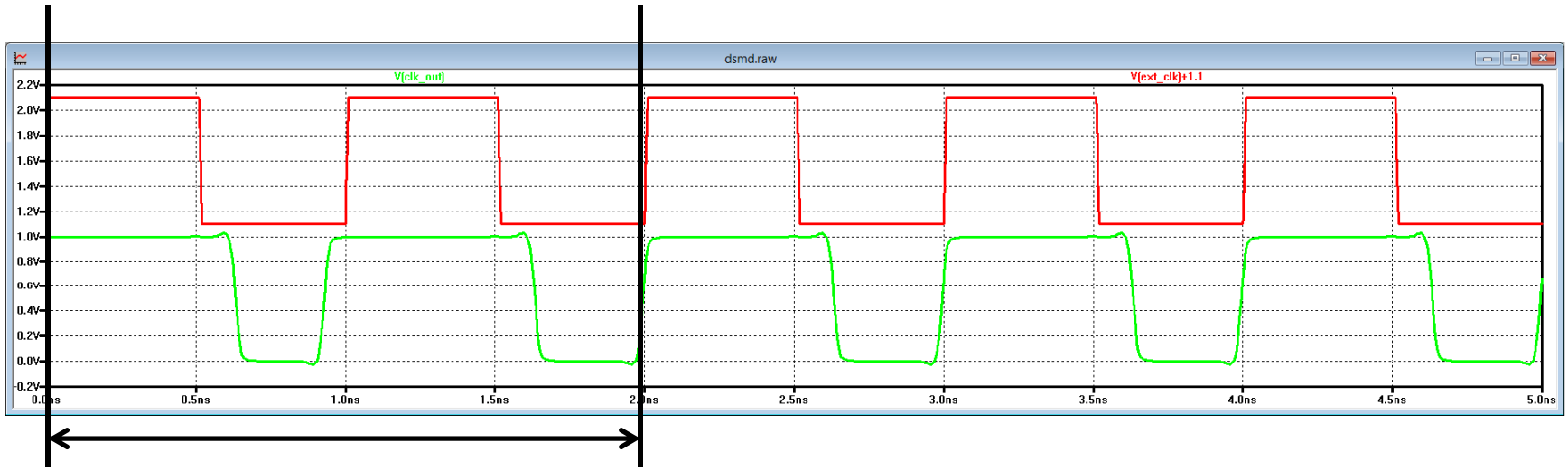

2 clock cycles

10 ps phase error

DSMD Simulation Results (1.25 GHz)

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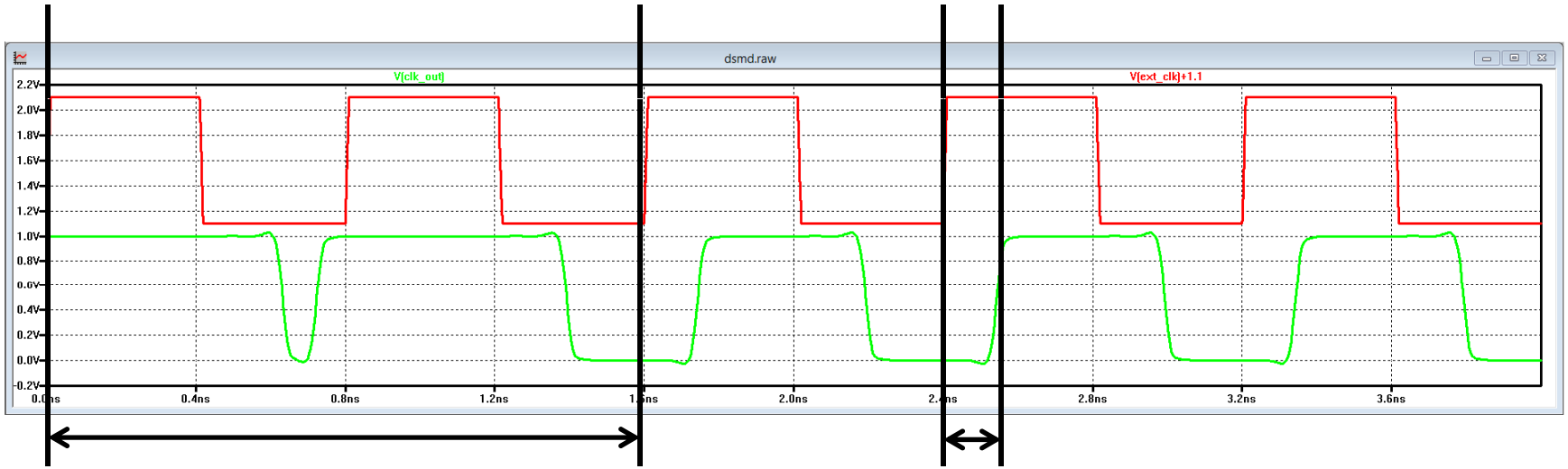

2 clock cycles

128 ps phase error

DSMD Simulation Results (1.43 GHz)

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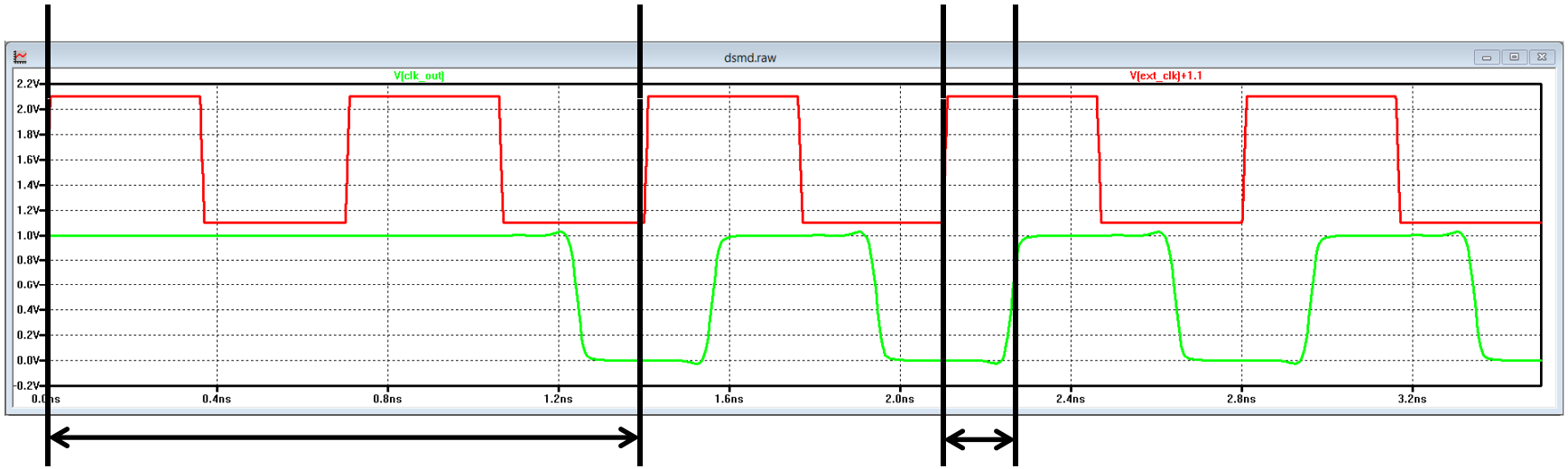

2 clock cycles

156 ps phase error

DSMD Advantages and Disadvantages

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Advantages

- Easy to design/understand
- Fixed duty cycle
- Fast clock generation and short recovery time
- Power consumption only occurs during switching
- Works well for higher clock frequencies if delay element has a small delay

Disadvantages

- Array size is proportional to clock period
  - Lower clock speeds require a large array
  - Fine phase characteristics required for best accuracy
- Introduces a phase quantization error

Analog Synchronous Mirror Delay

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- We will now focus on an implementation of an analog SMD (ASMD)
- The components of an ASMD are:
  - ✓ Input buffer
  - ✓ Delay monitor (DM)
  - ✓ Clock divider
  - ✓ Charge pump and comparator
  - ✓ Clock driver
- The circuit replicates the input clock using charge pumps to oscillate the input voltage to the comparators
- The rising edge of the internal clock will not coincide with the external clock

ASMD Input Buffer and Timing Diagram

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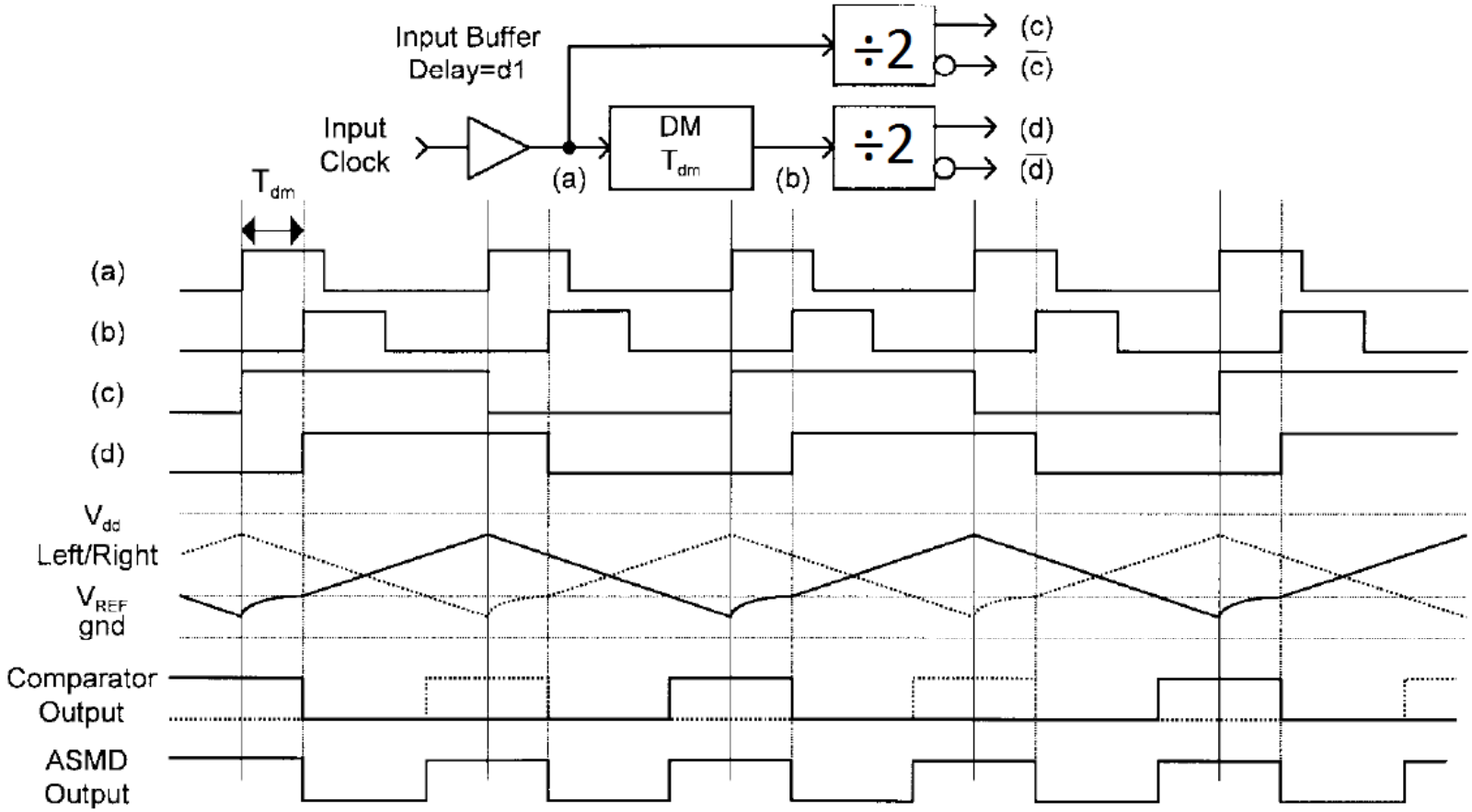

ASMD Charge Pump and Comparator

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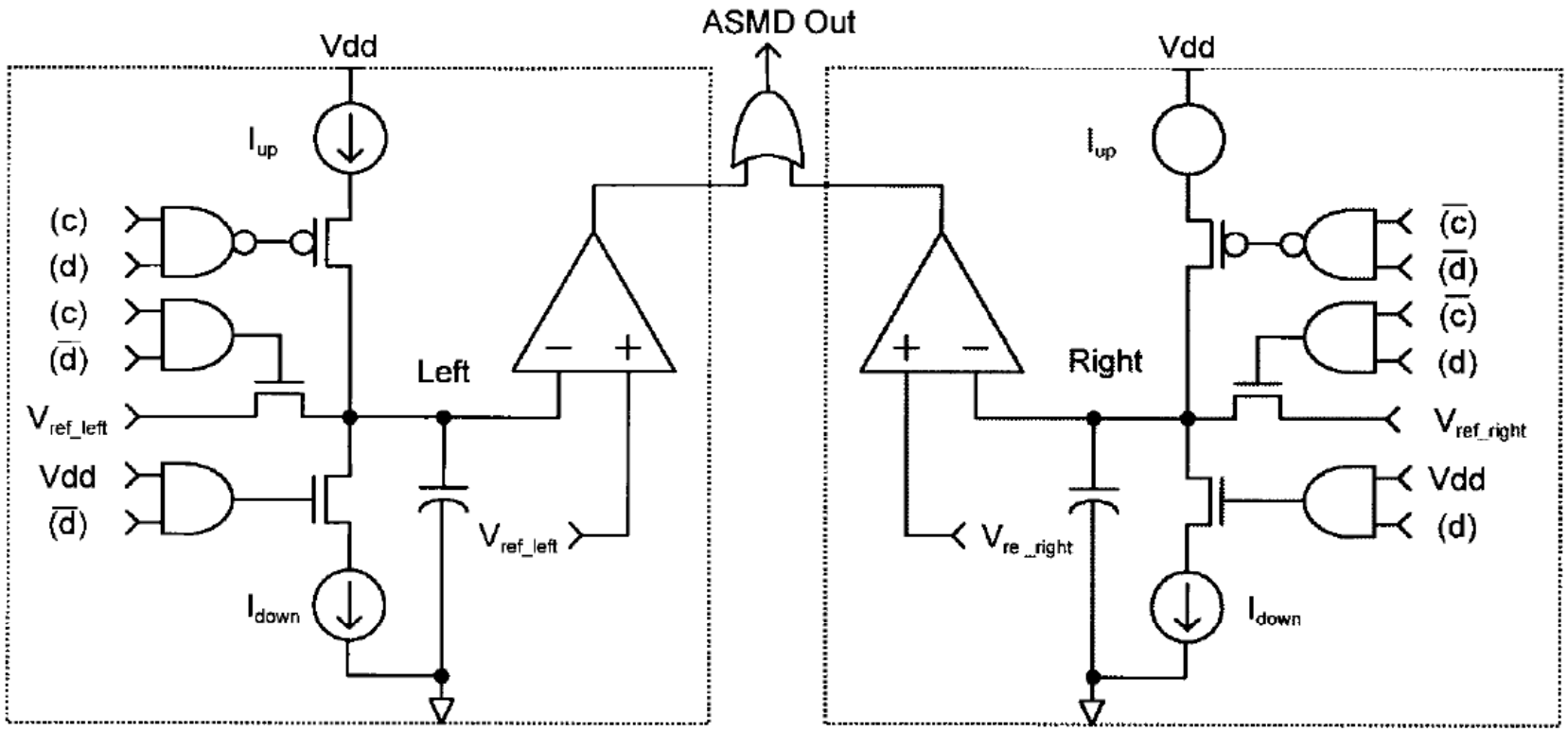

ASMD Calculations

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- Using a 10 μA supply current and designing for a minimum clock frequency of 100 MHz
  - ✓ $C = \frac{I_{pump} * T_{clk}}{VDD} = 100\ fF$
- During the period after the rising edge of the clock and before the signal has propagated through the DM (c = 1, d = 0)
  - ✓ $V_{left} = V_{ref}$
- After d goes high and before the falling edge of c (c = 1, d = 1) the capacitor charges at a rate of:
  - ✓ $\frac{dV}{dt} = \frac{I}{C} = \frac{100\ mV}{1\ ns}$
- When both control signals are low (c = 0, d = 0) the capacitor discharges at the same rate and measures the time it takes to cross V_{ref} and creates a pulse

ASMD Operation

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- It is clear from the schematic that when the charge pump causes the negative terminal of the comparator to drop below the reference voltage the output will go high
- A second circuit with the complemented signals connected to the control logic will cause a similar behavior 180° out of phase with the first signal.
- Using an OR gate we can replicate the input clock from these two signals.
- A major challenge with this architecture is matching the output duty cycle. If the pumping currents do not match exactly the duty cycle will change every clock period.

ASMD 100 MHz – 250 MHz Operating Range

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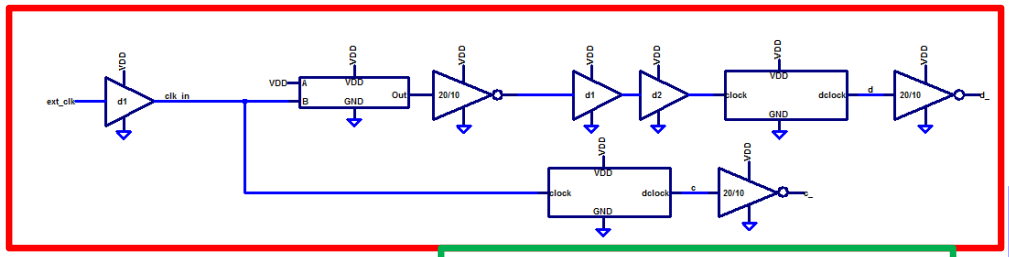
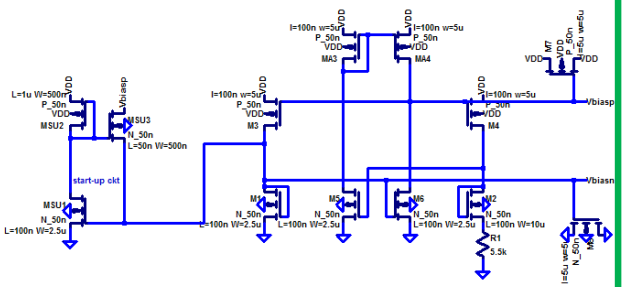
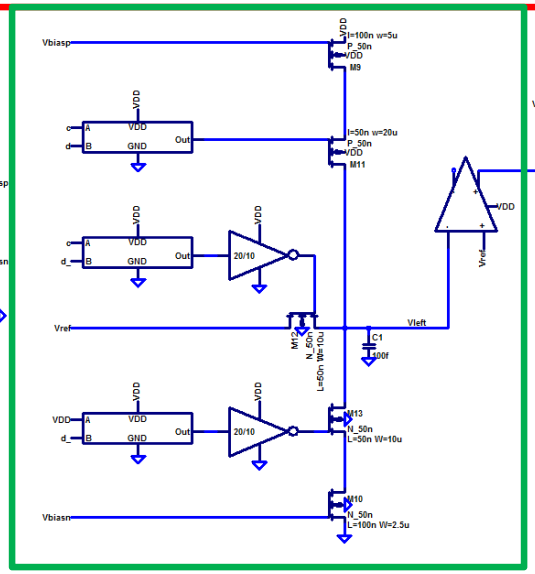
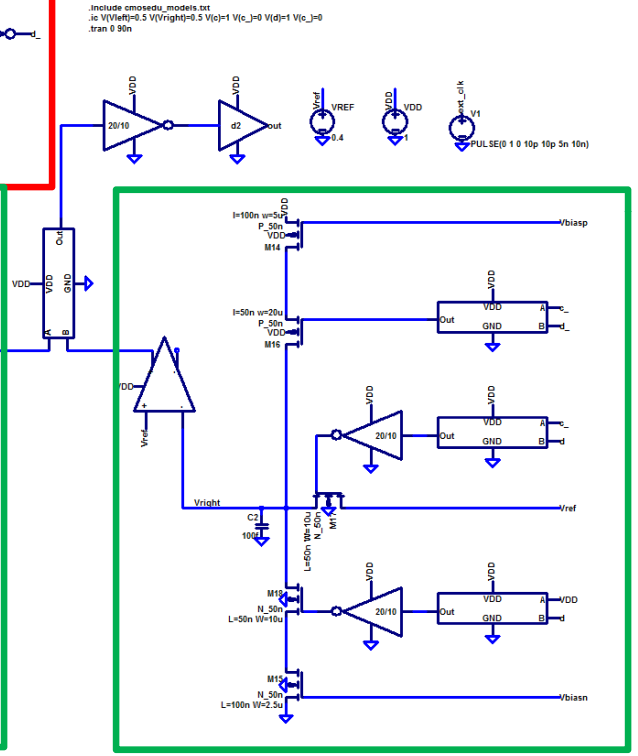
Input Buffer and Clock Divider





Bias and startup circuit





Charge Pumps

ASMD Simulation Results (100 MHz)

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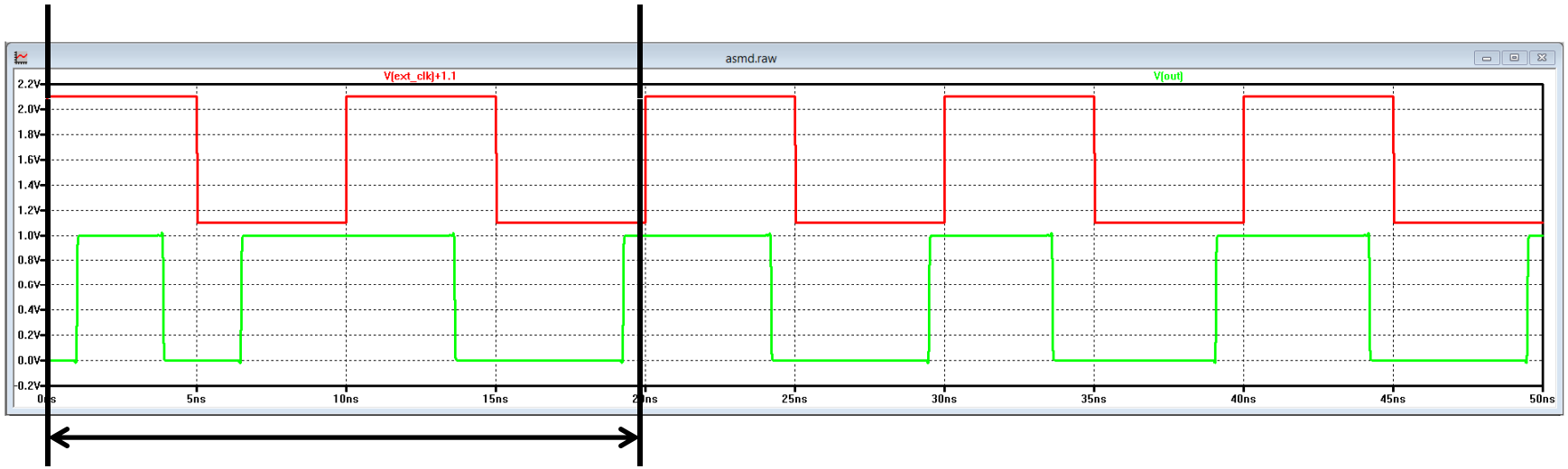

2 clock cycles

420 ps jitter

ASMD Simulation Results (160 MHz)

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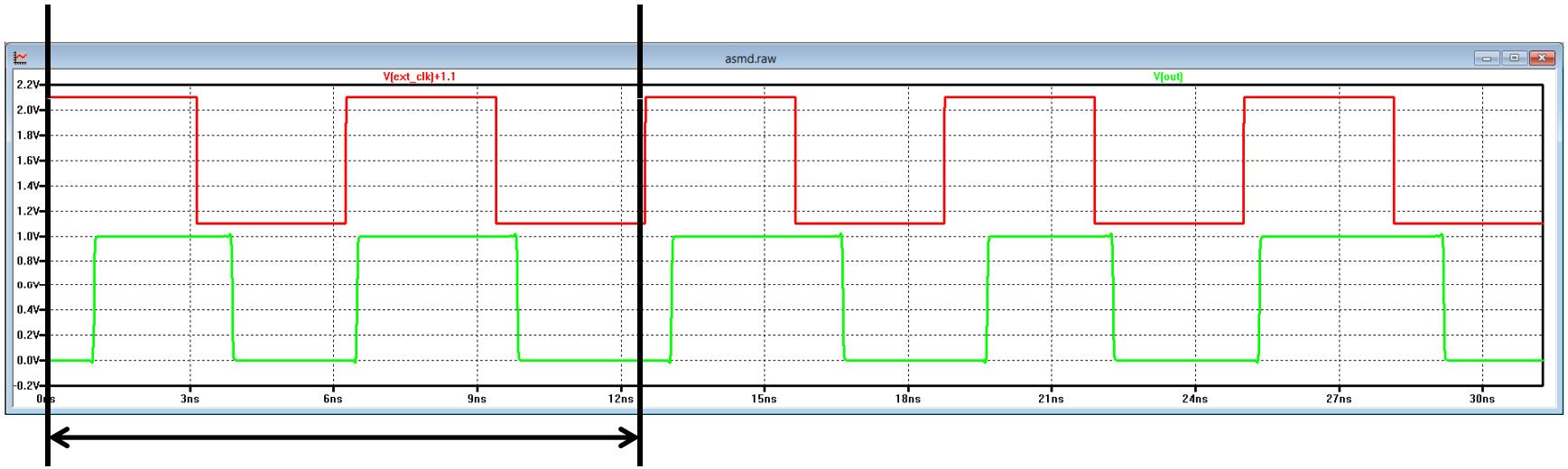

2 clock cycles

560 ps jitter

ASMD Simulation Results (200 MHz)

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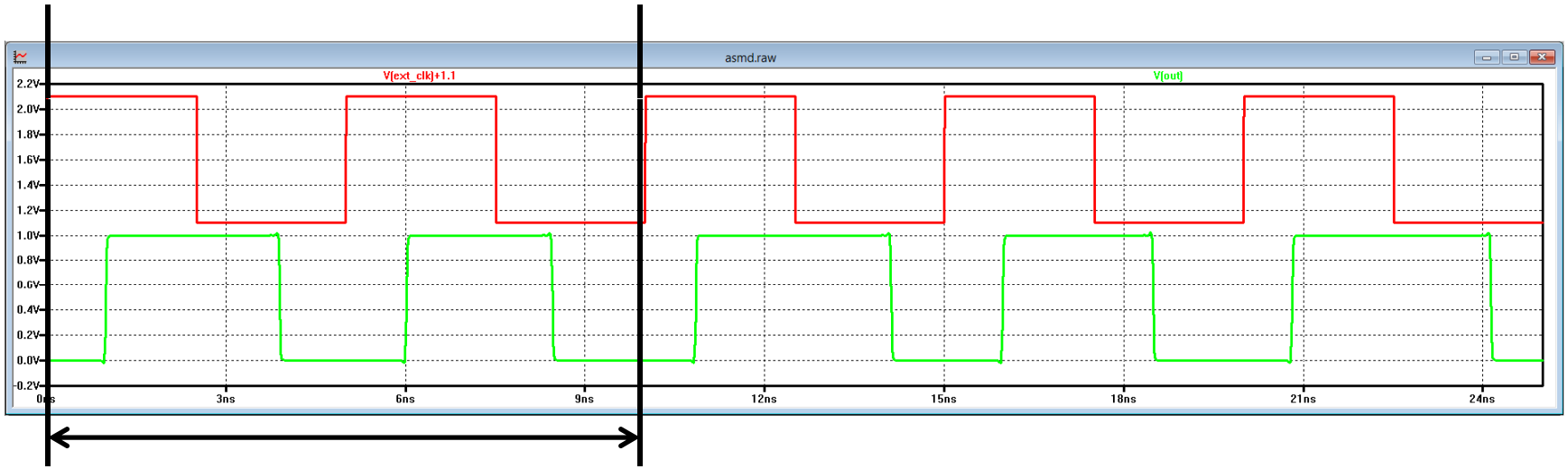

2 clock cycles

150 ps jitter

ASMD Simulation Results (250 MHz)

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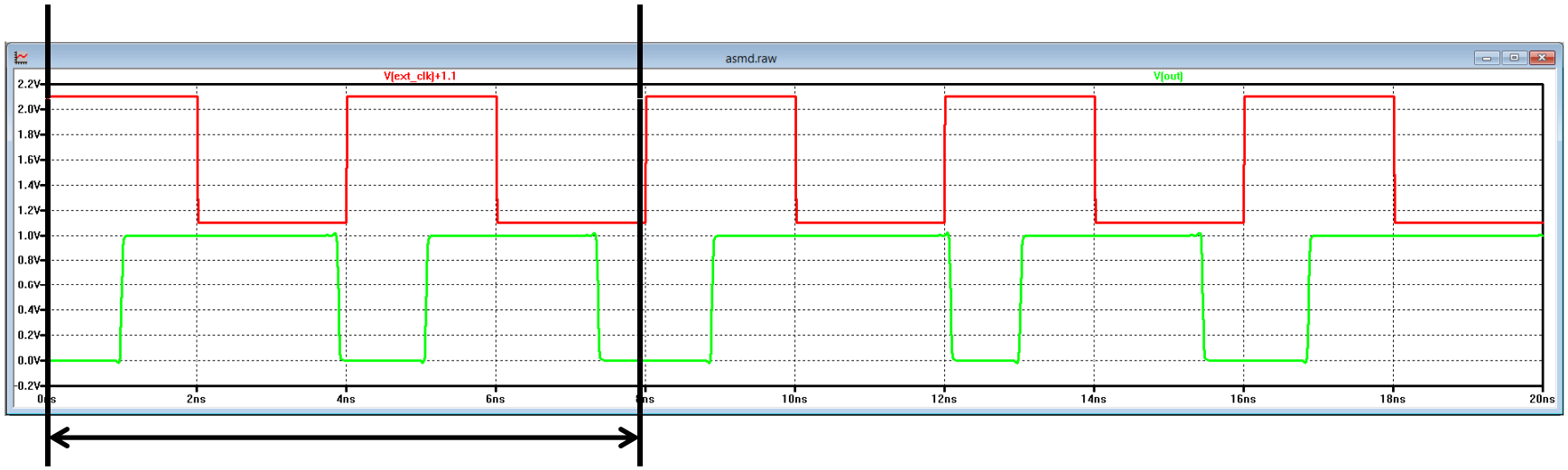

2 clock cycles

330 ps jitter

Improved ASMD Design

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- Clearly this ASMD design is not practical nor useful
- There are four apparent problems with the ASMD shown
  - ✓ Duty cycle dependence on V_{ref}
  - ✓ The up and down pumping mismatch
  - ✓ The circuit doesn't lock to the clock edge well
  - ✓ The timing mismatch from the control signals and their complements
- Replacing the positive comparator terminal V_{ref} connection with a second complemented pumping structure will cancel out the current mismatch for the comparator
  - ✓

$$\Delta t_{\text{dual}} = \frac{(\Delta\alpha + \Delta\beta) \cdot \{T_{\text{CLK}} - T_{\text{dm}}\}}{(\alpha + \beta + \Delta\alpha + \Delta\beta)}$$

$$\Delta t_{\text{single}} = \frac{(\beta + \Delta\beta - \alpha) \cdot \{T_{\text{CLK}} - T_{\text{dm}}\}}{(\beta + \Delta\beta)}$$

Improved ASMD Design

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- Adding a transmission gate to the true control signals will improve the timing matching for the true and complemented signals
- The capacitance on the comparator inputs will also need to be increased slightly
- Layout size and power consumption increase, tradeoff for improved performance

Comparator Pump Timing Comparison

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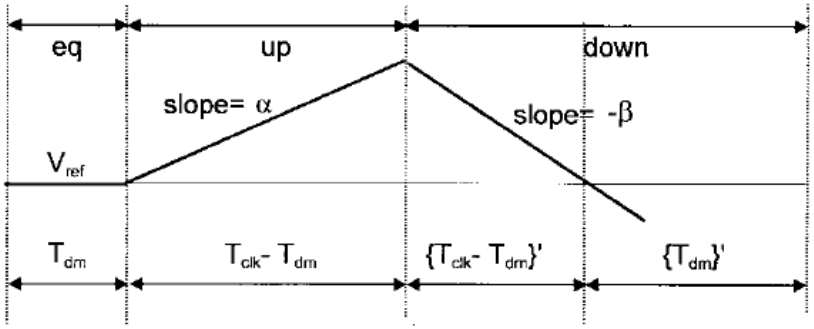

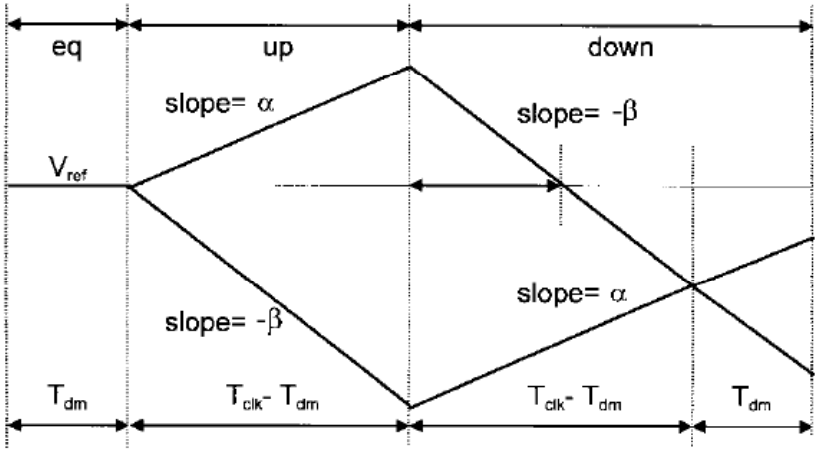

ASMD 100 MHz – 250 MHz Operating Range with Dual Pumping Scheme and TG Delay

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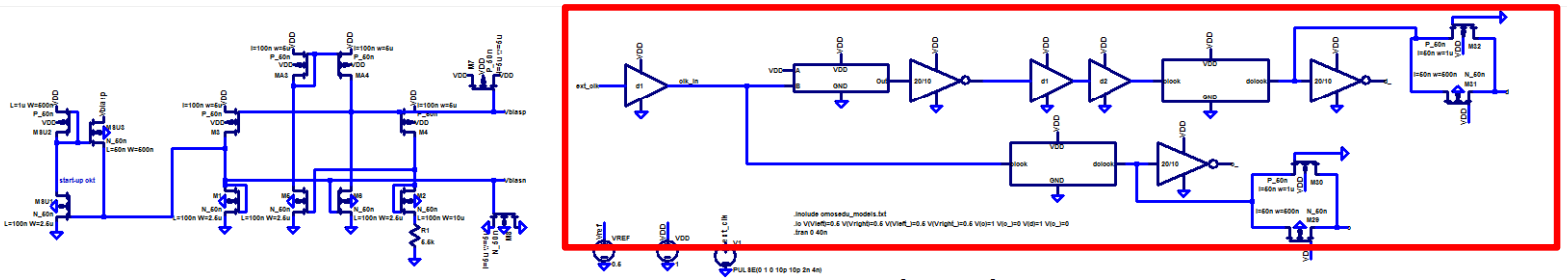
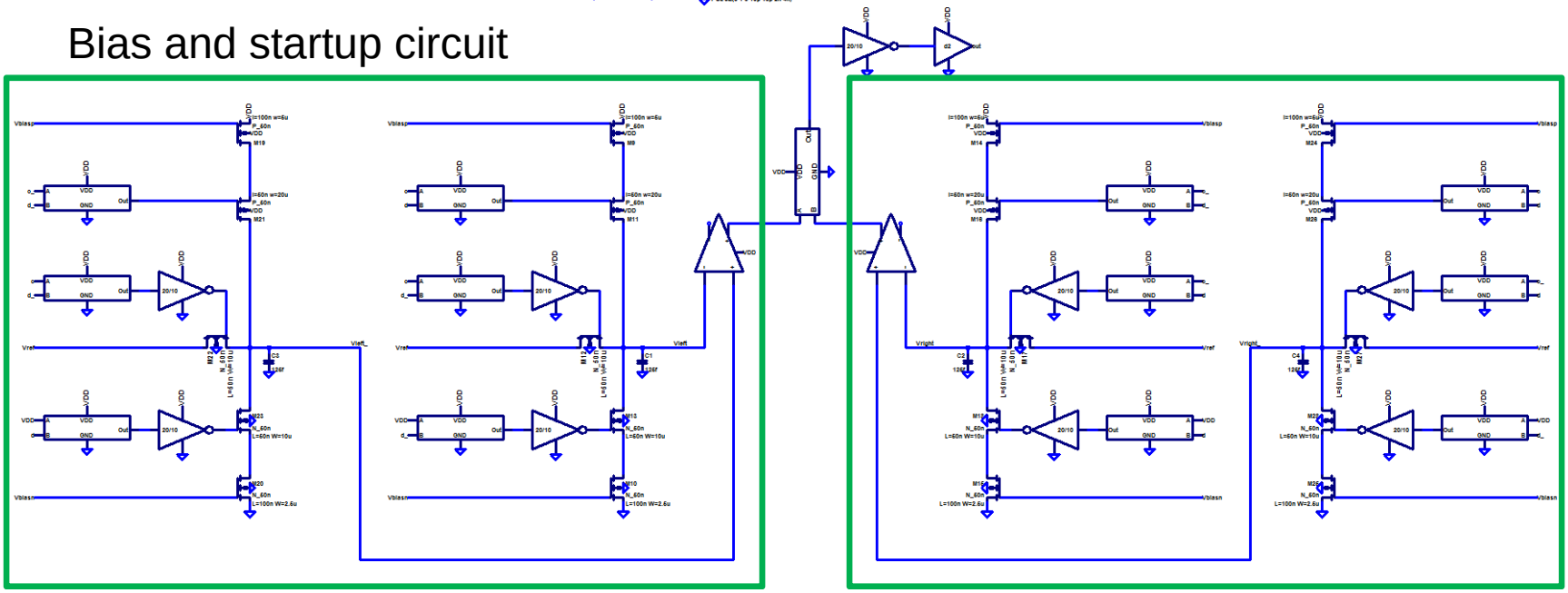
Input Buffer and Clock Divider



Bias and startup circuit



Charge Pumps

ASMD Simulation Results (100 MHz)

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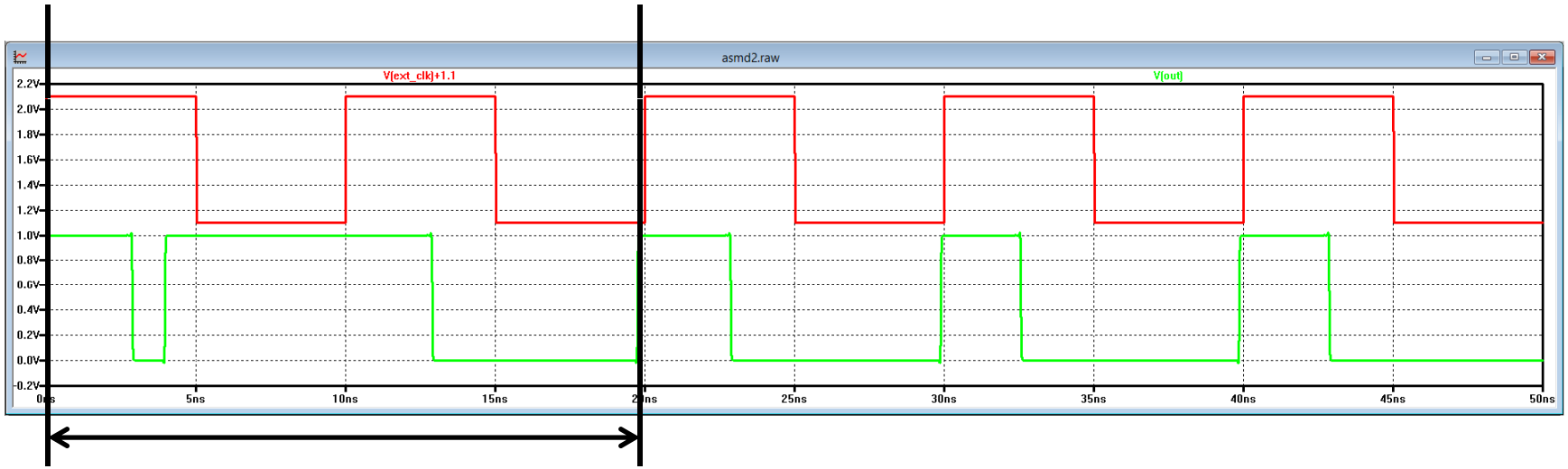

2 clock cycles

110 ps jitter

ASMD Simulation Results (160 MHz)

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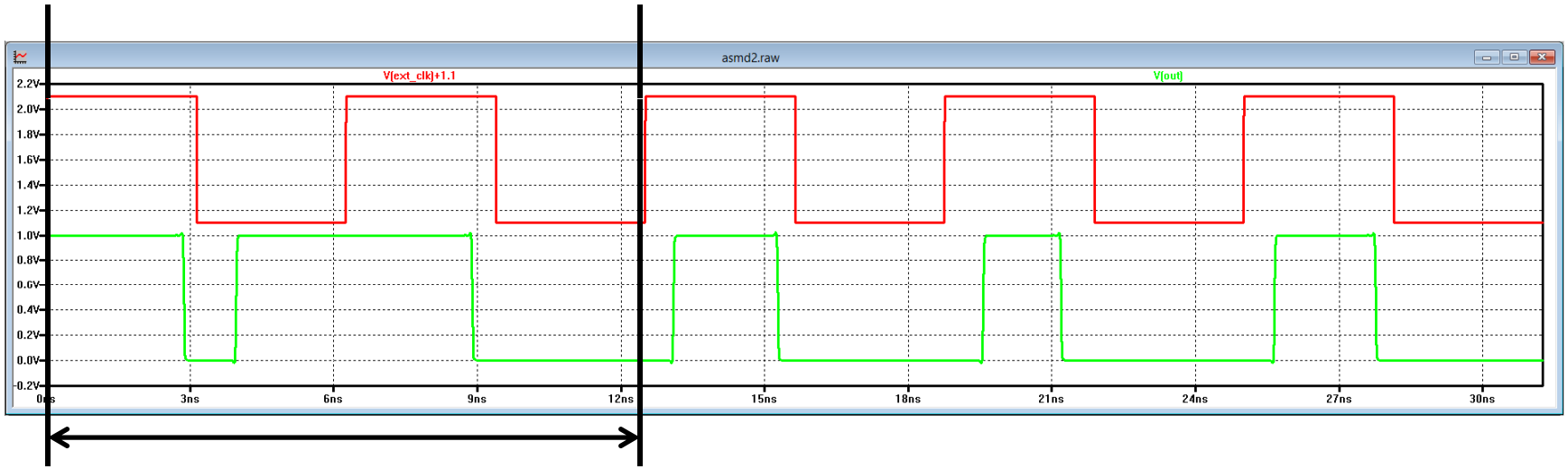

2 clock cycles

160 ps jitter

ASMD Simulation Results (200 MHz)

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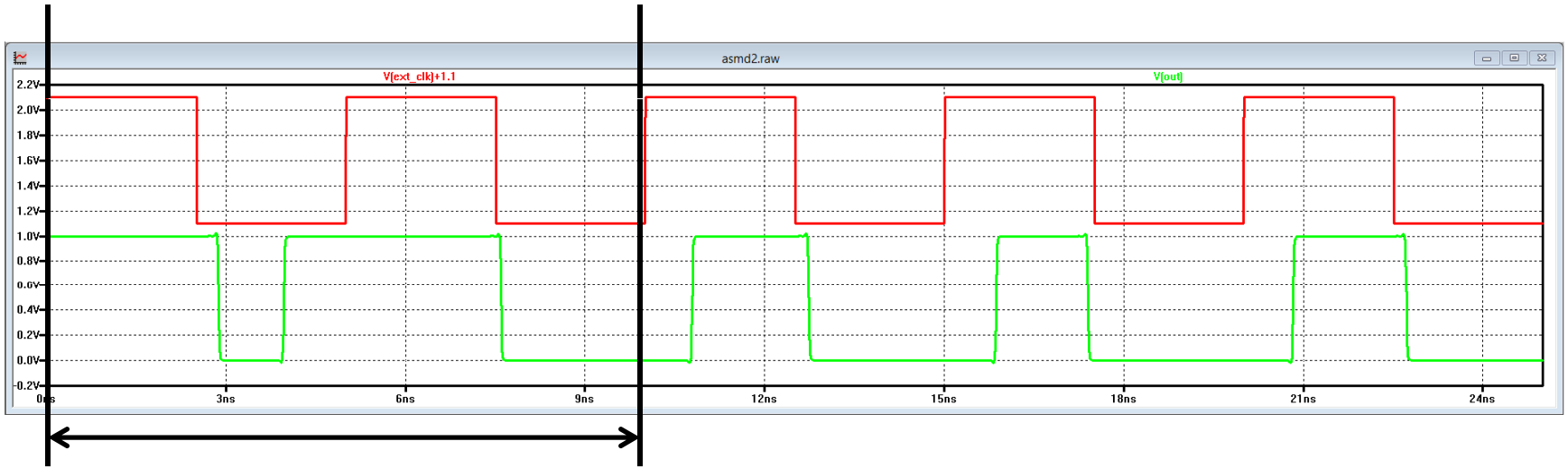

2 clock cycles

40 ps jitter

ASMD Simulation Results (250 MHz)

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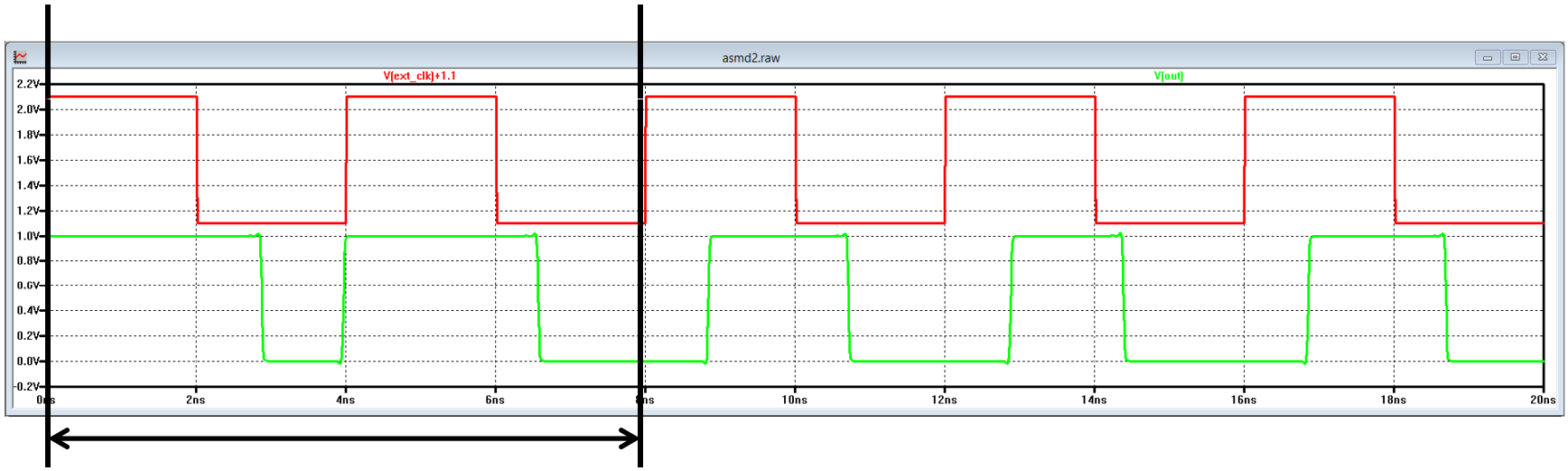

2 clock cycles

20 ps jitter

Comparison of Single/Dual Pump ASMD

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- The clock edge is now reliable (however the phase skew increases with frequency due to the internal delay of the comparator and pumping circuit)
- Jitter is greatly reduced
- Duty cycle mismatch is reduced
- Power consumption is increased
- Layout size is increased

ASMD Advantages and Disadvantages

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Advantages

- No delay array with a size dependency on clock period
- Fast clock generation and short recovery time
- Phase error is (ideally) zero
  - ✓ Due to the non-ideal nature of real circuits it is actually proportional to clock frequency
- Functions well at lower clock speeds

Disadvantages

- Requires a bias circuit
- Constantly consumes power (comparator and bias circuit)
- Duty cycle is modulated based on pump current and timing mismatches
- Some jitter is introduced due to timing mismatches

References

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- [1] Saeki, T. et al, "A Direct-Skew-Detect Synchronous Mirror Delay for Application-Specific Integrated Circuits," IEEE Journal of Solid-State Circuits, Vol. 34, pp. 372 – 379, Mar. 1999.
- [2] Shim, D. et al, "An Analog Synchronous Mirror Delay for High-Speed DRAM Application," IEEE Journal of Solid-State Circuits, Vol. 34, pp. 484 – 493, Apr. 1999.
- [3] Saeki, T. et al, "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay" IEEE Journal of Solid-State Circuits, Vol. 31, pp. 1656 – 1668, Nov. 1996.
- [4] Baker, R. Jacob, "CMOS Circuit Design, Layout and Simulation," 3rd edition, John Wiley & Sons, 2010.