A TUTORIAL APPROACH TO ANALOG PHASE-LOCKED LOOPS

By Angsuman Roy
Presentations Outline

- Introduction and Terminology
- Analog PLLs
- Phase Detector (Mixer)
- Voltage-Controlled Oscillator
- Low-Pass Filter and Damping
- Applications
  - Frequency Synthesis
  - FM Demodulation
INTRODUCTION

Basic Structure of a PLL:

- Reference Signal
- Phase Detector
- Low-Pass Filter
- VCO
- Output Signal
TERMINOLOGY

Analog PLL (APLL)
- Multiplying circuit (mixer) used for phase detector
- Other components are analog

Digital PLL (DPLL)
- Mixer replaced with XOR gate or phase frequency detector (PFD)
- Other components are unchanged

All Digital PLL (ADPLL)
- XOR Gate or PFD
- Other components are digital or numerically controlled.
WHY ANALOG PLLS?

- Used for RF Circuits
- Wide Tuning Range
- Low Noise
- Many Adjustable Parameters
Basic Structure of a PLL
WHAT IS A MIXER?

A mixer takes two input frequencies and outputs their sum and difference from the process of multiplication.
\[ V_1(t) = A_1 \cdot \sin(2\pi f_1 \cdot t) \]
\[ V_2(t) = A_2 \cdot \sin(2\pi f_2 \cdot t) \]
\[ V_1(t) \cdot V_2(t) = \sin(2\pi f_1 \cdot t) \cdot \sin(2\pi f_2 \cdot t) \]

**Trigonometric Identity:**
\[ \sin(a) \cdot \sin(b) = \frac{1}{2} [\cos(a - b) - \cos(a + b)] \]

\[ V_1(t) \cdot V_2(t) = \frac{1}{2} (A_1 \cdot A_2) \cdot [\cos(2\pi (f_1 - f_2) t) - \cos(2\pi (f_1 + f_2) t)] \]

\[ \underline{\text{Difference}} \quad \underline{\text{Sum}} \]
Mixer Design: 4 Quadrant Multiplier
4 QUADRANT MULTIPLIER DEVICE SIZES

1.8u/0.6u min size devices for speed

6u/0.6u for current sinking ability
Output voltage is developed across these resistors
AC OPERATION OF THE MIXER

Differential sine input with bias voltage represents RF input of 100 MHz

Same, but LO input of 10 MHz
TIME DOMAIN VIEW OF INPUTS/OUTPUT

- $V(\text{id1, id2})$
- $V(\text{rf1} - V(\text{rf2})$
- $V(\text{lo1} - V(\text{lo2})$

Time range: 24.99µs to 25.32µs
FFT OF IF OUTPUT

Difference frequency: 90 MHz
Sum frequency: 110 MHz

SFDR=70dB
GAIN AND NOISE

12 dB Loss

Loss is bad for most applications

Difference between noise floors is added noise or noise figure (NF) = 5 dB
Network to allow for sweeping differential voltages while keeping a fixed bias.

```
.include C5_models.txt
.dc V_RF -1 1 V_LO -1 1 0.5
```
4 QUADRANT MULTIPLIER GAIN

Linear only for small signals
4 QUADRANT MULTIPLIER GAIN

Changed sweep and step settings to show linear region better

*Check polarity of sources and change if needed*

$V_{RF} \text{ -0.25V to 0.25V}$

$V_{Lo}=0.2$

-0.2

0.1

0.2
Point A: \( K \times (0.1V \times 0.1V) = 0.02V \) \( \rightarrow \) \( K=2 \)
Point A: \( K \times (0.1V \times -0.2V) = -0.05V \) \( \rightarrow \) \( K=2.5 \)
Point C: \( K \times (0.15V \times -0.2V) = -0.075V \) \( \rightarrow \) \( K=2.5 \)
Increasing the value of these resistors increases gain but reduces load driving ability.

Increasing the bias voltage increases gain and allows for variable gain.
REPLACING RESISTORS

Resistors can be replaced with long L MOSFETs

1.8u/18u
When both RF and LO frequencies are the same, the mixer operates as a phase detector.

Simulation test set-up
IF output is rectified at twice the RF/LO frequency. Averaging this will result in some DC value.
There is a relationship between average IF voltage and phase between LO and RF.
FILTERING THE IF OUTPUT

Capacitor to filter IF output

IF output is now a DC value
Output Voltage as a Function of Phase

100 MHz RF/LO

\[ K_{PD} = \frac{0.12V}{\pi} \]
Output Voltage as a Function of Phase

- Output Voltage in mV
- Phase in Degrees

Graph shows a peak in output voltage at a certain phase, with a noted slope of 0.3 mV/deg.
Many options to choose from
- Ring oscillators
- Relaxation oscillators
- Varactor-tuned LC oscillators

Requirements are
- Relatively linear
- Has the tuning range needed for the intended application
DIFFERENTIAL RING OSCILLATOR

Same idea as a ring oscillator made from inverters but with differential amplifiers.
Current mirror loads (3.6u/0.6u)

Current sets delay

Output

Diff pairs (1.8u/0.6u)

White noise source for simulation

Current mirrors (3.6u/0.6u)
Problem: Odd output waveform shape

Problem: Output does not swing to full logic levels

Solution

Level Shifting: Need to shift the center of the output to $\frac{1}{2}$ VDD so inverters switch in the middle of the waveform.

Pulse Shaping: Inverter string is needed to provide full logic levels and sharpen the pulses.
LEVEL-SHIFTING

Level shifter with long L MOSFETs

Can also use resistors
INVERTER STRING

Small inverter for low capacitive loading

Big inverter for load driving ability

Inverter sizes are PMOS Width/NMOS Width
RESULT

300 MHz

Sharp transitions with 50% duty cycle
FREQUENCY TESTING

Frequency as a Function of Current

Input Current in uA

Frequency in MHz

7 MHz/uA
This MOSFET and resistor serves as a rudimentary voltage to current converter.
Frequency as a Function of Voltage

- Frequency in MHz
- Voltage in V
- 90 MHz/V

Frequency Testing
Mixer output is differential while VCO input is single-ended.

Active load for differential to single ended conversion.
Loop filter with buffer to isolate effects from mixer output impedance.

Mixer needs proper biasing and input levels.
Isolating start-up transients
Edges line up
USEFUL EQUATIONS

\[ K_F = \frac{1}{1 + sRC} \]  
Loop filter transfer function (simple 1\textsuperscript{st} order lowpass)

\[ H(s) = \frac{\phi_{LO}}{\phi_{RF}} = \frac{K_{PD}K_{VCO} \cdot \frac{1}{1 + sRC}}{s + \frac{1}{N}K_{PD}K_{VCO} \cdot \frac{1}{1 + sRC}} \]  
System transfer function (2\textsuperscript{nd} order)

\[ \omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N \cdot RC}} \]  
Natural frequency

\[ \zeta = \frac{1}{2RC\omega_n} \]  
Damping ratio

N is for the divider ratio in frequency synthesis examples. If there is no divider use N=1.
Overdamped PLL not locking on a single frequency

FFT of output shows two peaks at 300 MHz and a noisy one at 291 MHz.

The difference is the natural frequency.
**UNDERDAMPED CASE**

VinVCO voltage shows some oscillation and ripple voltage.

FFT of output shows the correct peak at 300 MHz but there is significant phase noise.
VinVCO voltage settles and looks fairly random.

FFT of output shows the correct peak at 300 MHz with less noise.
Stable oscillator topologies don’t scale well to high frequencies.
- Quartz (32 KHz-160 MHz)
- Rubidium (typically 10 MHz)
- Silicon MEMS (1 MHz-140 MHz)

A PLL locked to a stable reference can generate a stable high frequency oscillator.
- Quartz (10 PPM)
- Silicon MEMS (100 PPM)
- Rubidium (0.0001 PPM or 0.1 PPB)
FREQUENCY DIVIDER

Each stage divides by 2

TSPC D-FF
FREQUENCY MULTIPLIER SCHEMATIC
APPLICATIONS: FM DEMODULATION

- **FM Modulator**: Provides differential input at correct amplitude.
- **Additional filtering to filter out VCO ripple**.
INPUTS AND OUTPUTS

- Filtered VCO input
- VCO input
- Original signal
REFERENCES

- The Art of Electronics by Horowitz and Hill
- MT-080 Mixers and Modulators by Analog Devices
- MT-086 Fundamentals of PLLs by Analog Devices
- Practical Tips for PLL Design by Dennis Fischette
- FM & PM Demodulation from The Scot’s Guide to Electronics
- Mixer Basics Primer by Christopher Marki