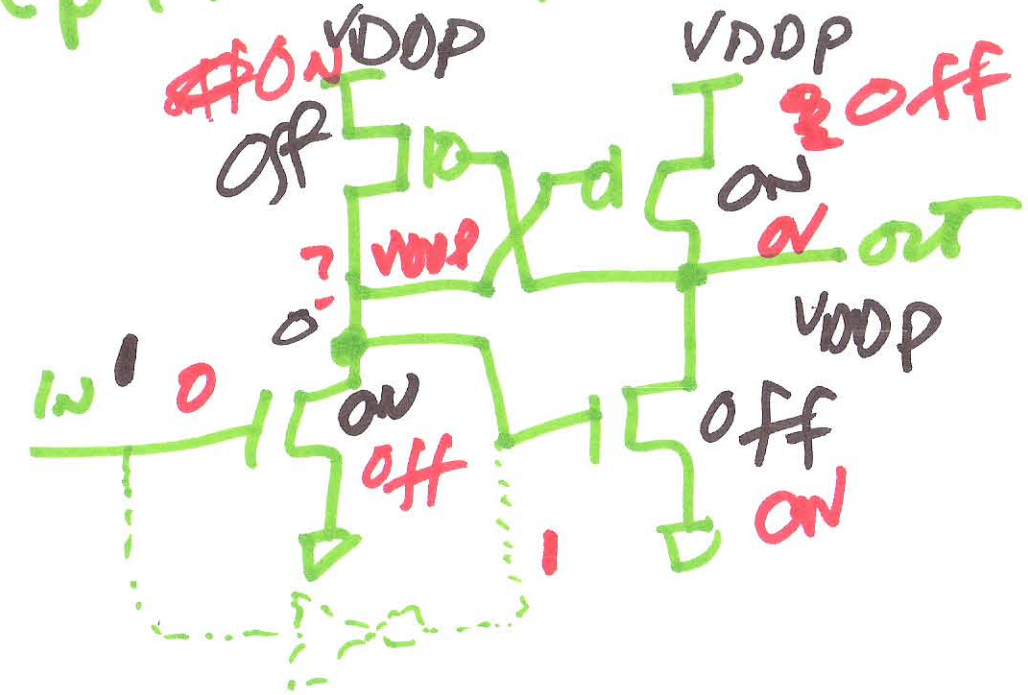
ECG 721

Memory Circuit Design

Sept. 21, 2015



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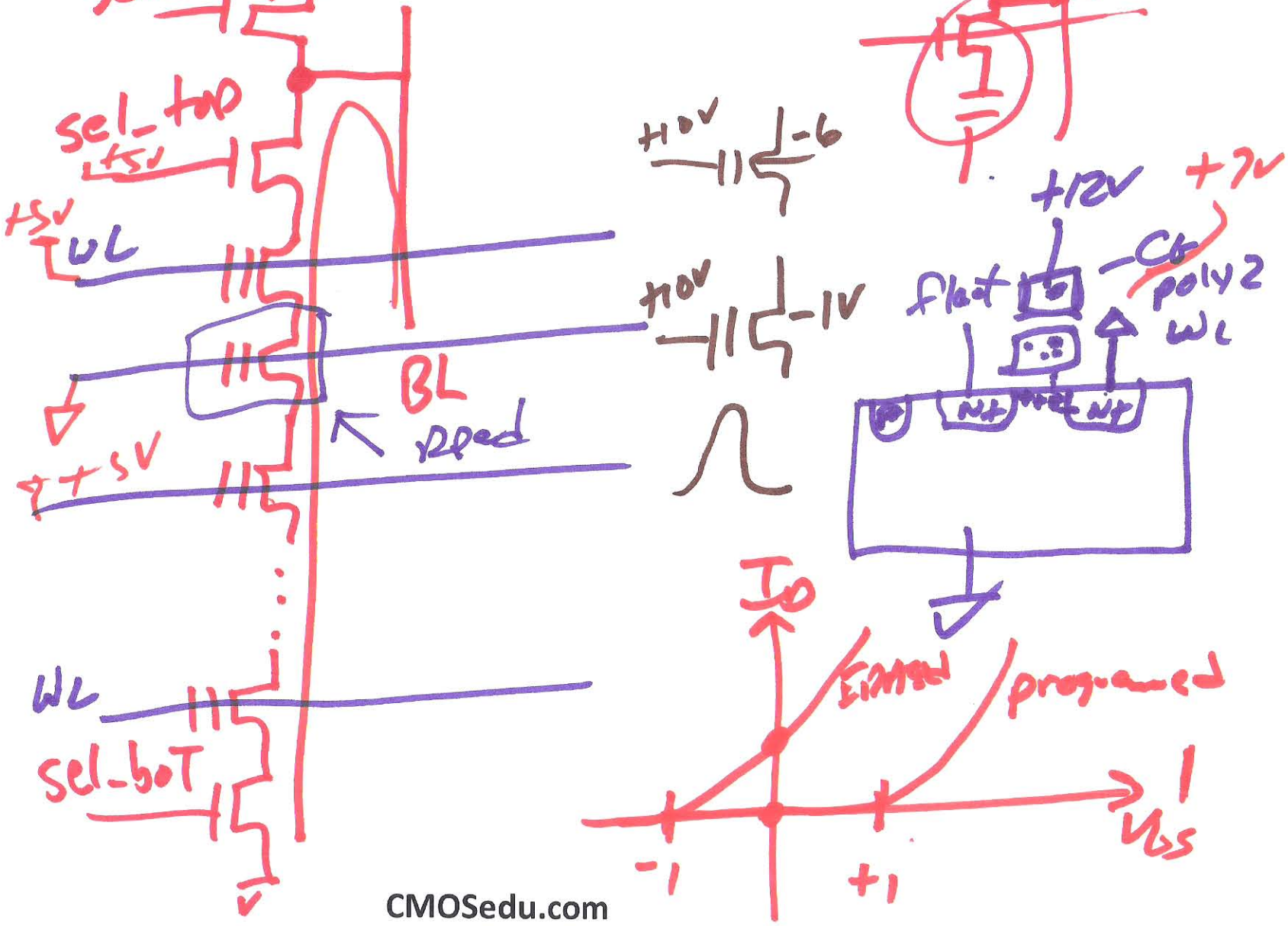
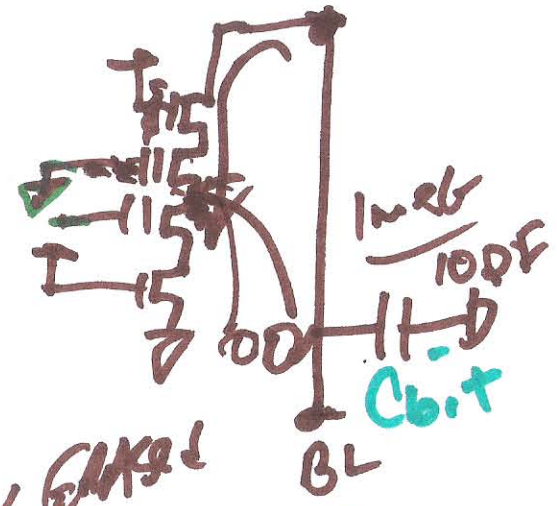
1)

Ch. 16 Review

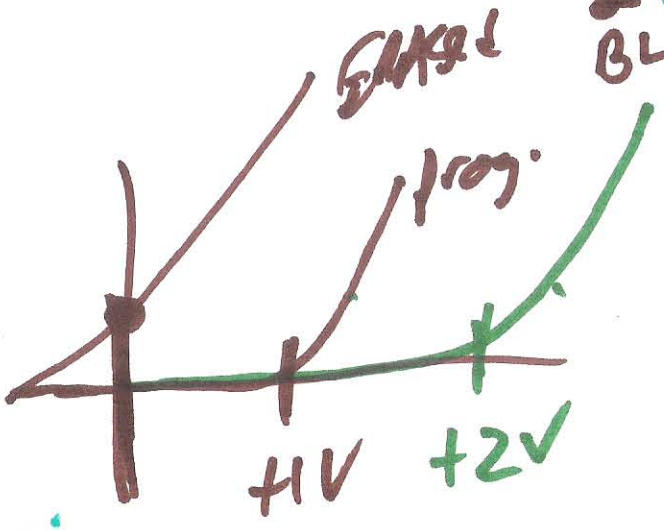
NAND Flash

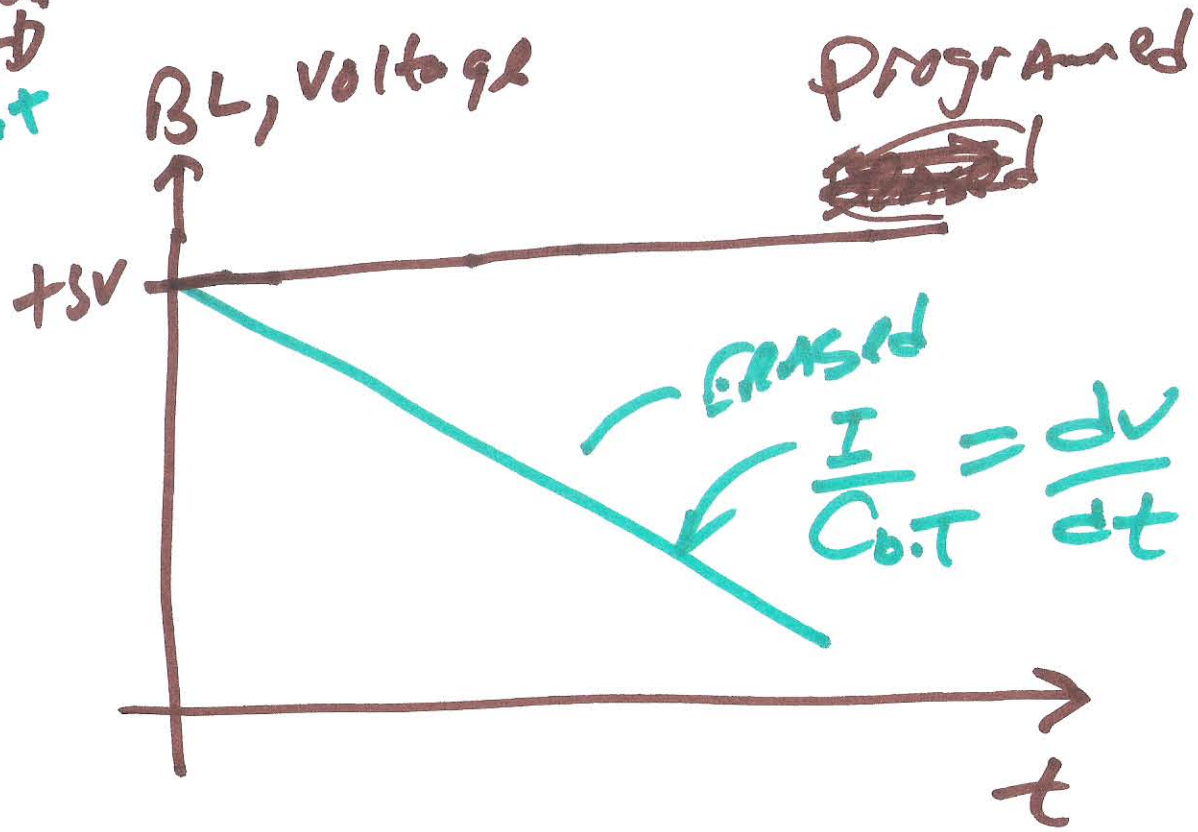




$I = C\frac{dv}{dt}$

$RC = 10^{4}\,s$

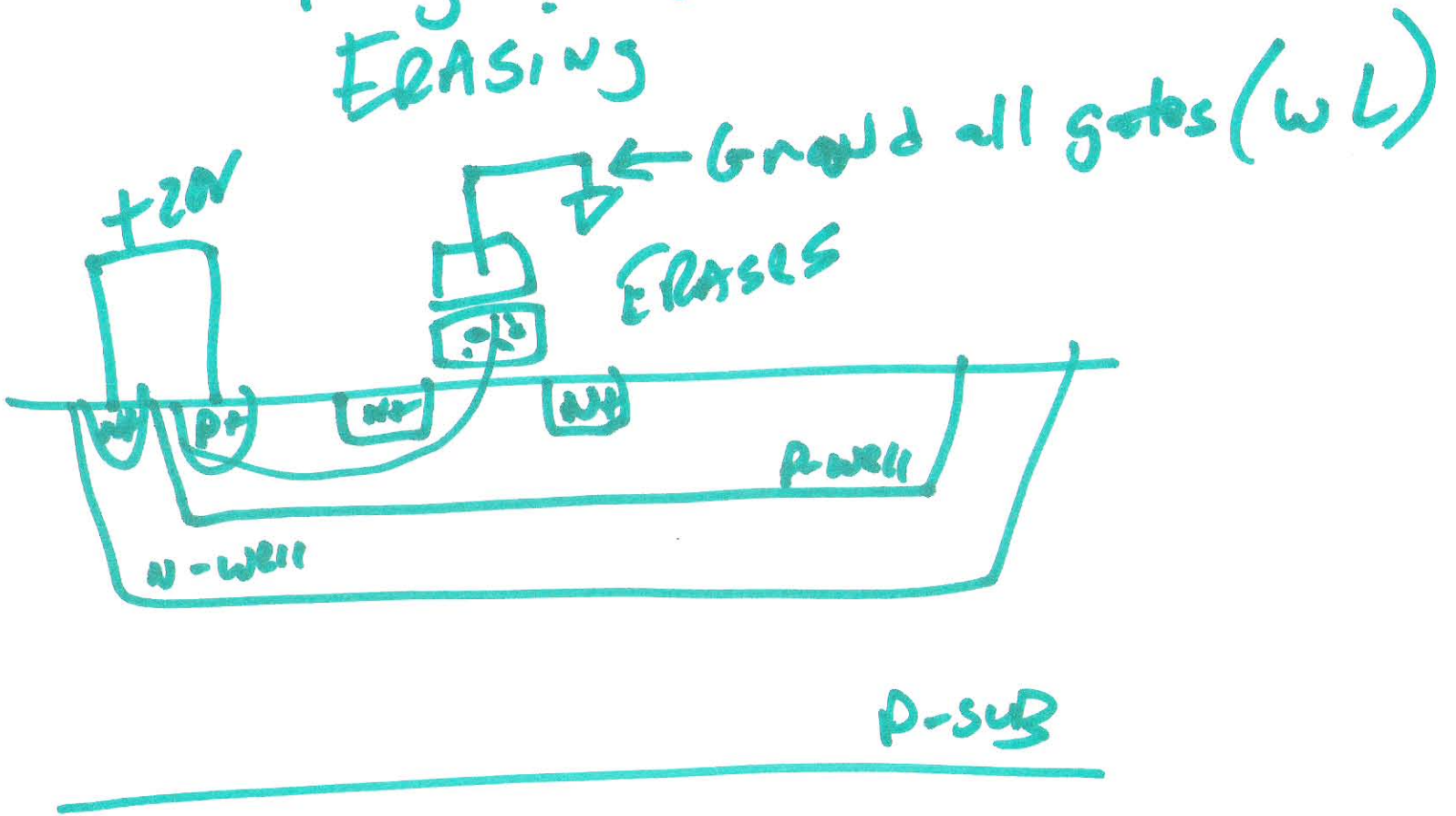


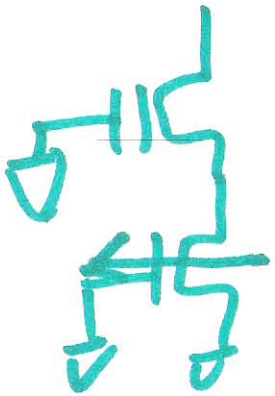


3)

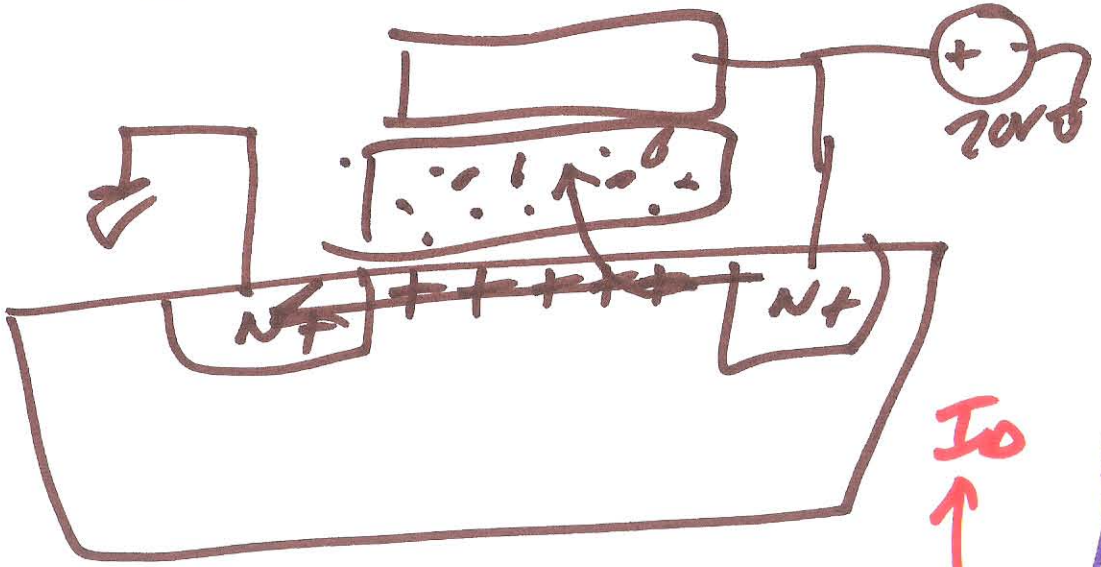
~~Programming~~ FNT

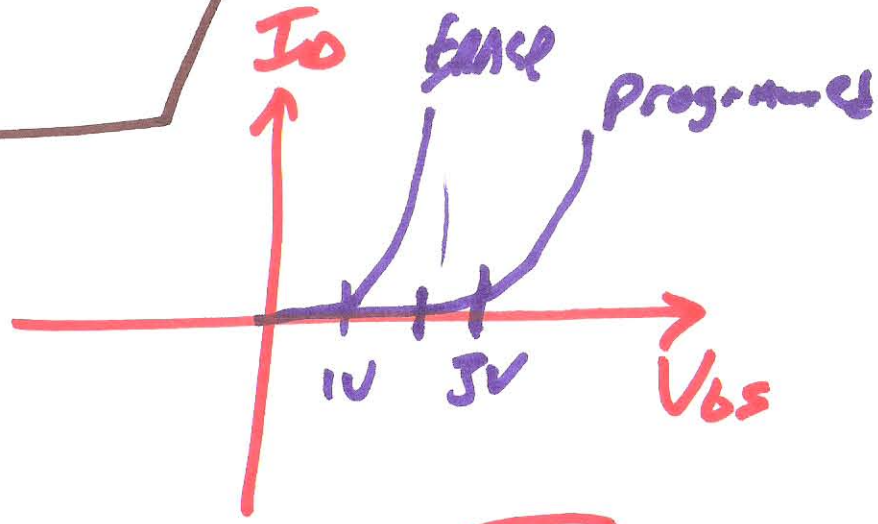
ERASING

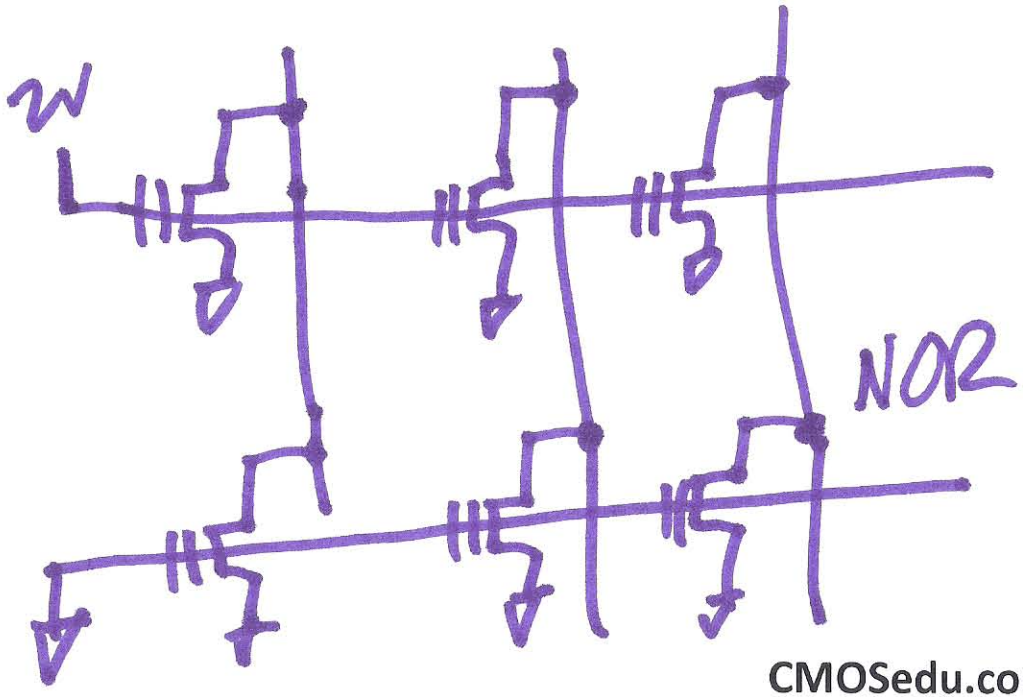


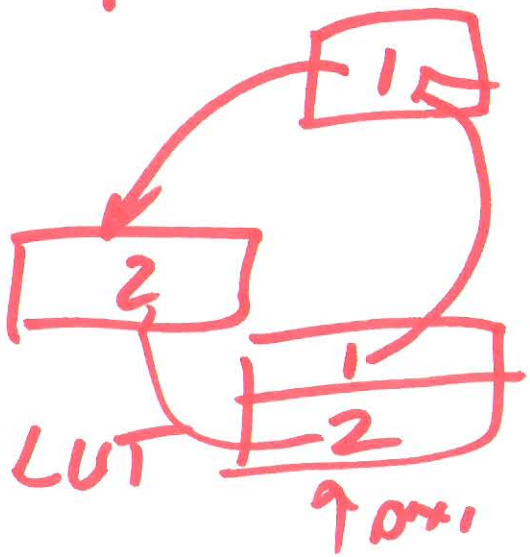


Channel Hot Electrons (CHE)



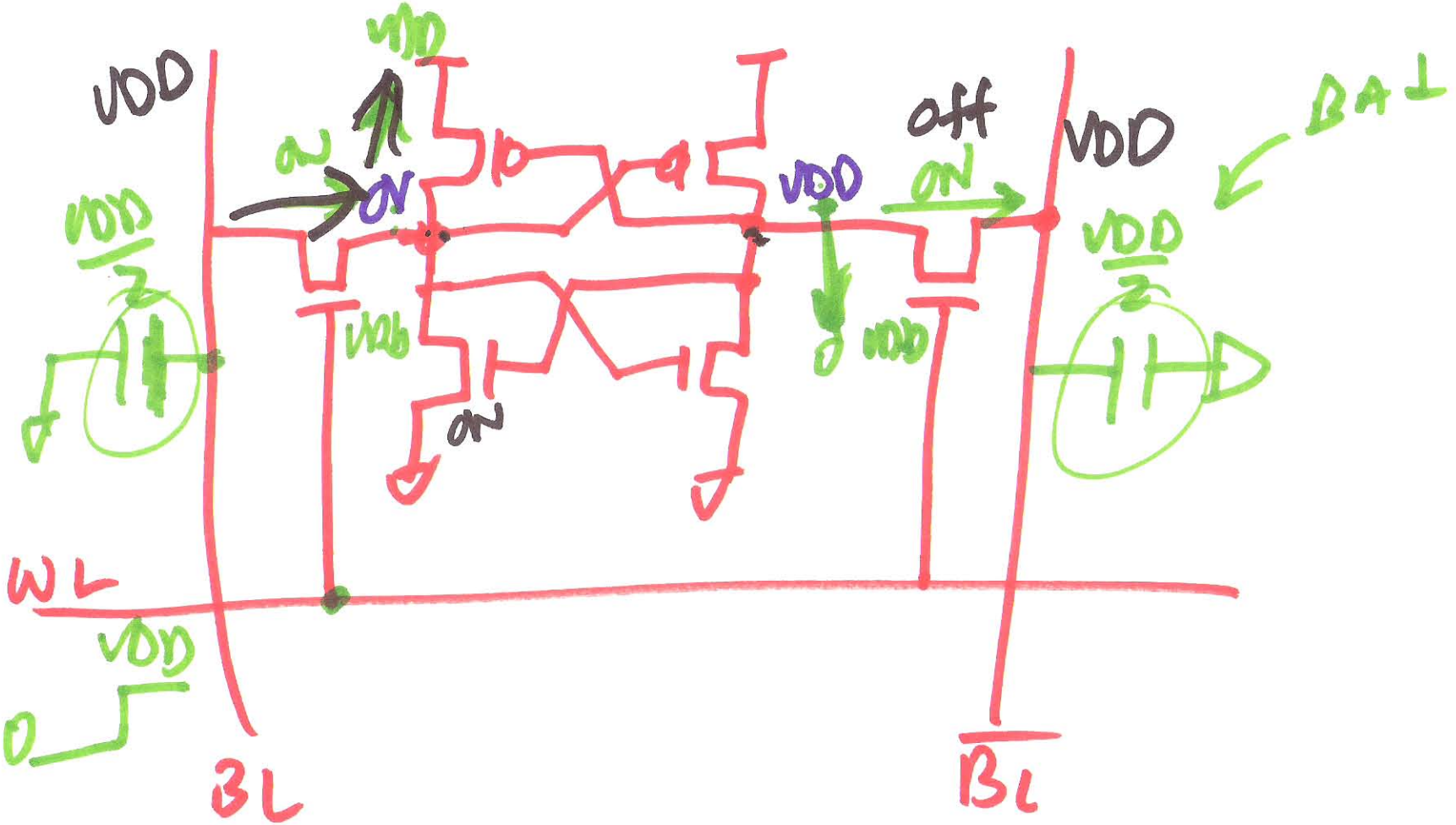






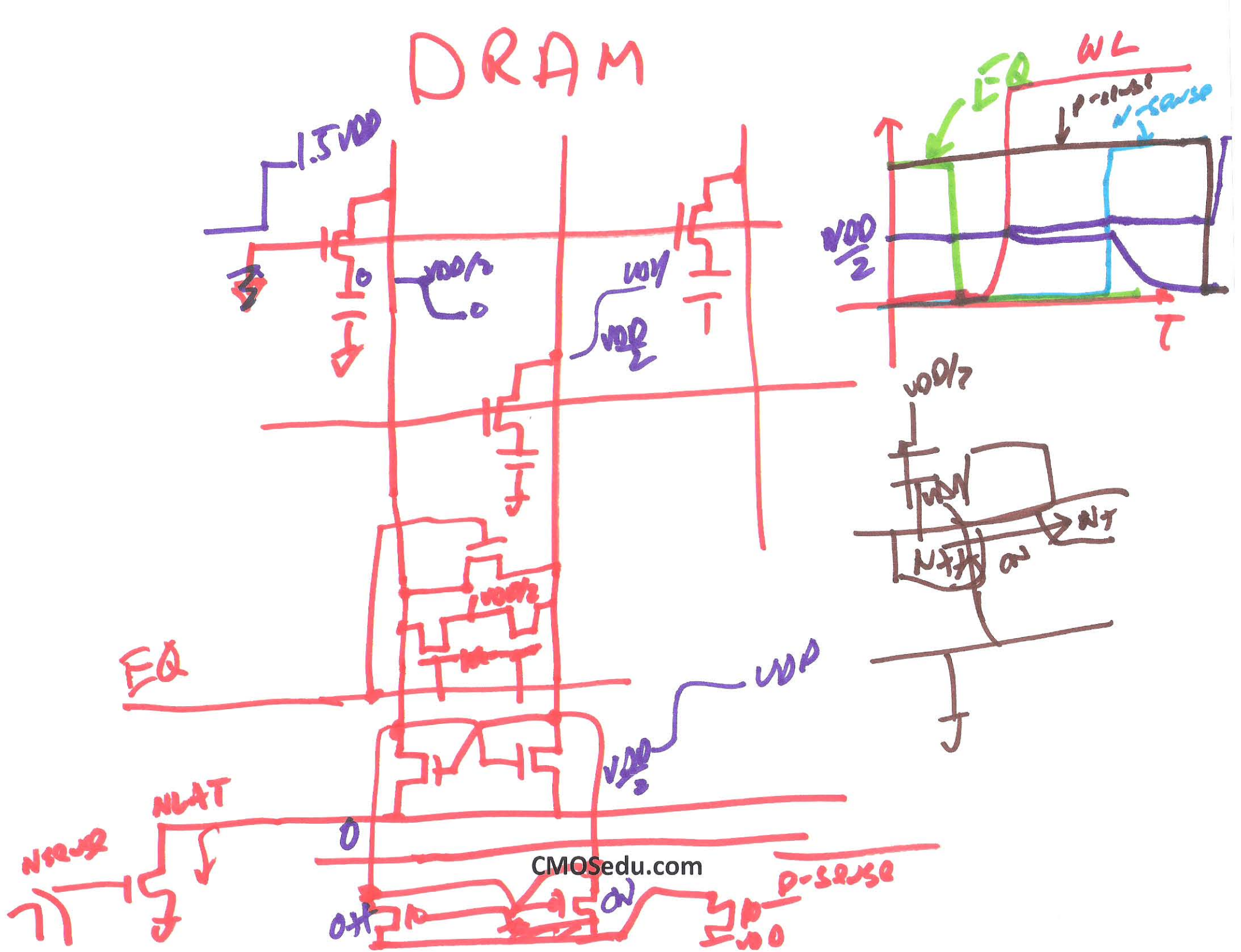
5)

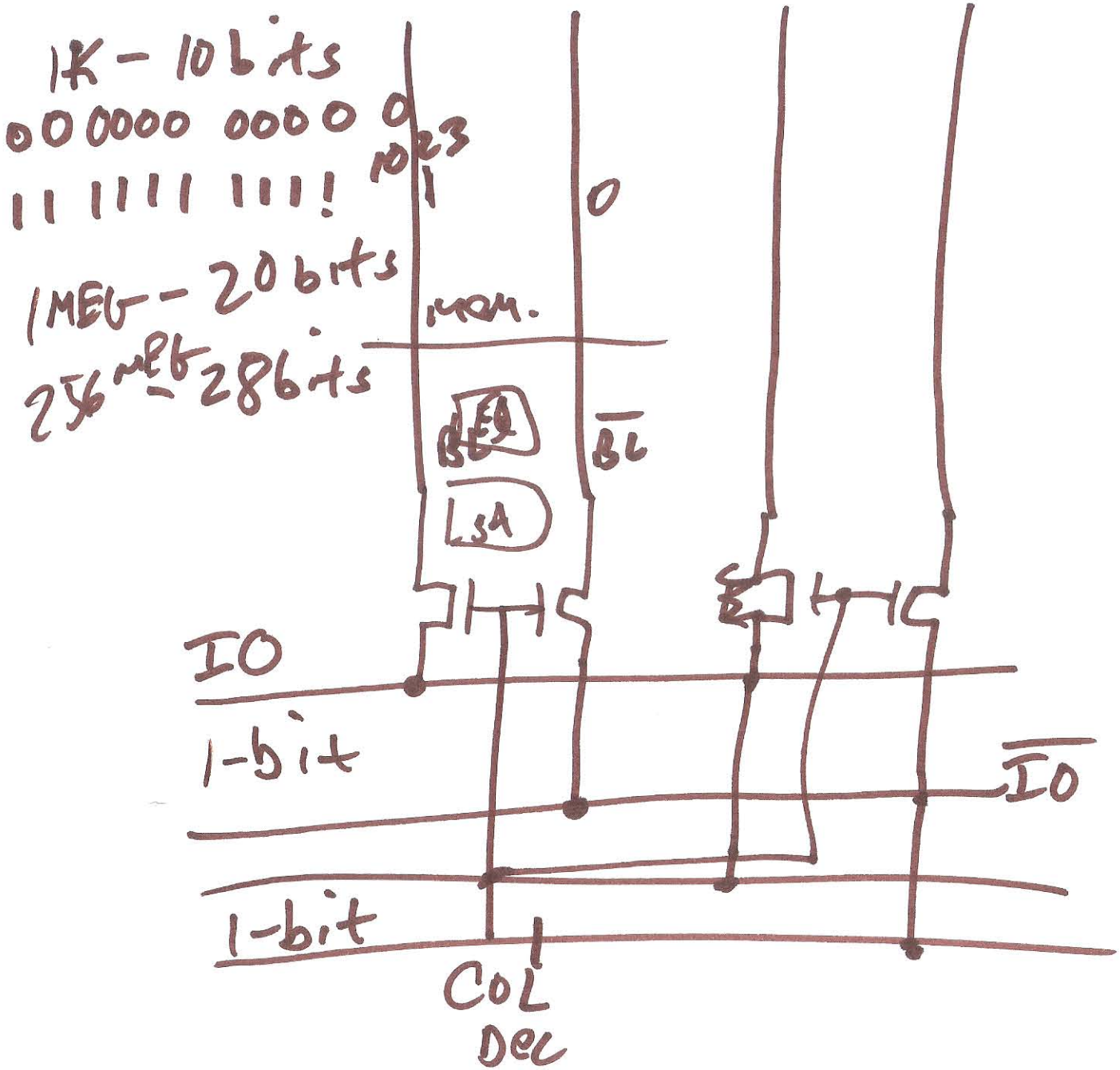
6T-SRAM


VDD
VDD
ON
ON
VDD
off
ON
VDD
BAL
VDD/2
VDD
VDD
ON
VDD/2
WL
VDD
0
BL
BL

6)

DRAM





26

256 MWords

word = 8 bits

14-bits RW Add

14-bits Column Add

16

14-bits = 8K

16 K RWS

16 K Cols

256K

512 512

32 ARRAYS

~~512~~ ARRAYS

256

64 ARRAYS / INTEL.

8)