Overview of Packaging using Through Silicon Vias (TSV)

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12/03/21

SECTION 1

INTRODUCTION TO THROUGH SILICON VIAS (TSV)

- This section will introduce and discuss through silicon vias and its packaging. Here are some points this section will cover:
  - Origin and background of the TSV
  - Advantages vs disadvantages of using a TSV
  - What devices use TSV's

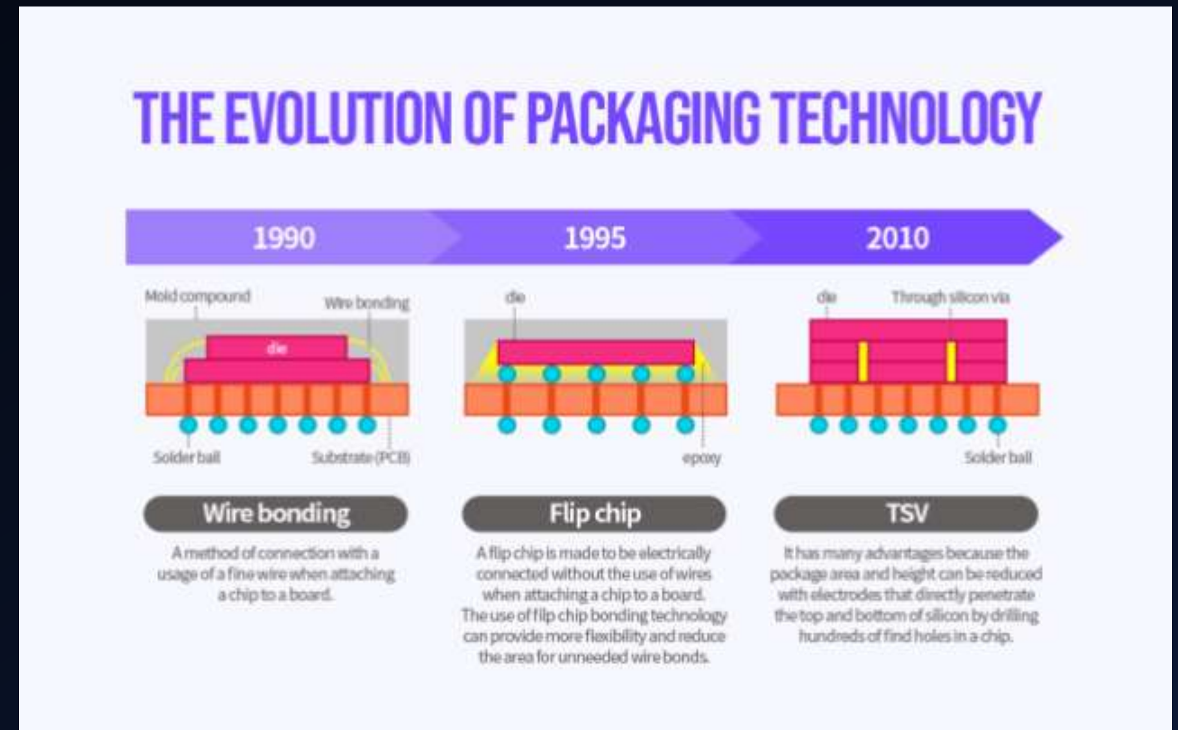

Figure 1 Evolution of Integrated Circuits Packaging [18]

Origin of Through Silicon Vias

- TSV started with the patent idea of "Semiconductive Wafer and Method of Making the Same" filed on October 23, 1958 (granted on July 17, 1962) by William Shockley. [15]
- It was then further developed by IBM researchers Merlin Smith and Stern Emanuel with their patent "Methods of Making Thru-Connections in Semiconductor Wafers" filed on December 28, 1964 (granted September 26, 1967). [17]
- It was not until the 1980s that the first 3-Dimensional Integrated Circuit (3D IC) was fabricated with the TSV process. This achieved higher levels of integration with Moore technology – affectively improving performance and cost of semiconductor technology [2].
- Today, many companies use and evolve their technology by implementing 3D TSV packaging into their devices. Some notable companies being Samsung Electronics, Xilinx, and Toshiba Electronics. [9] TSV technology is being implemented in both memory and logic silicon devices. [16]

https://www.nobelprize.org/prizes/physics/1956/shockley/biographical/

Figure 2.1 William Shockley [12]

https://ethw.org/Merlin_G._Smith

Figure 2.2 Merlin Smith [4]

About Packaging using Through Silicon Vias

- A TSV is used to allow vertical interconnection access through a microchip and passes through the silicon die or wafer. This allows for stacking of silicon dice. [20]
- There are three types of IC packaging
  1. 2-Dimensional Integrated Circuits (2D IC)
  2. 2.5-Dimensional Integrated Circuits (2.5D IC)
  3. 3-Dimensional Integrated Circuits (3D IC)
- TSV's are vital in 2.5-dimensional and 3-dimensional integrated circuits (2.5D and 3D IC) for increasing overall system performance. [16]
  - Improved power management
  - Increased data transfer rates
  - Better signal integrity
  - Increase in bandwidth

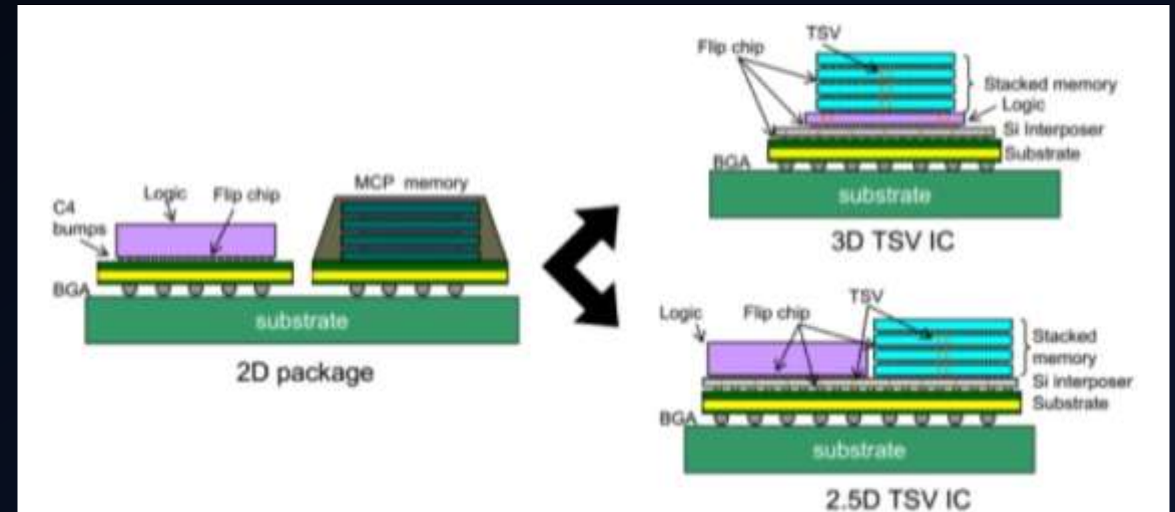

Figure 3 Structure of the three types of IC packaging [1]

About Packaging using Through Silicon Vias

- A 2D IC is packaged using either flip-chip or wire-bond technology. The flip-chip technology is wireless and contains copper tracks, copper vias, and solder bumps that can be roughly 100um in diameter attached to the substrate (PCB). [10]
- A 2.5D IC differs from the 2D by adding in a silicon interposer placed between the dice and the substrate, where the interposer has TSV's connecting the metallization layers on its upper and lower surfaces. [10] This allows for interconnection between different dice to occur by setting them side-by-side. Example: A memory die to a logic die.
- A 3D IC is set up similarly to 2.5D, but it differs by stacking the dice vertically on top of each other. The TSV's are used to interconnect between the dice.
- Both 2D and 3D IC use flip-chip technique onto the silicon interposer.

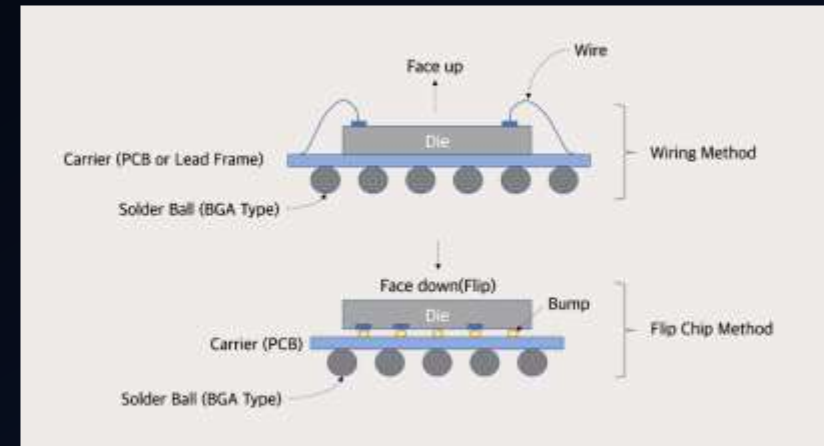

Figure 4.1 Cross-sectional view of 2D IC, wire-bond (top) flip-chip (bottom) [1]

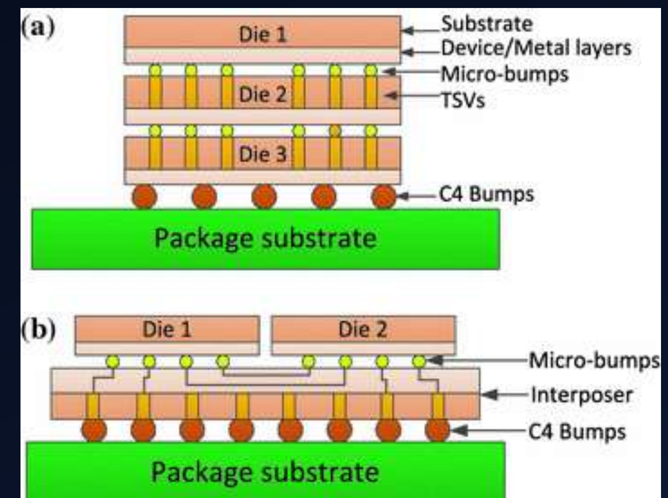

Figure 4.2 Cross-sectional view of (a) 3D IC and (b) 2.5D IC [21]

Advantages and Disadvantages of TSV and Alternatives

- This table lists the advantages and disadvantages of packaging using 2D IC (no TSV) and 2.5D and 3D IC (with TSV).

Integrated Circuits	Advantages	Disadvantage
2D (edge-wired package)	• Higher mobilities and immunity against surface defects • More flexible materials can be used (ex. Making flexible displays)	• Higher cost • Largest layout space • Highest power consumption
2.5D (TSV package)	• Placing chips side-by-side reduces heat buildup • Easier to upgrade/modify	• Larger layout space • Larger interconnection
3D (edge-wired package)	• Small layout space used • Better power consumption	• Slightly larger area used than the 3D TSV package due to edge-wiring • Data buffer
3D (TSV package)	• Smallest layout space used • Highest signal performance • Better power consumption	• Less flexible in various stacked dice's size, pitch, and material • Larger vertical space used

Table 1 Advantages and Disadvantages of using different IC packaging [10]

Importance of Packaging

- Packaging is important in order to prevent the following:
  - Physical damage
  - Environmental damage
  - Lose signal integrity of more sensitive/fragile connections
- And it can also enhance the following:
  - Channel heat dissipation
  - Improve performance
  - Reduce power consumption
- Organizes I/O wires of the IC

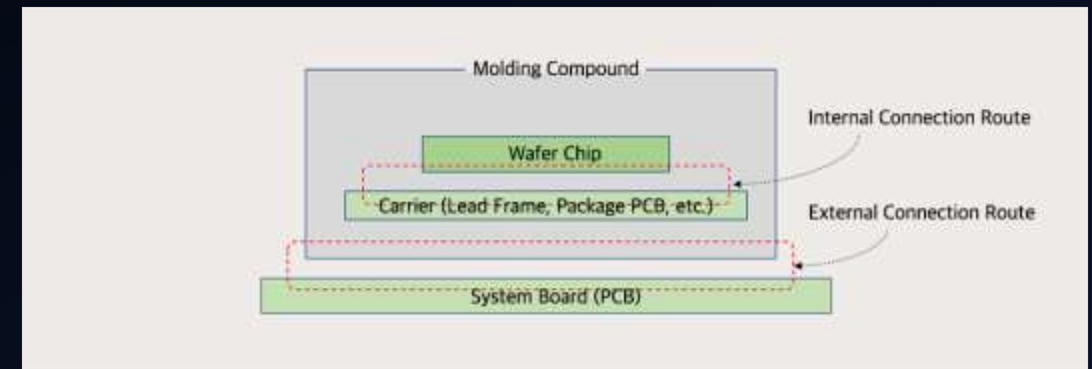

Figure 5 Internal and external structure of semiconductor package [1]

Devices Today using TSV Packaging

Figure 6.1 DRAM using 3D TSV packaging technology [6]

- DDR5 SDRAM made by Kingston
- Package Type: BGA, 3DS TSV

- Kintext UltraScale made by Xilinx
- Package Type: SSI (3D TSV)

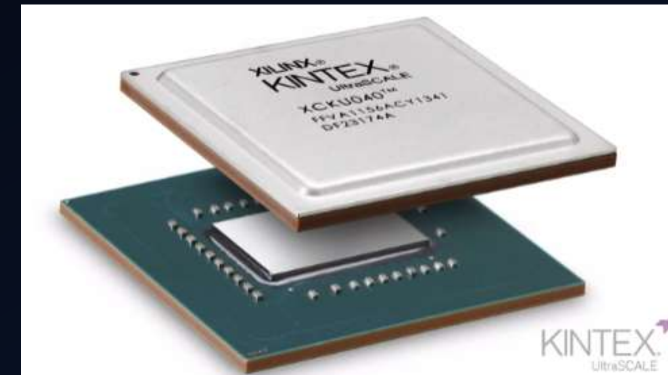

Figure 6.2 FPGA using 3D TSV packaging technology [22]

Figure 6.3 RDIMM Chip using 3D TSV packaging technology [14]

- DDR4 RDIMMs made by Samsung
- Package Type: BGA, 3DS TSV

SECTION 2

ANALYTICS OF THROUGH SILICON VIAS (TSV) AND ITS PACKAGING

- This section will go more in-depth with TSV technology. Here are some points this section will cover:
  - Performance
  - Cost
  - Using BGA in TSV IC technology
  - Process of a TSV
  - Current problems in TSV technology
  - Future outlook of TSV packaging

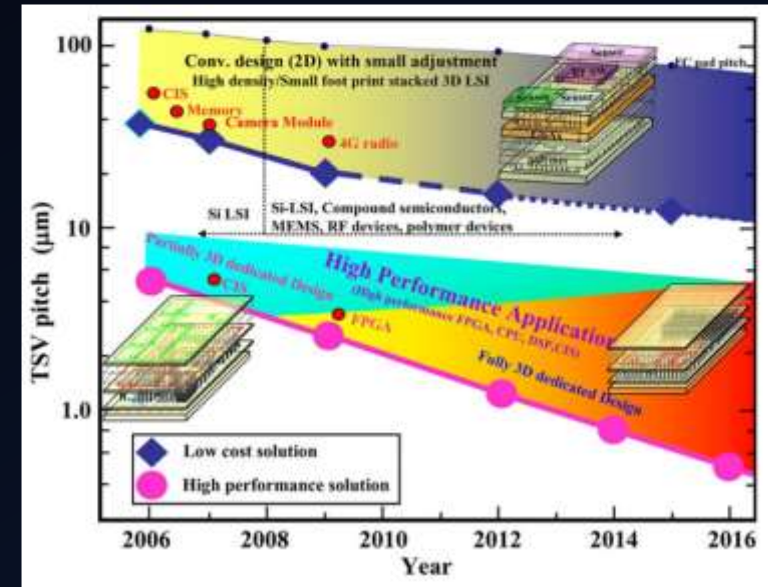

Figure 7 Road map of TSV technology [11]

Performance of TSV Packaging

- From the older DDR3 to the newer HBM2, there's a significant increase in performance for both signal performance and power consumption as shown in Figure 8.
- Note: The right-side y-axis in Figure 8 is supposed to have a decimal, not a comma.
- The DDR3, DDR4, and GDDR5 devices recorded in the graph were that of 2D IC technology. This graph showcases the improvement by migrating to the more evolved technology, 3D TSV.
- By combining flip-chip ball grid array (FCBGA) assembly with 3DS TSV technology, the performance of HBM2 can be realized. [16]

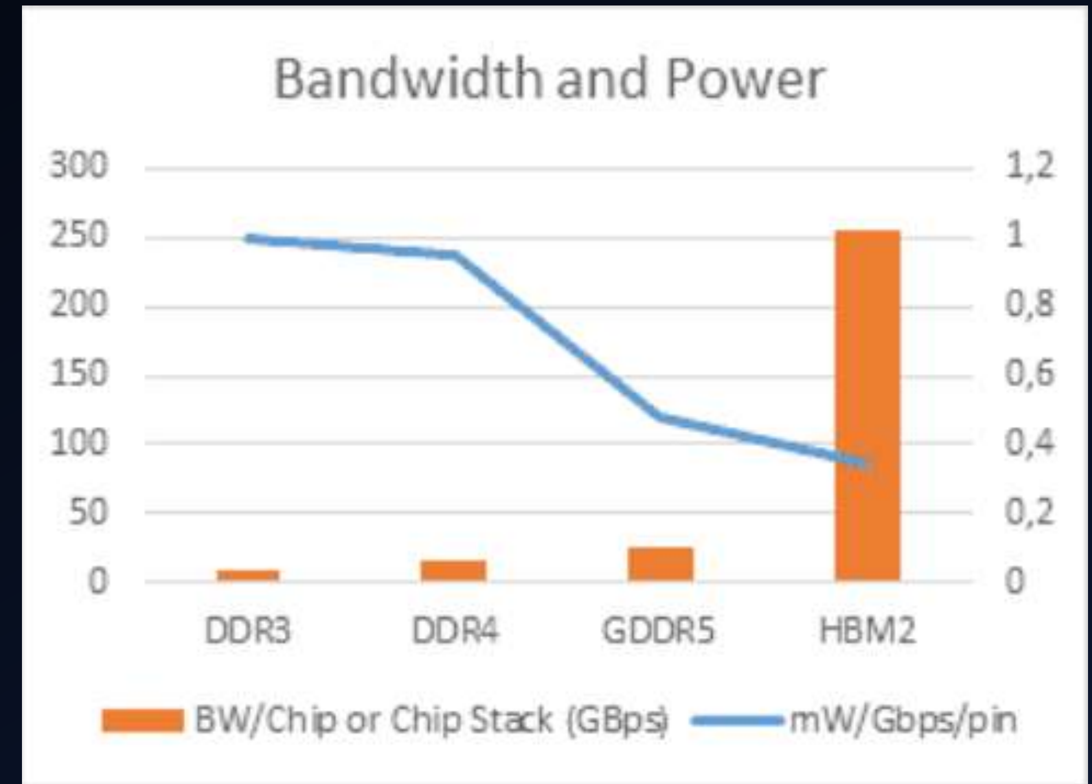

Figure 8 Memory products showcasing increase bandwidth with decrease in power consumption [16]
Bandwidth (GBps) left axis, Power Consumption (mW) per Gbps per pin right axe

Cost of TSV Packaging

- With increase performance comes evolving technology. The 3D TSV IC is currently the new generation of IC tech.
- In Figure 9.1, the CAGR of TSV packaging has increased a lot more than its other packaging competitors. This shows that there is an increasing larger demand for TSV packaging in the recent years than there are for alternatives. [7]
- In Figure 9.2 assesses the cost between 2.5D and 3D TSV technology. The evolving 3D TSV technology grows to be cheaper over time.

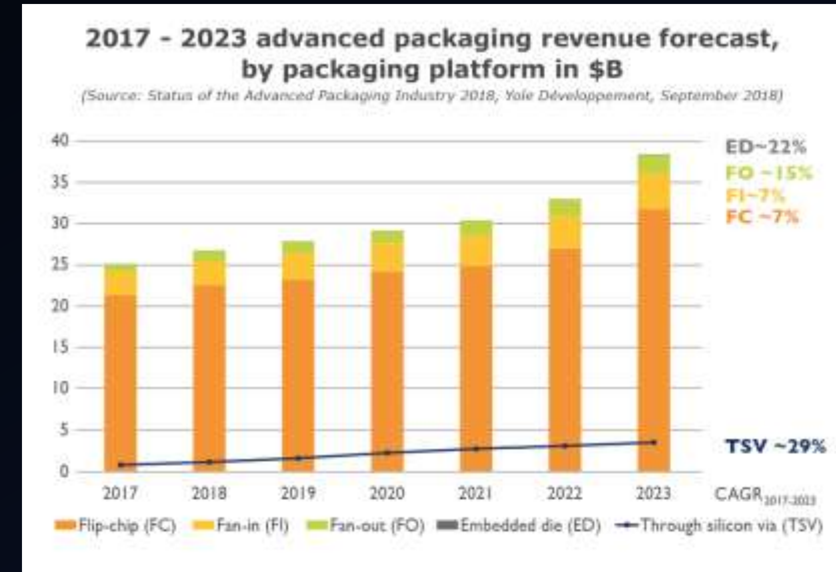

Figure 9.1 Compound Annual Growth Rate (CAGR) of Advanced Packages in the last few years [7]

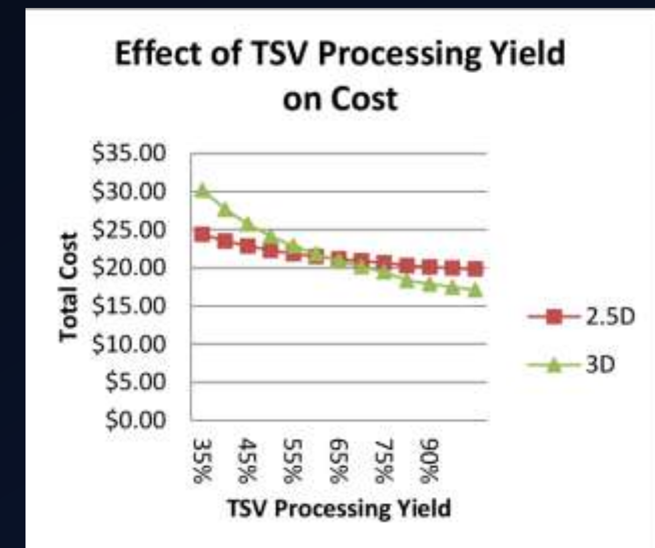

Figure 9.2 Cost Comparison of 2.5D and 3D TSV [13]

BGA Technology (flip-chip) in TSV Packaging

- Most popular TSV IC's use BGA technology, or flip-chip, to maximize performance of their devices. Here are some advantages and disadvantages of using a BGA.

Advantages	Disadvantages
High interconnection density	Prone to stress due to flexural stress
Efficient (fast) and manageable	Difficult inspection for verification
Better heat dissipation	Cost of equipment (oven)
Shorter path between die and PCB substrate	Difficult to modify during development

Table 2 Advantages and Disadvantages of using BGA [2]

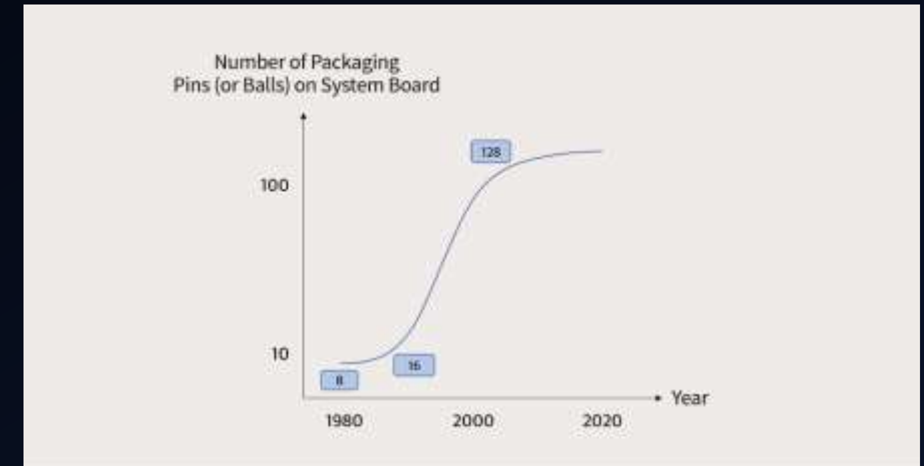

Figure 10 Increase of BGA pins as IC's evolve [1]

In-depth look at a TSV Process

- Figure 11 is a 3D Large-Scale Integration (LSI) structure that uses TSV technology to interconnect the image sensor.
- Image sensors were one of the first applications to use TSV's.
- In this specific project, they use TSV's to connect the backside bump to the sensor chip, allowing direct connect to the substrate (PCB).
- The TSV holes are made with a deep Si etch and a successive SiO_2 etch process. A rectangular etch is made for the TSV once created.

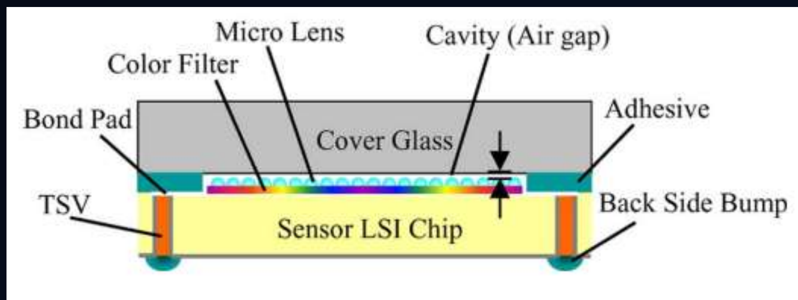

Figure 11.2 Cross-sectional view of CSP Structure [11]

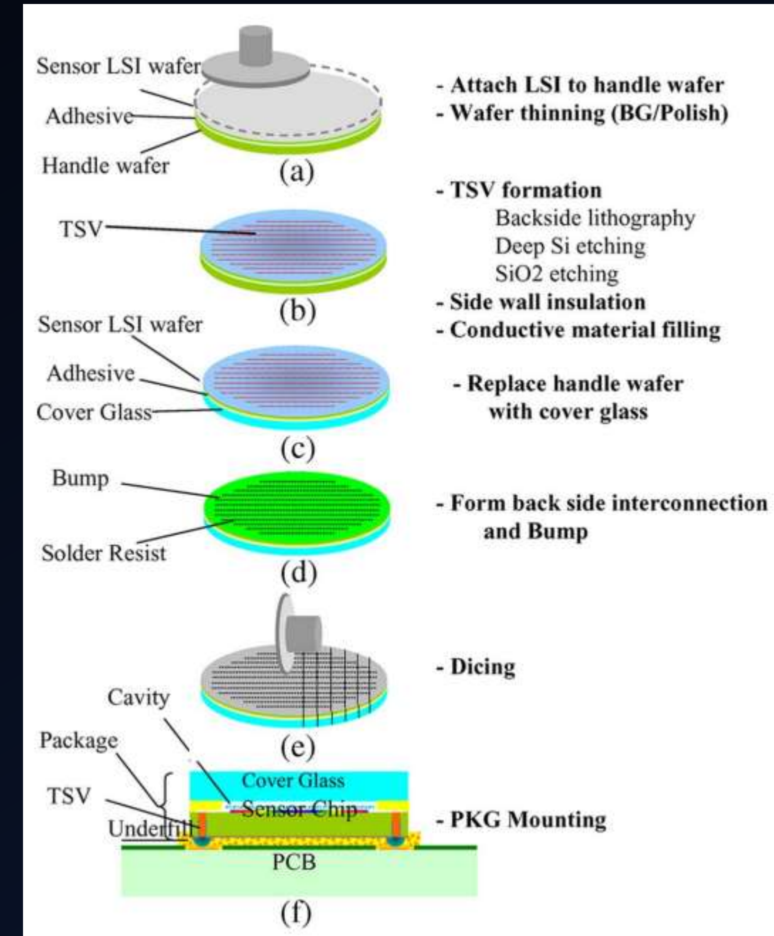

Figure 11.1 Chip Sized Package (CSP) for an Image Sensor Process flow with TSV [11]

In-depth look at a TSV Process

1. The TSV goes through the etching process, forming a cavity. Figure 12 (a)(b).
2. A side-wall insulator is formed by using a low temperature plasma enhanced chemical vapor deposition (PECVD), SiO_2 deposition, and SiO_2 RIE. This is made to create a dielectric insulation to prevent current leakage. Figure 12 (c).
3. Contact and diffusion barrier metal deposition are placed in the TSV cavity. Figure 12 (d).
4. The cavity is now filled with a conductive paste. This is used to reduce process cost. Figure 12 (e).
5. The top of the TSV is shaved off of excess contact metal, conductive paste, and diffusion metal. Figure 12 (f).

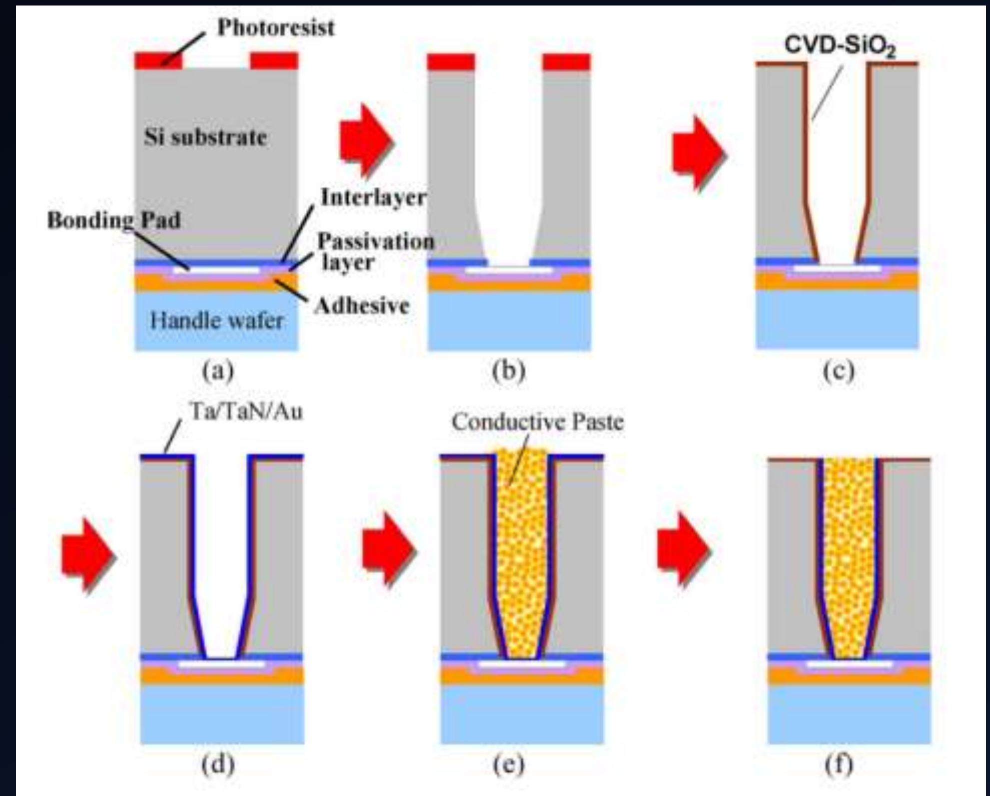

Figure 12 Process flow for a TSV [11]

In-depth look at a TSV Process

- Figure 13.1 was scanned using an electron microscope (SEM) to capture this image. This image is showing an etched rectangular TSV cavity of 60 x 60 um^2.
- Figure 13.2 gives the cross-sectional view after the TSV process was completed. The TSV has a diameter of 20 um and depth of 270um.
- Advantages of using this method for creating TSV's:
  - Lower cost of equipment compared to other techniques
  - Shorter processing time
- Disadvantages of using this method for creating TSV's:
  - TSV's have relatively high resistivity than normal
  - Conductive paste contraction during the cure cycle

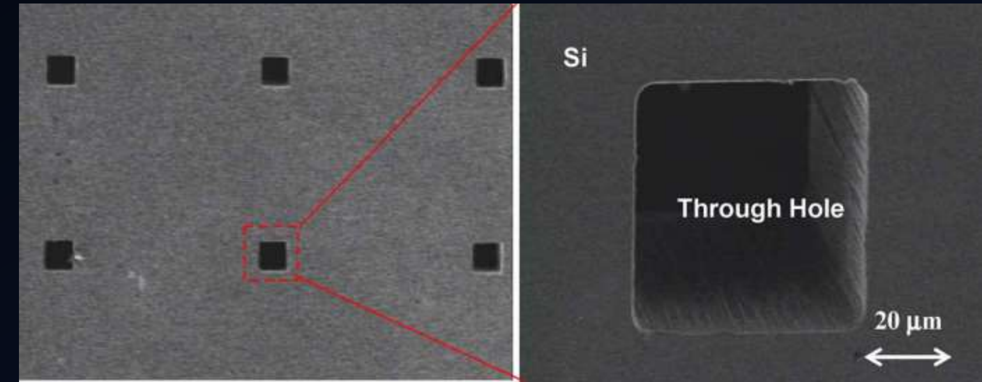

Figure 13.1 TSV hole created after the etching process [11]

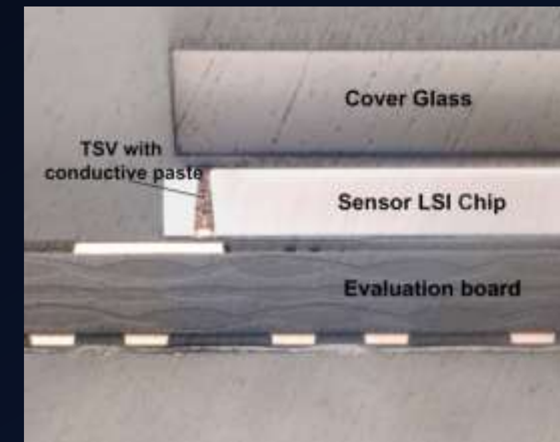

Figure 13.2 Cross-sectional view of CSP after packaging [11]

Current Challenges of TSV Packaging

- As 3DS TSV ICs continue to grow, devices as large as 12 stacks of die are being created. [14] Samsung's 12-layer 3D-TSV IC technology has a vertical height of 720um. Consider the three-way optimization: power, performance, and area (PPA). With the traditional 2D IC slowly turning towards 3D, cubic area must be optimized. [8] As of now, with every 3DS TSV IC, the increase in vertical area is the tradeoff.

- One of the bigger hurdles are power and thermal. The top die of a 3DS IC gets its power from a lower die. At the lowest die, it gets its power from the interposer. The higher the stack, the more power is consumed from the lowest die footprint. And the more power applied to the footprint, the more power needs to be dissipated. [8]

- Currently not many EDA tools support 3D IC development. EDA tools need to keep up with the 3DS IC designs to incorporate vertical stacking tradeoffs, alongside its power consumption, so it can meet PPA standards. [8]

Moving Forward

- More dice will stack together like Samsung's new 12-layer 3D-TSV. Thickness remains the same thickness as its 8-layer counterpart (720um). [14]
  - Provides 24-gigabyte (GB) of High Bandwidth Memory (HBM)
  - Over 60,000 TSV holes for maximum performance
- Currently, 3DS ICs are used primarily on memory-based products. Other future applications may lead into further development of Internet-of-Things (IoT) and mobile devices. [23]

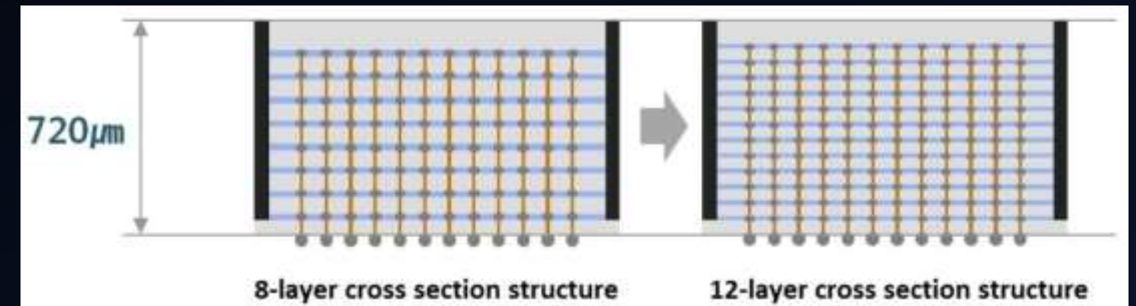

Figure 14.1 Samsung's 12-layer 3D-TSV technology [14]

Summary

- A TSV is used as a high-performance interconnection technique to fabricate three-dimensional integrated circuits (3D IC). It stands as the higher performing technology as opposed to its alternatives: wire-bond, flip-chip.
- There are three different design types in IC (1) 2-dimensional, (2) 2.5-dimensional, and (3) 3-dimensional. TSVs are vital in 2.5D and 3D designs, but both use flip-chip to attach the chip to the substrate (PCB).
- The benefits of using 2.5D and 3D TSV technology is the improved power management, increased data transfer rates, better signal integrity, and the increase in bandwidth.
- The drawbacks of using 2.5D and 3D TSV technology is the larger vertical space used and the flexibility of dice size, pitch, and materials used.
- The packaging of the IC is important to prevent damage and improve chip efficiency/performance.
- 3DS TSV IC demand are on the rise and will soon see the technology used more often to improve electronics cost and performance.

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