Design of Analog Phase-Locked Loops (A tutorial)

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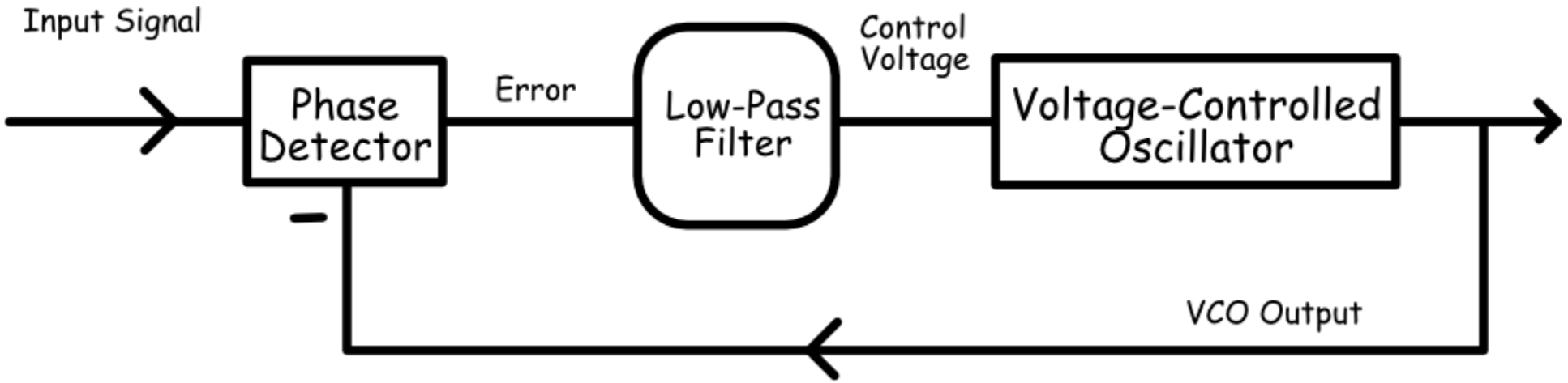
Guideline of APLL Design

- General Phase-Locked Loop Design
- Types of Phase-Locked Loops
- The Phase Detector
- Filters
- Voltage-Controlled Oscillators
- Simulation of The Analog Phase-Locked Loop

General Phase-Locked Loop Design

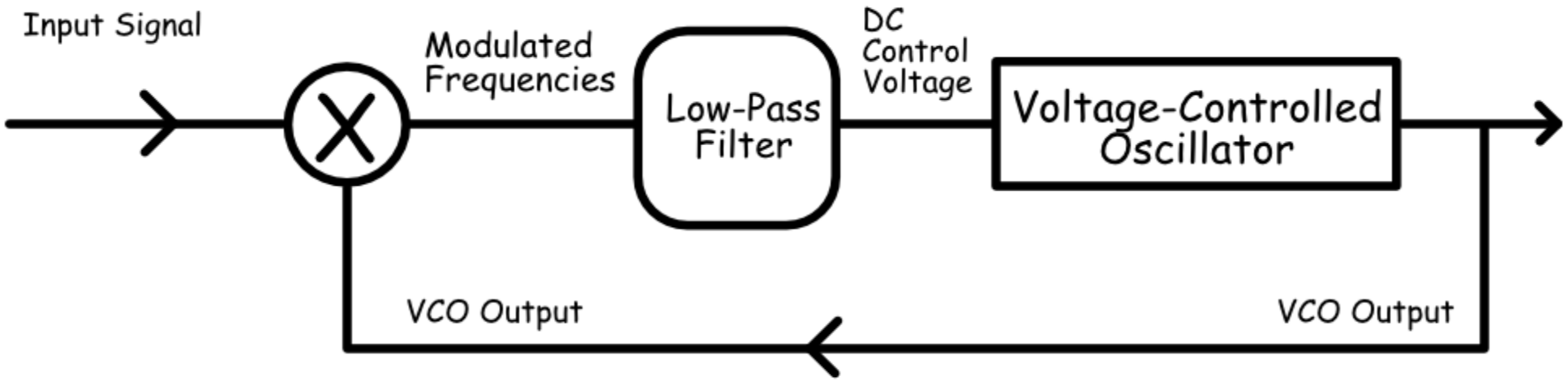


- The Phase-Locked Loop (PLL) is a feedback system that creates a frequency from a Voltage Controlled Oscillator (VCO) that is synchronous to the input signal.
- The output of the VCO is subtracted to the input signal to produce an error signal that would control the VCO frequency that minimizes the error signal.

Types of Phase-Locked Loop Systems

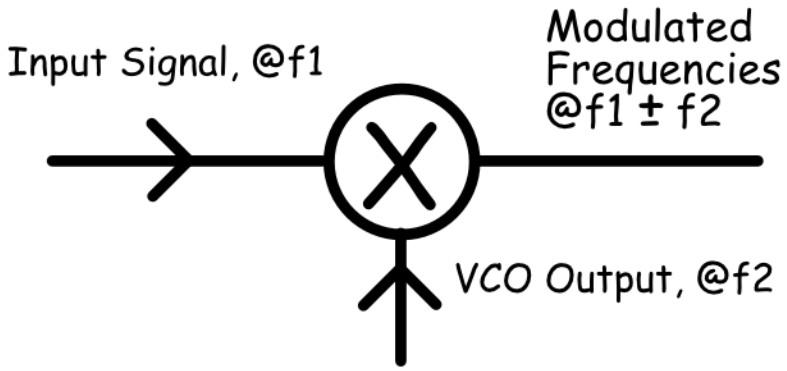
- Analog PLL (APLL)
  - Contains analog circuitry
  - Multiplier circuit used as a phase detector
  - Low-Pass Filter used to filter out undesired signal. Can be active LPF.
  - VCO made using inverters
- Digital PLL (DPLL)
  - XOR or Phase Frequency Detector (PFD) used as a phase detector
  - Low-Pass used to filter out undesired signal. Can also be active LPF
  - A clock divider used to generate signal for the XOR clock input.
- All-Digital PLL (ADPLL)
  - Same structure as DPLL
  - All components replaced with its digital counterpart (Digital Filter replacing LPF, Digital VCO replacing VCO.

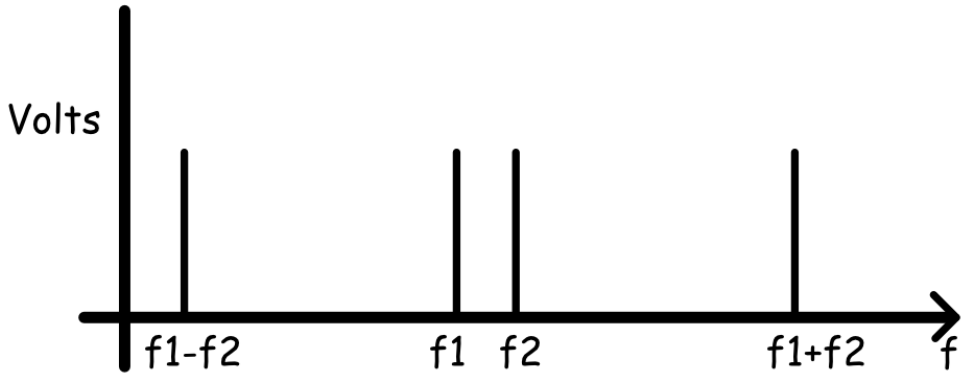
The Analog Phase-Locked Loop (APLL)



- The first component of the APLL is the multiplier. The multiplier in this application will serve as the phase detector.
- The Low-Pass Filter will see two frequencies (discussed later) and filter out the high frequency. This can be achieved with an RC filter.
- The VCO will output a certain frequency depending on the output of the LPF.

The Multiplier Circuit





- The multiplier circuit will take in two input signals with different frequencies and produces two new modulated frequencies.
- In this application, the difference between the two frequencies will serve as a phase deviation.
- If the frequencies are in phase, then the result is a constant DC error.
- Else, a frequency slightly above DC will be produced.

Multiplier Mathematics

$V_{in}(t) = V_{in} \cdot \cos(2\pi f_1 \cdot t + \theta_1)$

$V_{clk}(t) = V_{clk} \cdot \cos(2\pi f_2 \cdot t + \theta_2)$

Recalling the trigonometric identity:

$$\cos(A) \cdot \cos(B) = \frac{\cos(A+B)+\cos(A-B)}{2}$$

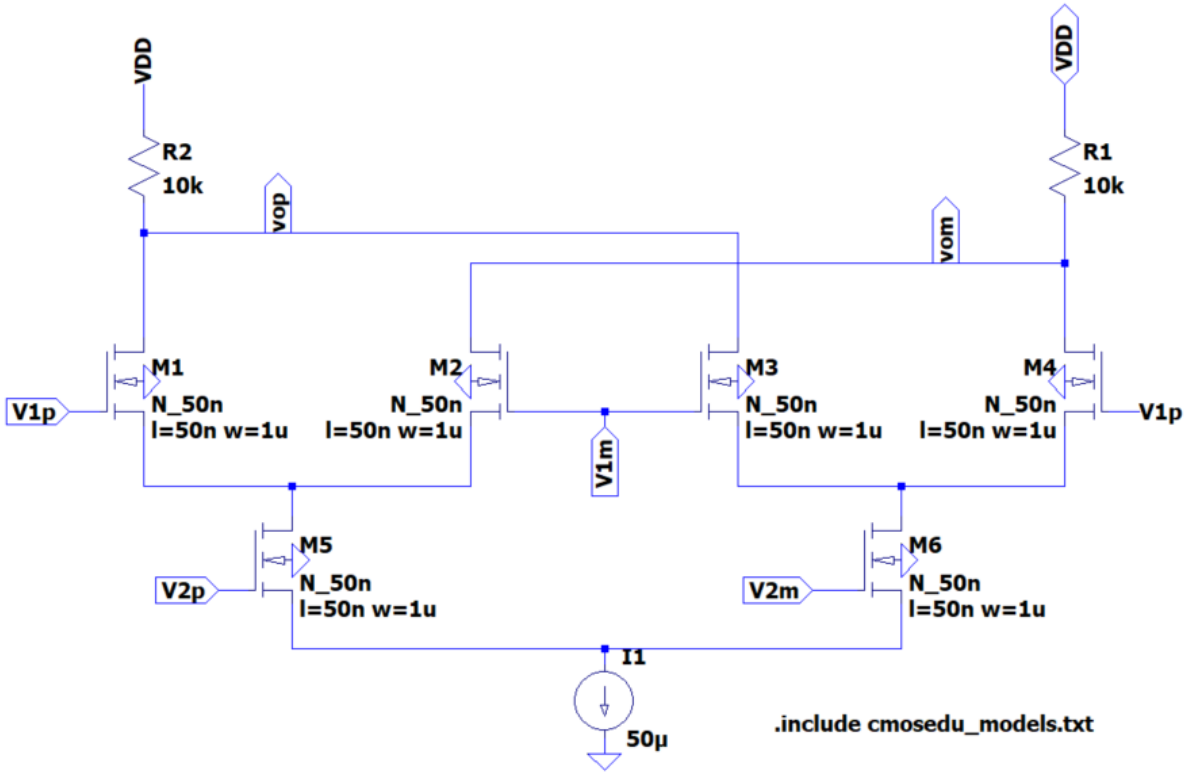
$$V_{mult}(t) = \frac{V_{in} \cdot V_{clk}}{2} \cdot \left[\cos\left(2\pi f_1 \cdot t + \theta_1 + (2\pi f_2 \cdot t + \theta_2)\right) - \cos\left(2\pi f_1 \cdot t + \theta_1 - (2\pi f_2 \cdot t + \theta_2)\right)\right]$$

If $f_1 = f_2 = f$:

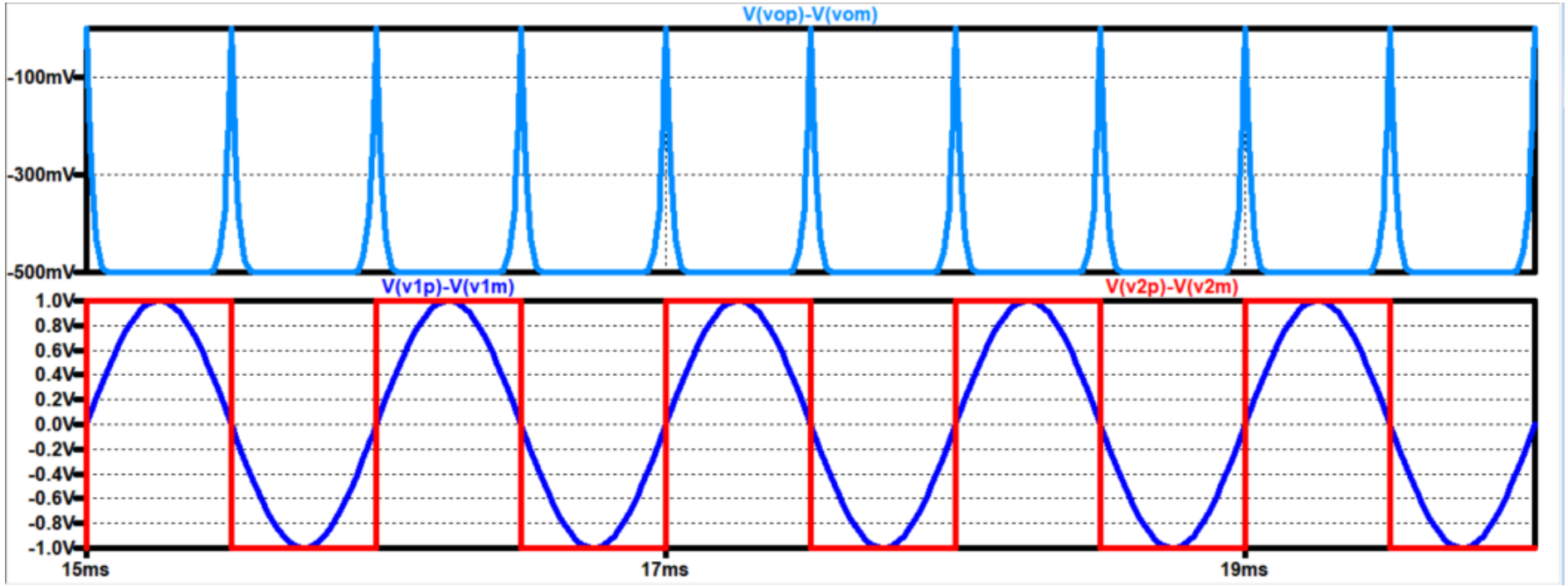
$$V_{mult}(t) = \frac{V_{in} \cdot V_{clk}}{2} \cdot [\underbrace{\cos(4\pi \cdot t + \theta_1 + \theta_2)}_{\text{High Frequency to Filter in LPF}} - \underbrace{\cos(\theta_1 - \theta_2)}_{\text{DC Phase Error}}]$$

Multiplier Circuit: LTSpice

- The multiplier circuit used is a 4-Quadrant multiplier, where the input and output signals are fully differential and require a positive and negative component.
- The sizes are chosen so that we use the smallest length for speed, and a width that would sink a nominal bias current of 10μA. In this circuit, devices M1-4 each will nominally sink around 12.5μA, which is sufficient current.

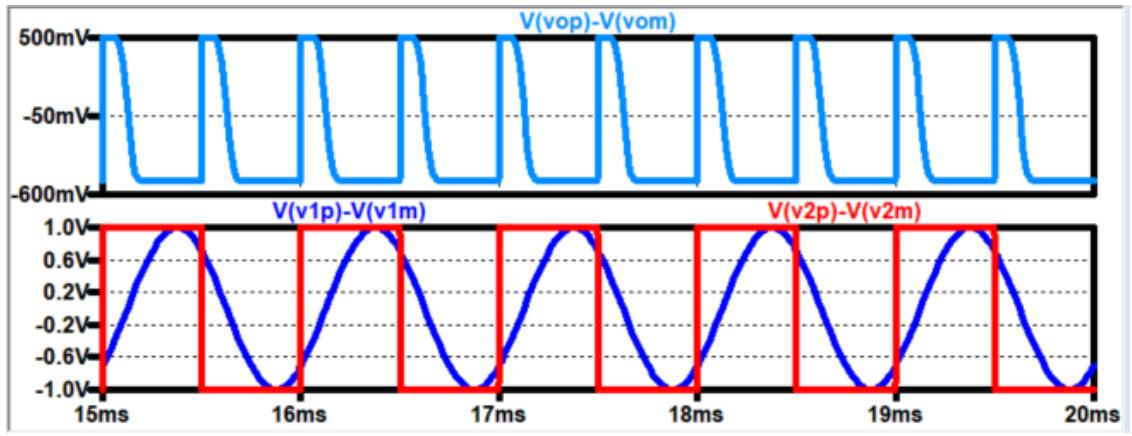


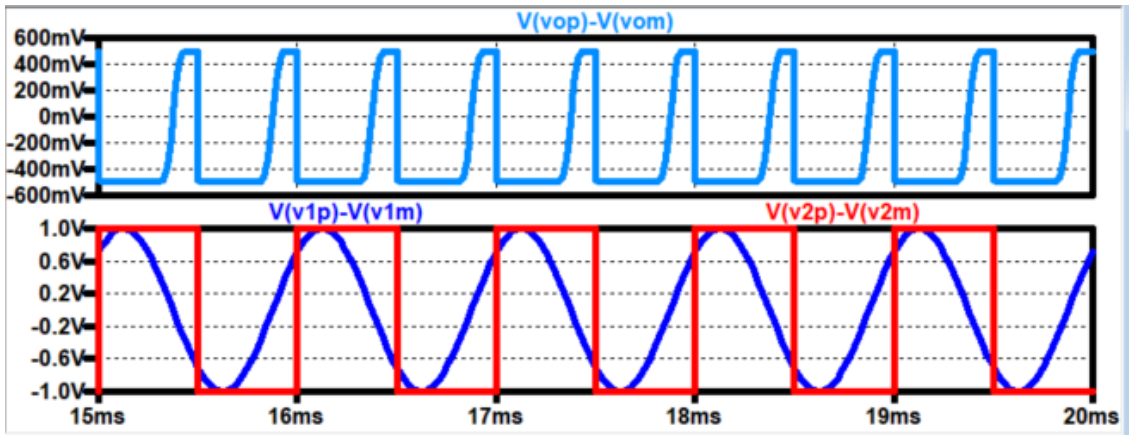
Phase Detector (PD) Sim: $\phi = 0\pi$



From above, the sine wave (input data) and square wave (from VCO) have no difference in phase, which results in a DC average voltage of -0.5V

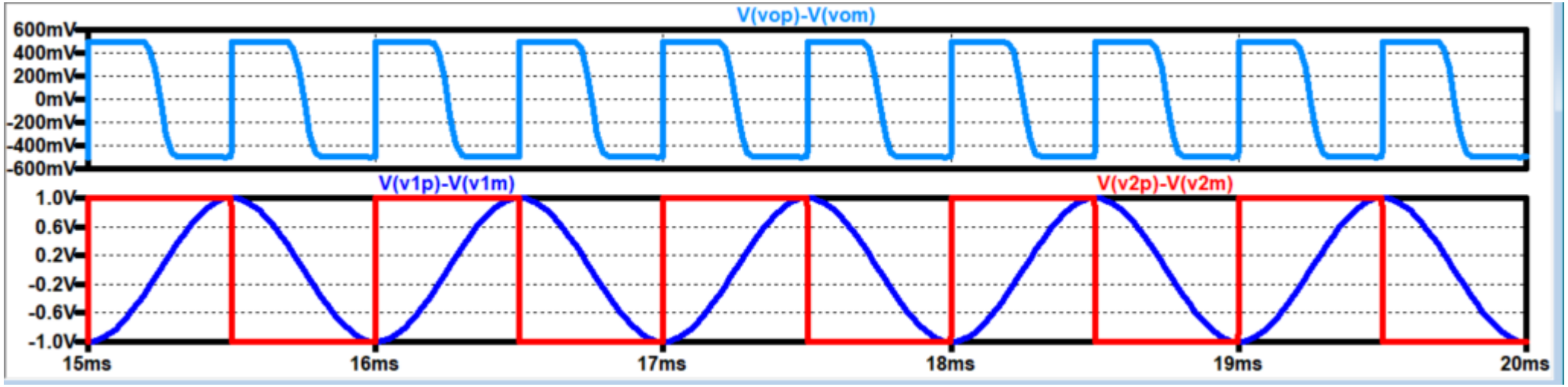
Phase Detector (PD) Sim: $\phi = \frac{\pi}{4}\left(or -\frac{\pi}{4}\right)$





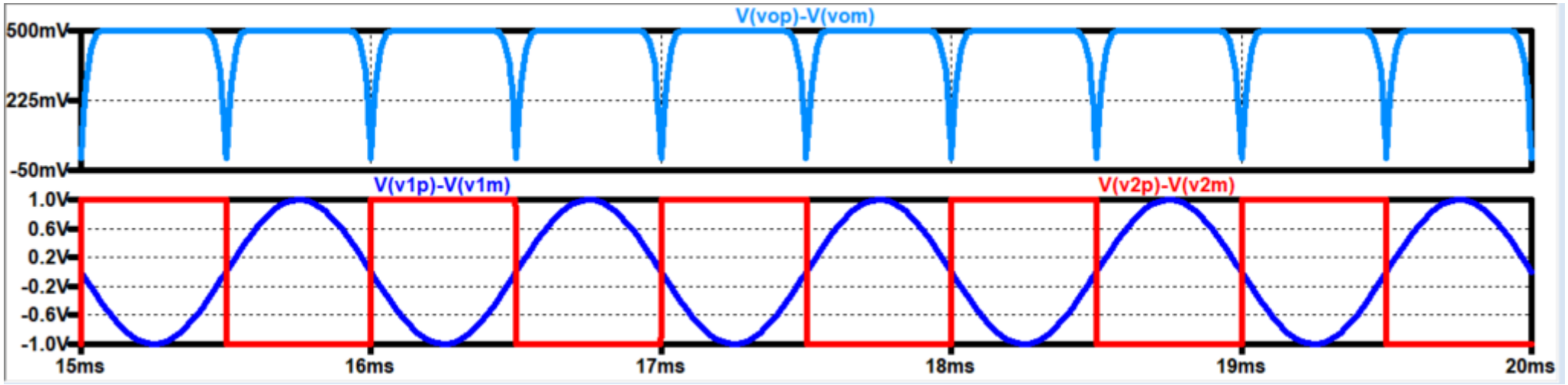
- Moving the phase of the input by either $\frac{\pi}{4}$ or $-\frac{\pi}{4}$, we see that the average DC value will be slightly above -0.5V for both plots, which signifies that as we get to π or $-\pi$, we should get a max voltage of +0.5

Phase Detector (PD) Sim: $\phi = \frac{\pi}{2}$



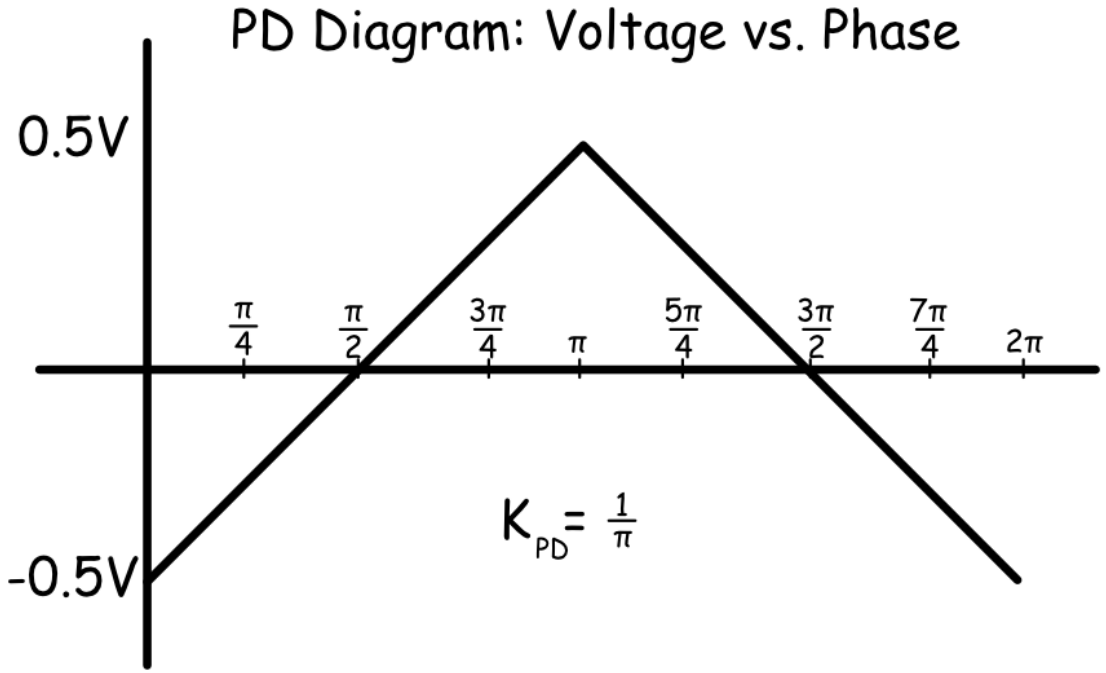
- From above, as the sine wave is shifted by $\frac{\pi}{2}$, we will have an average voltage of 0V

Phase Detector (PD) Sim: $\phi = \pi$



- With the rising edges having a phase difference of π, the average voltage is 0.5V.

Phase Detector Gain



- From the above slides, the average voltage can be shown as a function of phase, which is estimated above.
- The gain of the phase detector is calculated as the average voltage over phase in radians

Low-Pass Filter

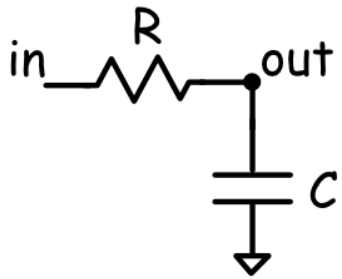
- This stage will filter out any unwanted frequencies and harmonics that are a consequence of using a multiplier and square wave.

❑ Main Filters
  - ❑ Passive: Uses resistors and capacitors
  - ❑ Active: Amplifier is used

- Single-Pole Filter:
  - Simplest to tune
  - Less components
  - Prone to having poor damping factor

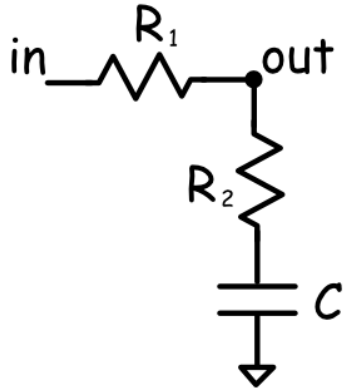
- Lag-Loop Filter:
  - Contains a single-zero in numerator
  - Zero in numerator assists with phase
  - Damping factor increased for shorter lock times

Single-Pole RC Filter



$$K_F = \frac{1}{1 + j\omega R_1 C}$$

Single-Pole, Single-Zero RC Filter

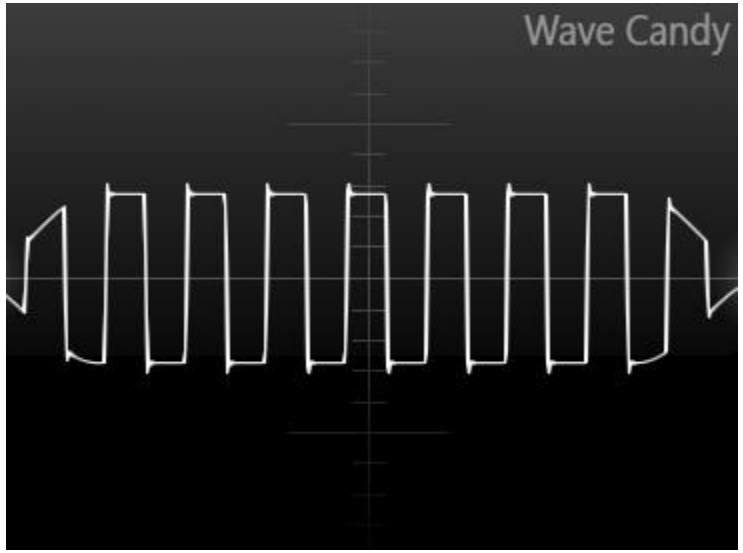


$$K_F = \frac{1 + j\omega R_2 C}{1 + j\omega (R_1 + R_2) C}$$

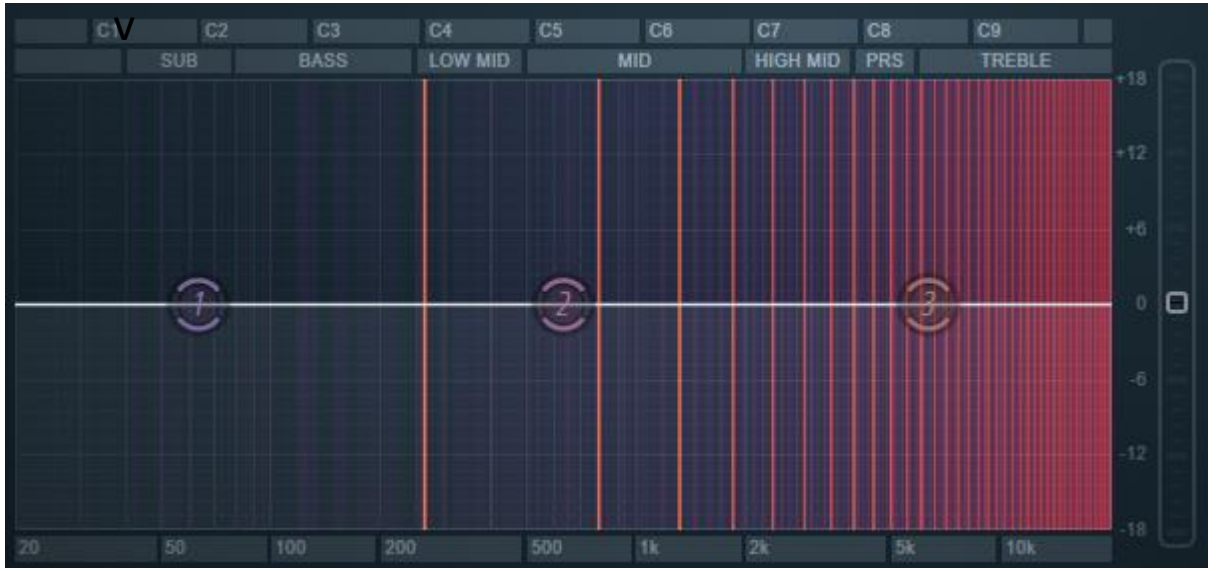
Why use LPF?

- The Low-Pass Filter will feed into the VCO, which will require an average DC voltage, else, there is a chance that the PLL will have a bad VCO settling time
- A square wave is used as one of the inputs. Looking at the spectrum, we can see the following harmonics:

Fundamental Frequency: 264Hz
(Middle C on Piano)

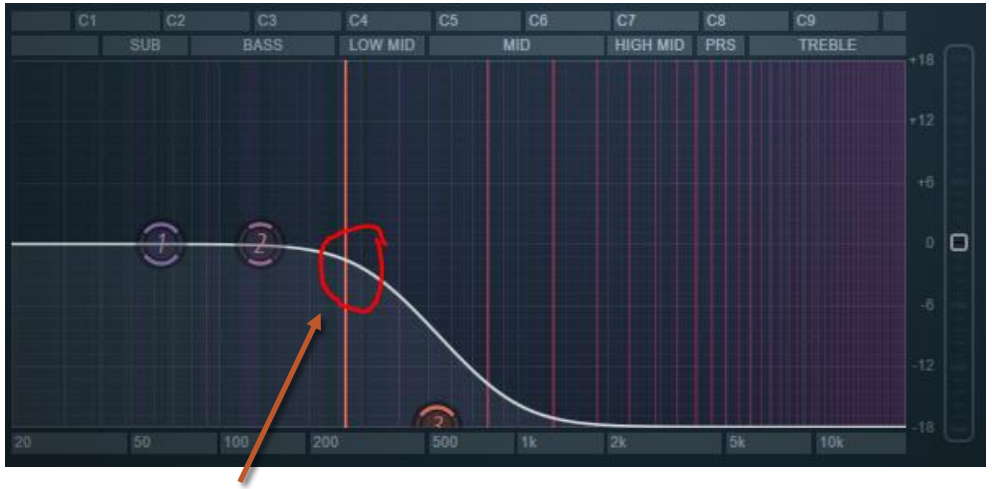


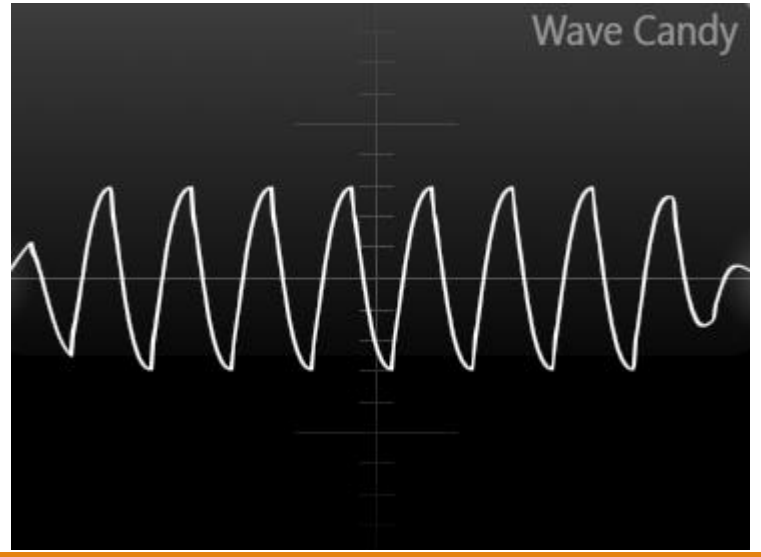
Harmonics of Square wave
(Each bar-line represents a single sine wave)



Why use LPF?

- By filtering out the high frequencies, the square wave will start to look more like a single frequency or even DC
- Since a sine wave has multiple harmonics (many sine waves), the multiplier circuit will also multiply with those frequencies and create unnecessary amounts of modulated frequencies
- Below is the spectrum of a filtered square wave, and the harmonics are mostly filtered out.
- If the loop filter is omitted, then multiple harmonics will be introduced and create too many nonlinearities





Small Signals Demonstration
(Using FL Studio Music Software)

- The two signals of interest are a sine wave and square wave at the same fundamental frequency of 264Hz (middle C)
- When both signals are at the same frequency, there is a resulting frequency at DC and at twice the fundamental frequency (528Hz)
- By changing the sine wave's frequency, as both signals are multiplied together, the DC and the high frequency will come towards the fundamental frequency

f = 264Hz f = 528Hz

Frequency @ DC moves to right! f = 264Hz Freq @ 528Hz moves to left!

Voltage-Controlled Oscillator

- Creates a periodic signal whose frequency can be controlled by an input voltage
- General VCO design uses current-starved standard size inverters.
  - The bias current can be controlled and linearized with a wide MOSFET device, shown to the right
- The center frequency (when $V_{in} = \frac{VDD}{2}$) should be within a frequency range of interest.
  - Calculated using the total capacitance, number of stages (N must be odd + ≥ 5), VDD, and bias current

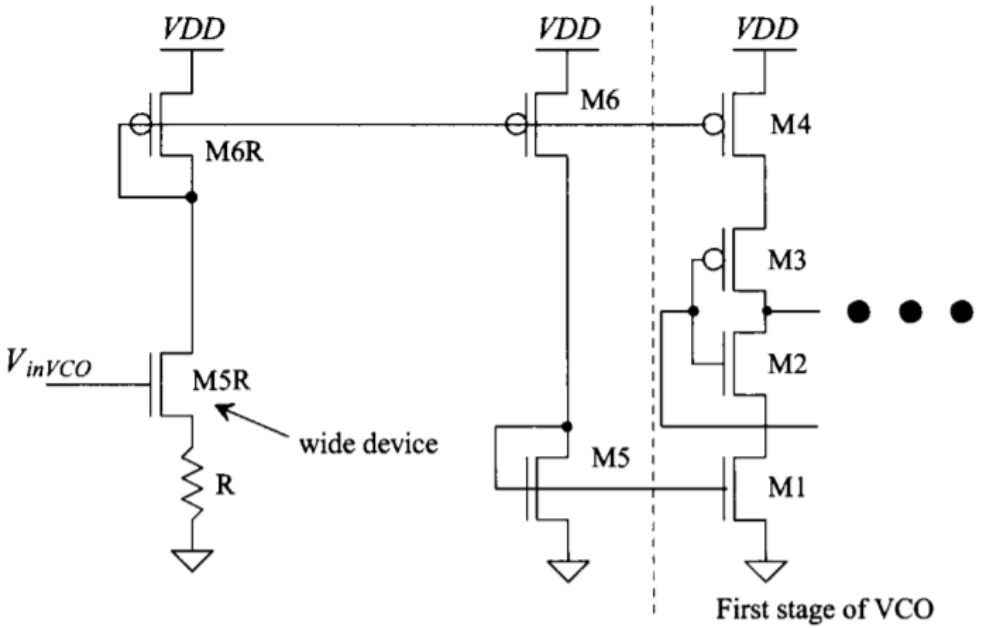
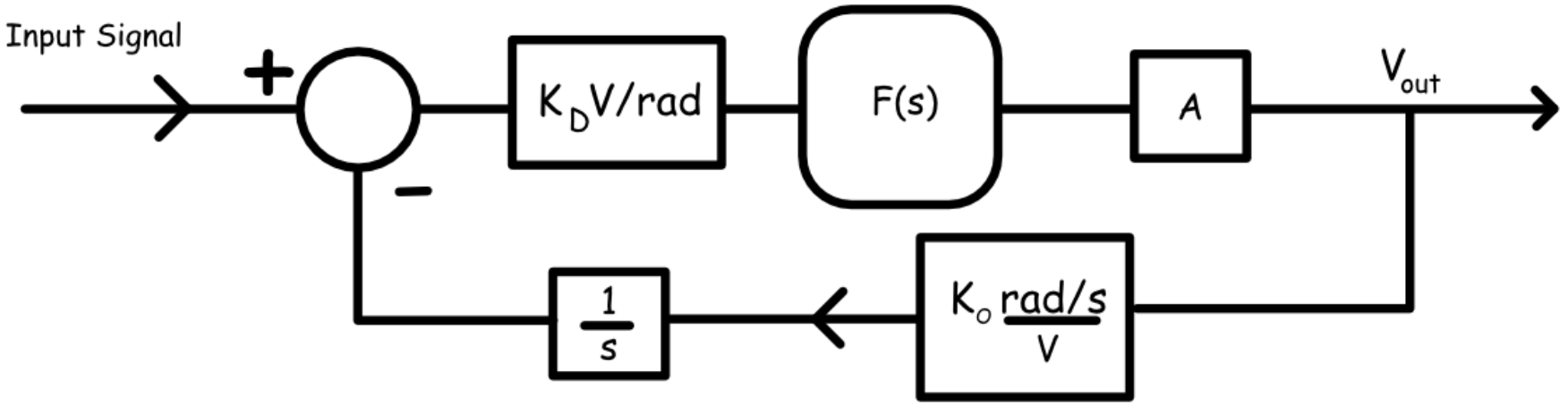


Figure 19.17 Linearizing the current in a current-starved VCO.

APLL Closed-Loop System

- The APLL will have the following block diagram
  - K_D is the PD gain, F(s) is the LPF gain ($F(s) = \frac{1}{1+\frac{s}{\omega 1}}, \omega_1 = \frac{1}{RC}$), A is an optional amplifier gain, K_O is the oscillator gain, and $\frac{1}{s}$ signifies an integration.
- The closed-loop response of the APLL is:
- $\frac{K_D \cdot F(s) \cdot A}{s + K_D \cdot F(s) \cdot A \cdot K_O} = \frac{1}{K_O} \cdot \frac{1}{1 + s \cdot \frac{1}{K_D \cdot F(s) \cdot A \cdot K_O}}$, the APLL closed-loop response



APLL Closed-Loop System

- The complete transfer function will be a 2nd order system, which will be harder to design but will give great results if done properly
- The following is a general equation for the 2nd order APLL, with design parameters:
- $H(s) = \frac{1}{K_O} \cdot \frac{1}{1+\frac{s}{G}+\frac{s^2}{\omega_1 G}}$, where the loop gain, $G = K_D K_O A$, natural frequency, $\omega_n = \sqrt{G \cdot \omega_1}$, and the

damping factor, $\zeta = \frac{1}{2} \cdot \sqrt{\frac{\omega_1}{K_V}}$

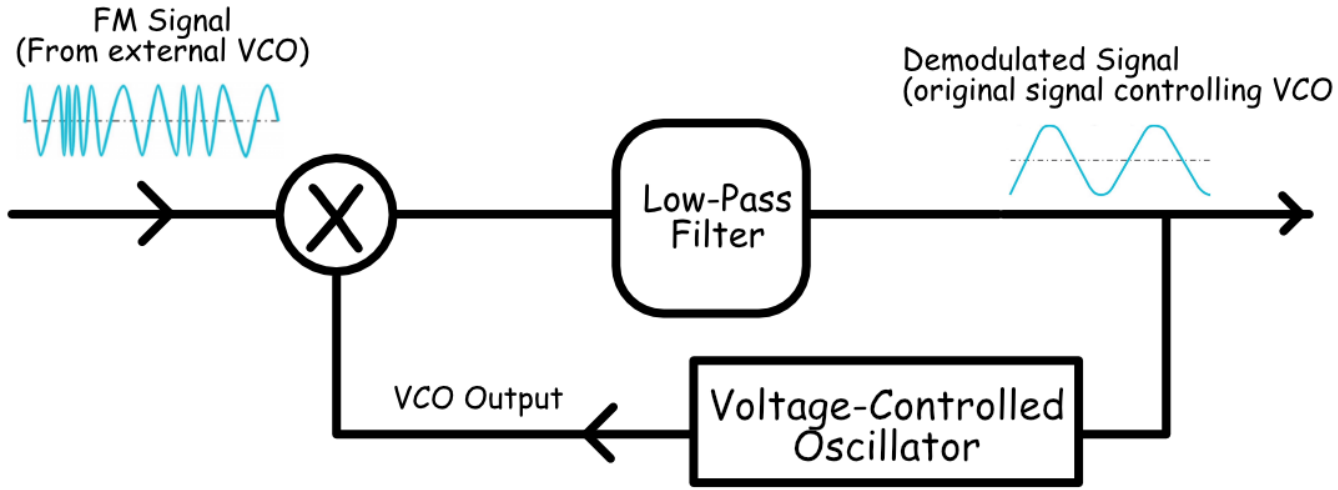
- Using the linearized VCO from Fig. 19.18 in the CMOS textbook, the center frequency is 100MHz, and the gain of the VCO is

$K_O = 1.57 \cdot 10^9 \frac{rad}{V} \cdot s$, and the gain of the PD is $K_D = \frac{1}{pi} \cdot \frac{V}{rad}$

- The Bandwidth is chosen to be $\omega_1 = \frac{1}{20ns} = 50MHz$, therefore R=10k and C=2pF

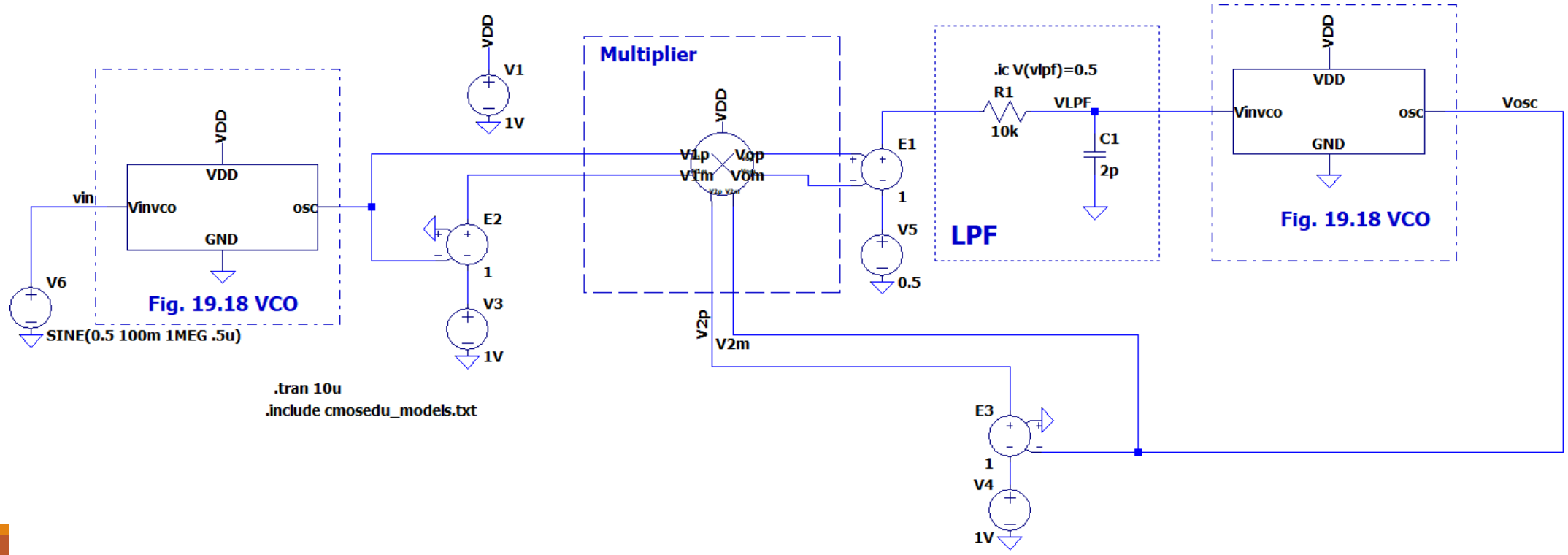
FM Demodulation

- One of the main applications of an APLL is in the use of Frequency Modulation.
- A testbench can be setup where the input signal is the FM signal (from an external VCO), and the output demodulated signal is the result of filtering the error signal.
- The demodulated signal is also controlling the local VCO, and the difference between the external and internal VCO's results in a low frequency oscillating demodulated signal



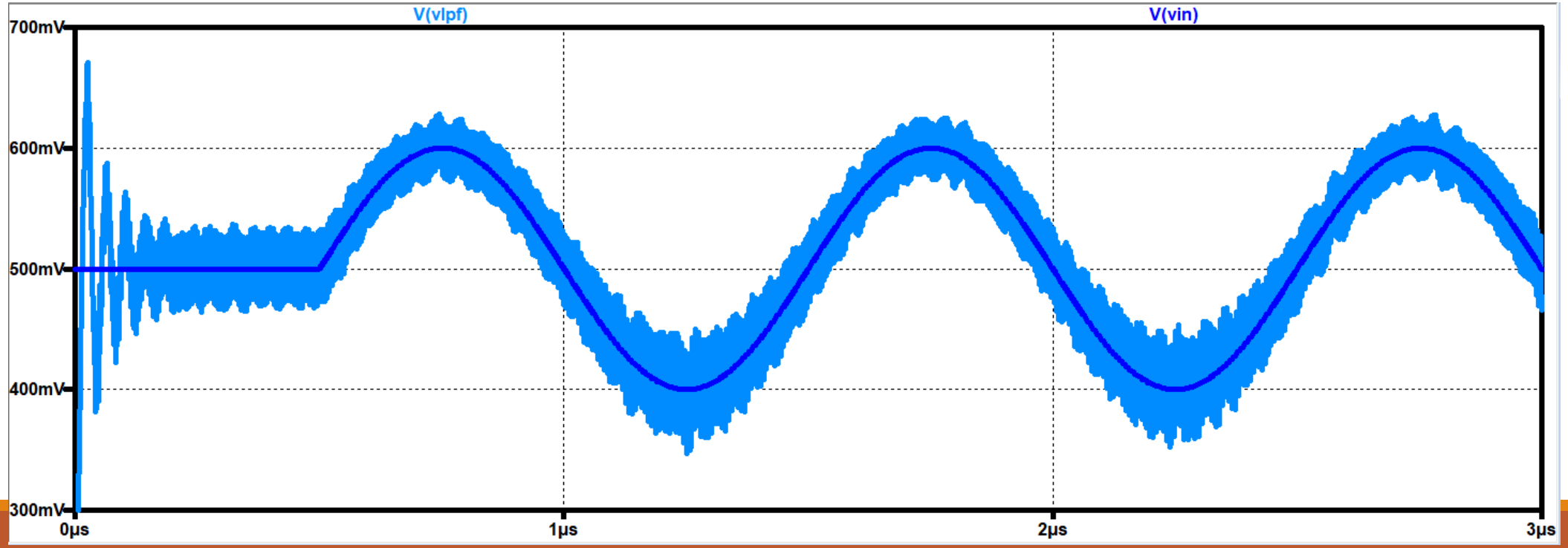
FM Demodulation

- The following experiment has been created, where the input signal is a low-frequency sine wave (1MHz) that feeds into a VCO and generates the FM signal. The APLL will take in the signal and the error will filter out harmonics which will result in a demodulated signal at V_{OSC} .



FM Demodulation

- V(vin) is the original signal, and V(vlpf) is the demodulated signal.
- There is some ringing and the signal still contains harmonics.
- This can be fixed by utilizing the lag-loop filter and adding an additional zero.



Lag-Loop Filter:

- The lag-loop filter has the following transfer function:

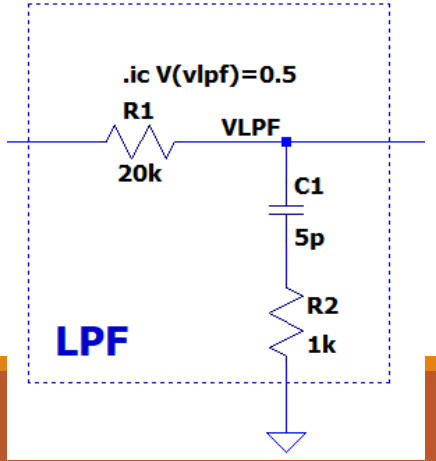
$$F(s) = \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}, \omega_z = \frac{1}{R_2 C}, \omega_p = \frac{1}{(R_1 + R_2) \cdot C}$$

- From above, if R2=0, we get the original RC circuit. If R1 is small, we see that we have a pole/zero cancellation (bad!!). When this occurs, its like the filter did not exist at all and all the harmonics pass through the VCO, defeating the purpose of the lag-loop filter.

- For general lag-loop design, R1 >> R2, and C can be tuned to decrease the bandwidth (filter more frequencies)

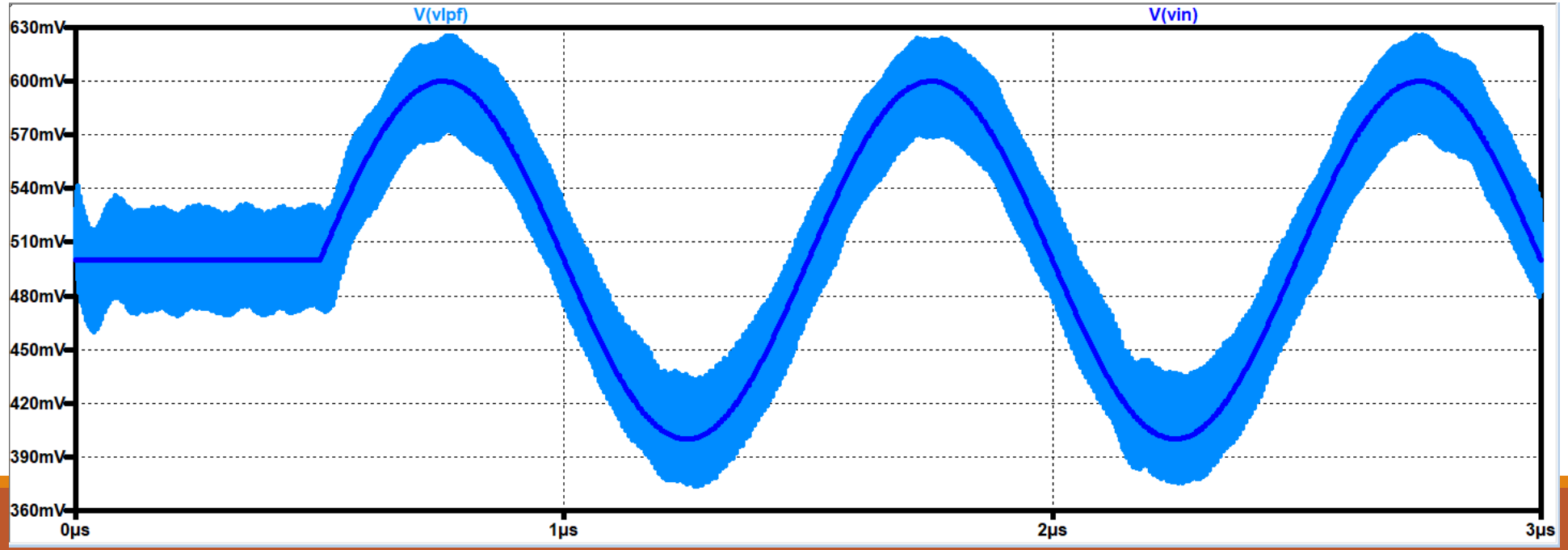
- For the Lag-loop, $\omega_z = \frac{1}{5ns} = 200MHz$ and $\omega_p \approx \frac{1}{100ns} = 10MHz$

- A value of R1=20k, C1=5pF, and R2=1k are chosen for the next simulation



FM Demodulation: W/Lag-Loop Filter

- By adding a lag-loop filter, the APLL has a better settling time and damping factor.
- The resulting signal is a cleaner demodulated signal, which can be filtered again to remove the high frequency harmonics.
- The values of the filter are chosen so that the capacitor is larger than what is used in a single-pole RC circuit, and the feed-forward resistance is high, else there is a pole/zero cancellation that effectively defeats the purpose of the lag-loop filter.



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