Radiation effects and Mitigation techniques on DRAM

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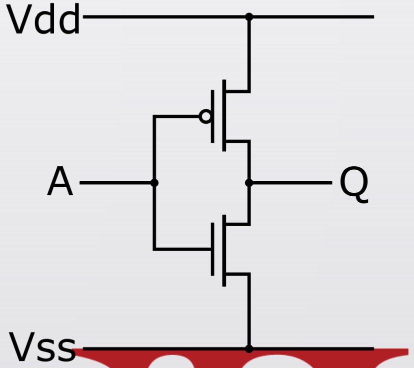


Objectives

Review	Radiation effects on MOSFETS
Present	Radiation Effects on DRAM
Show	Current Mitigation Techniques on DRAM

Radiation Effects on MOSFETS

Total Ionization Dose

- Total ionizing dose (TID) is the amount of energy deposited by ionization processes in the target material.

Displacement damage

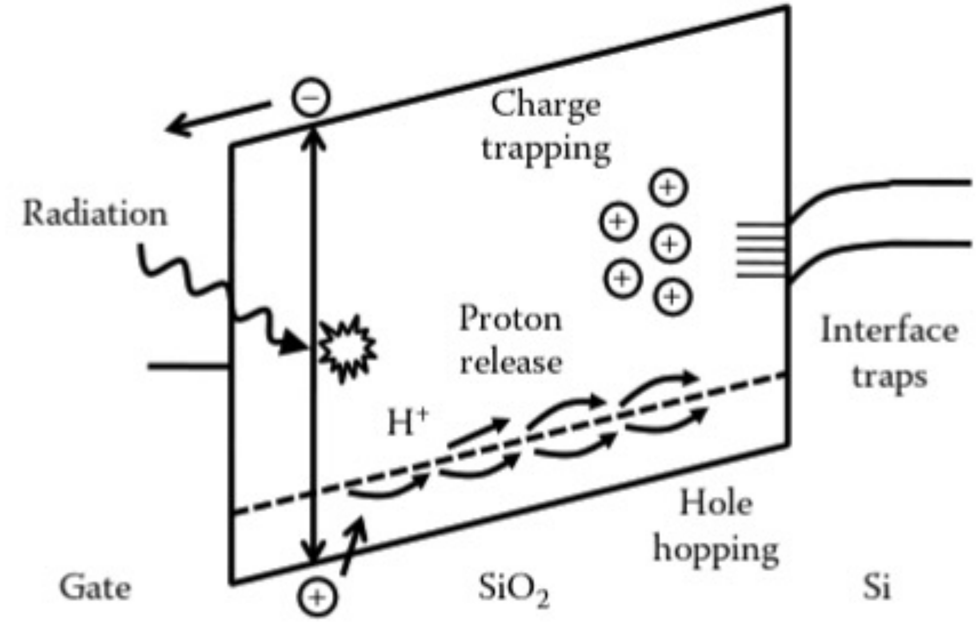
- Displacement damage (DD) is related to the displacement of atoms from the lattice of the target material by impinging particles due to Coulomb interactions and nuclear reactions with the target nuclei

Single Event Effect

- A single-event effect (SEE) is caused by the passage of a single, highly ionizing particle (heavy ion) through sensitive regions of a microelectronic device.

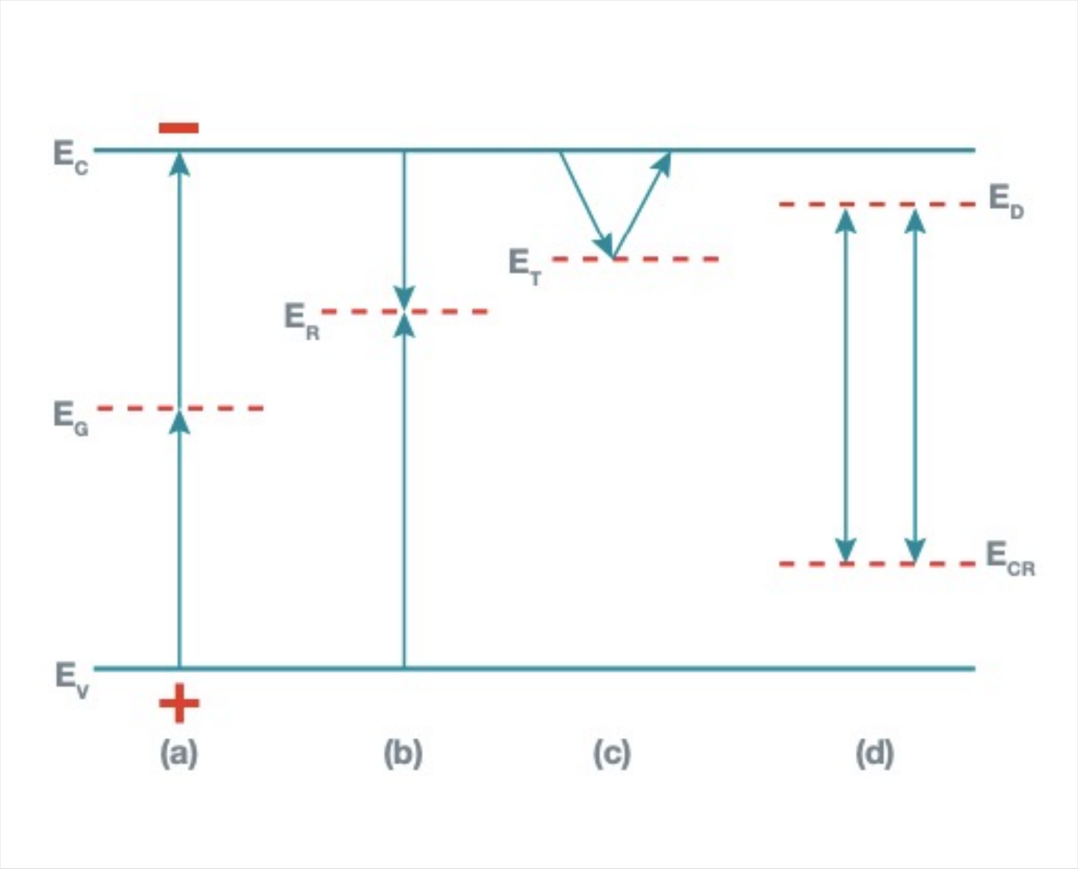
TID on MOSFETs

- Generates defects in insulating layers
- Buildup of (positive) trapped charge in insulating layers
- the MOSFET experiences shifts in the threshold voltage, decreases in transconductance, and leakage currents.



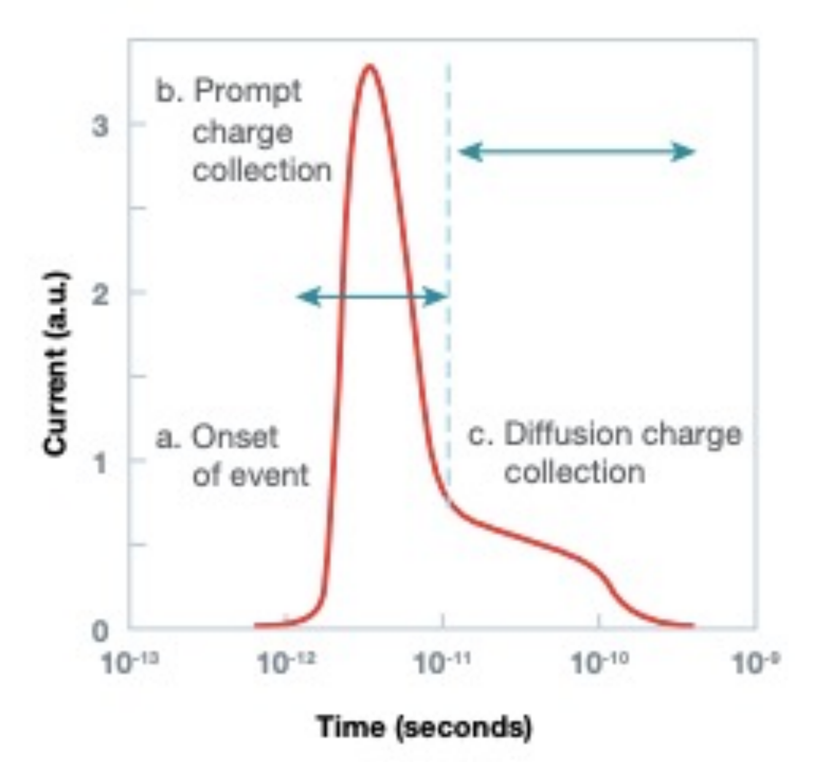
Displacement Damage on performance (Extra)

- Band-gap traps in silicon
- (a) increase recombination
- (b); and enhance free-carrier trapping
- (c); localized donor-acceptor trap pairs reduce free-carrier concentration

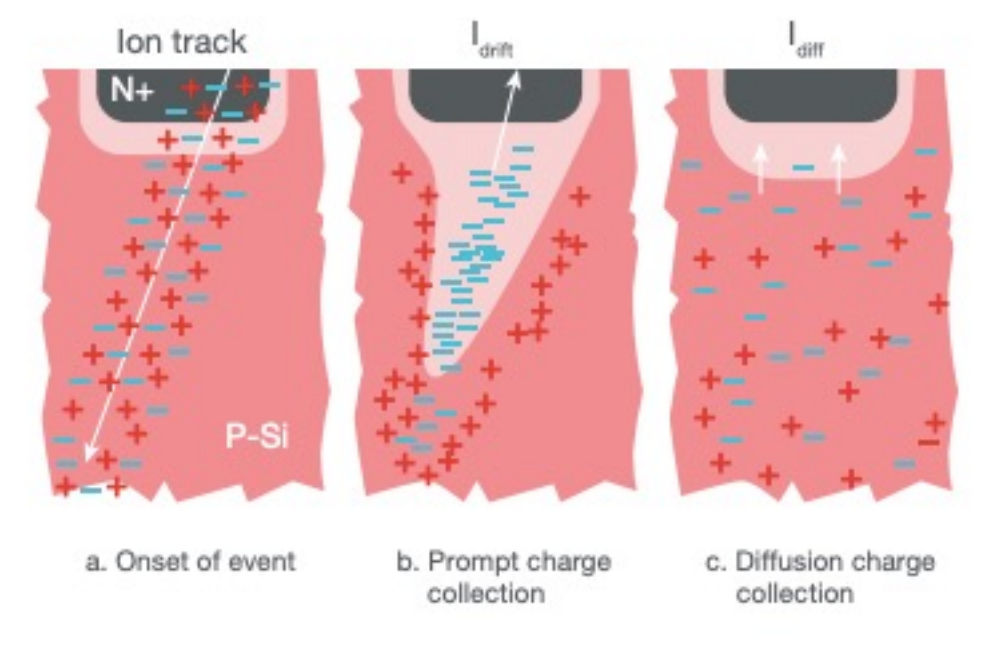


Single Event Effect (SEE)

current transient caused by the passage of a high-energy ion through the junction.



An ionizing radiation event results in ionization track,

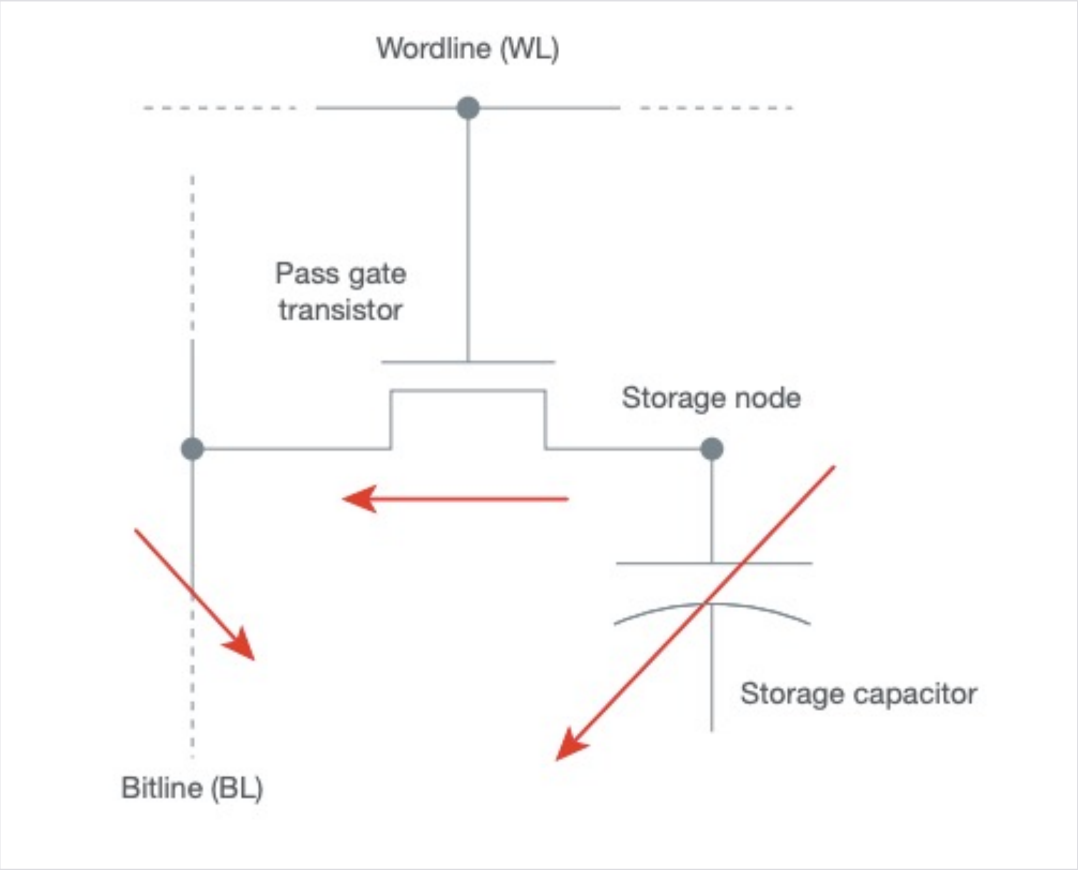


Radiation Effects On DRAM

- DRAM devices are subject to both total-dose and single-event effects (SEEs)
- SEEs commonly found in DRAM devices:
  - Single-event upsets (SEUs), which are isolated single-bit or multibit errors
  - Single-event functional interrupts (SEFIs), which are corrupted rows, columns, or whole address ranges
  - Single-event latch-up
  - Current increase

Single Event Upsets (SEU) in DRAM

- A strike in the read path can either cause a transient error or a persistent data error. Depending on which part of the circuitry is upset, it is possible that the erroneous value is written back to the array by the sense amplifier.

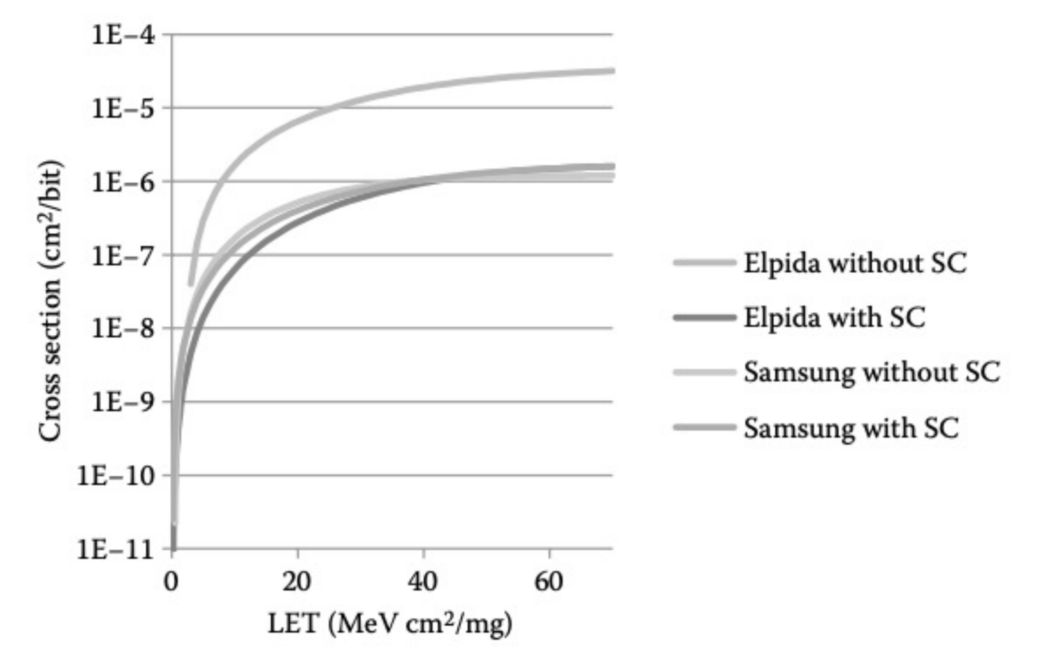


SEFIs and Burst Errors

SEFIs are caused by heavy-ion strikes in the control circuitry

Row SEFIs, corrupting either a single row of the device address space, part of a row, or multiple rows

Column SEFIs, corrupting either a single column of the device address space, part of a column, or multiple columns



Effect of software conditioning on the device SEFI cross section for two DDR3 SDRAM part types

Single-Event Latch-Up and Current Increase

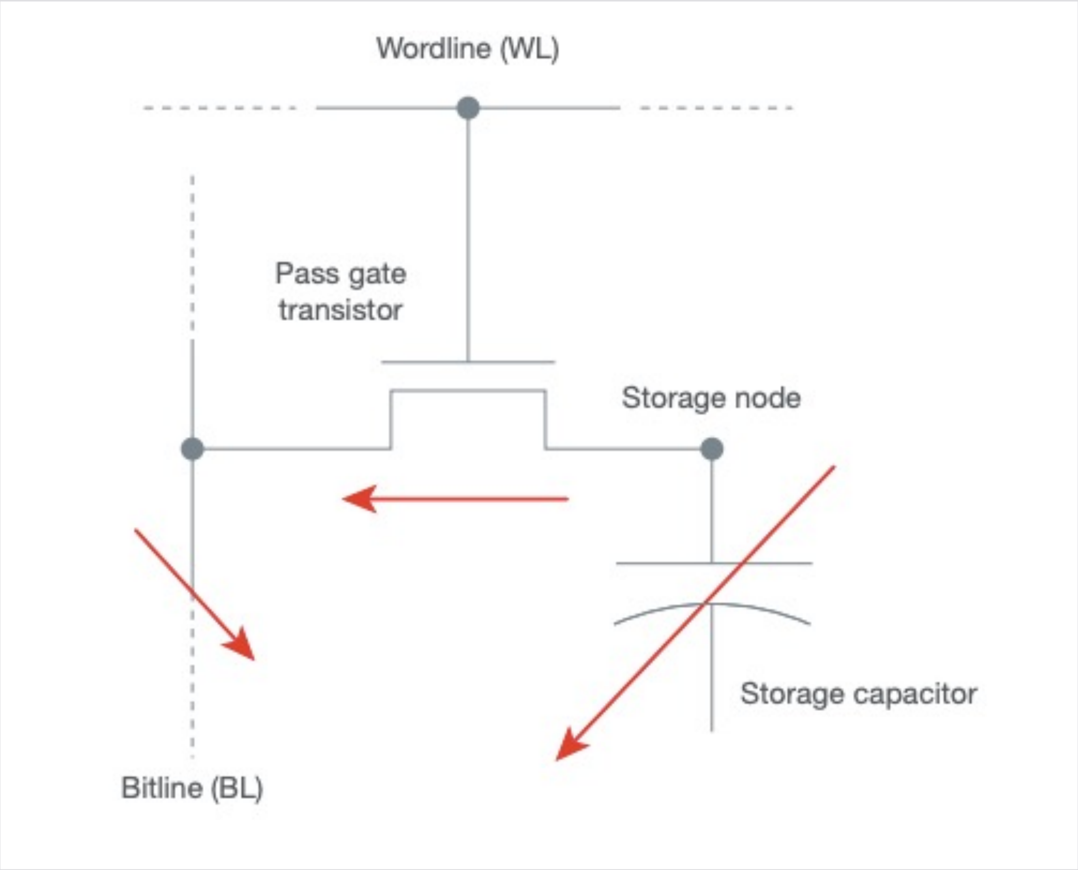
- Radiation can cause a latch-up (single-event latch-up [SEL]), which can in turn destroy the device
- increased operating current are distinguished from latch-up in that the current does not destroys the device

Total-Dose Effects on DRAM

- Total-dose effects commonly found in DRAM devices are:
- Decreased retention time, causing isolated errors
- Current increase
- Functional failure

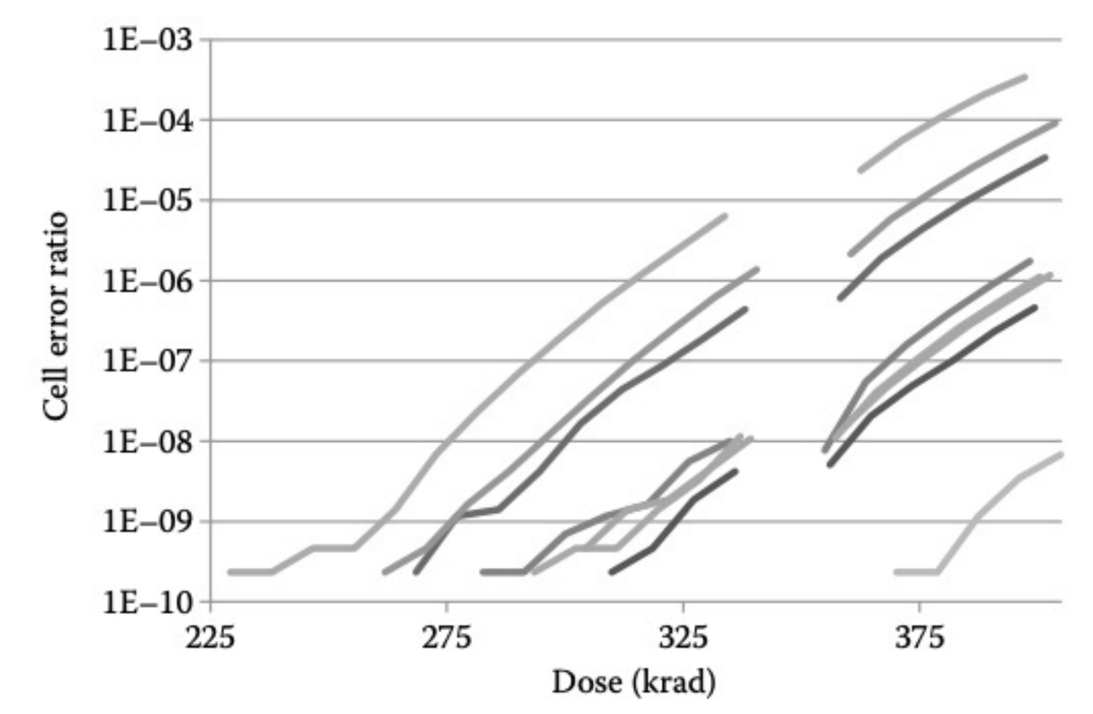
Retention Time

- The retention time is the time until the charge has leaked off the cell capacitor
- The refresh interval must therefore be shorter than the retention time or errors will occur
- Scheick et al. found, for a Toshiba 16-Mbit DRAM, that the median **retention time decreases** exponentially with absorbed dose



Data Errors

- When reading data from a device that has been exposed to photon radiation, errors occur.
- These errors are mostly randomly-distributed, single-bit errors.



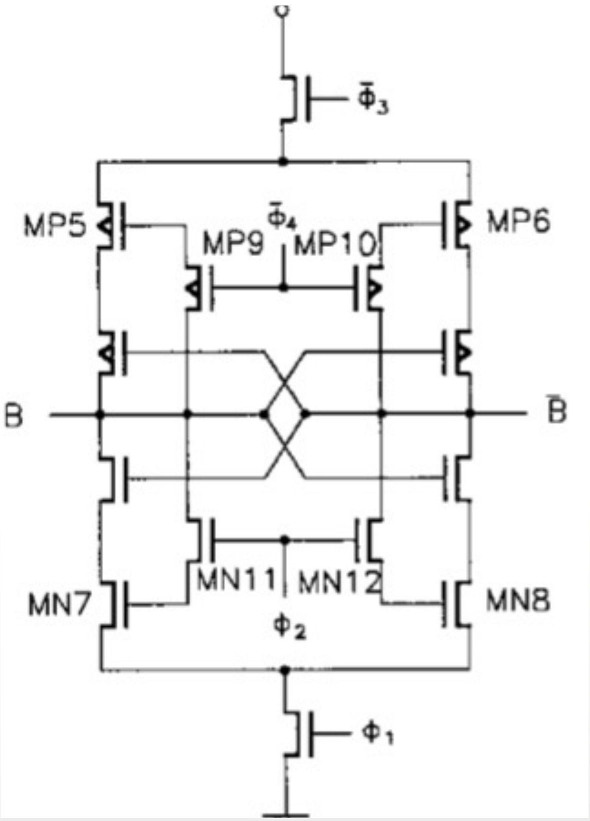
Errors in eight 4-Gbit Samsung DDR3 SDRAM devices during in situ ^{60}Co irradiation at room temperature

CURRENT INCREASE AND FUNCTIONAL FAILURE

- Operating current typically increases with received dose
    - Lee et al. [38] tested 64-Mbit DRAMs and found that, for a Samsung device, the standby current increased slightly up to 20 krad
- Functional Failure varies according to application

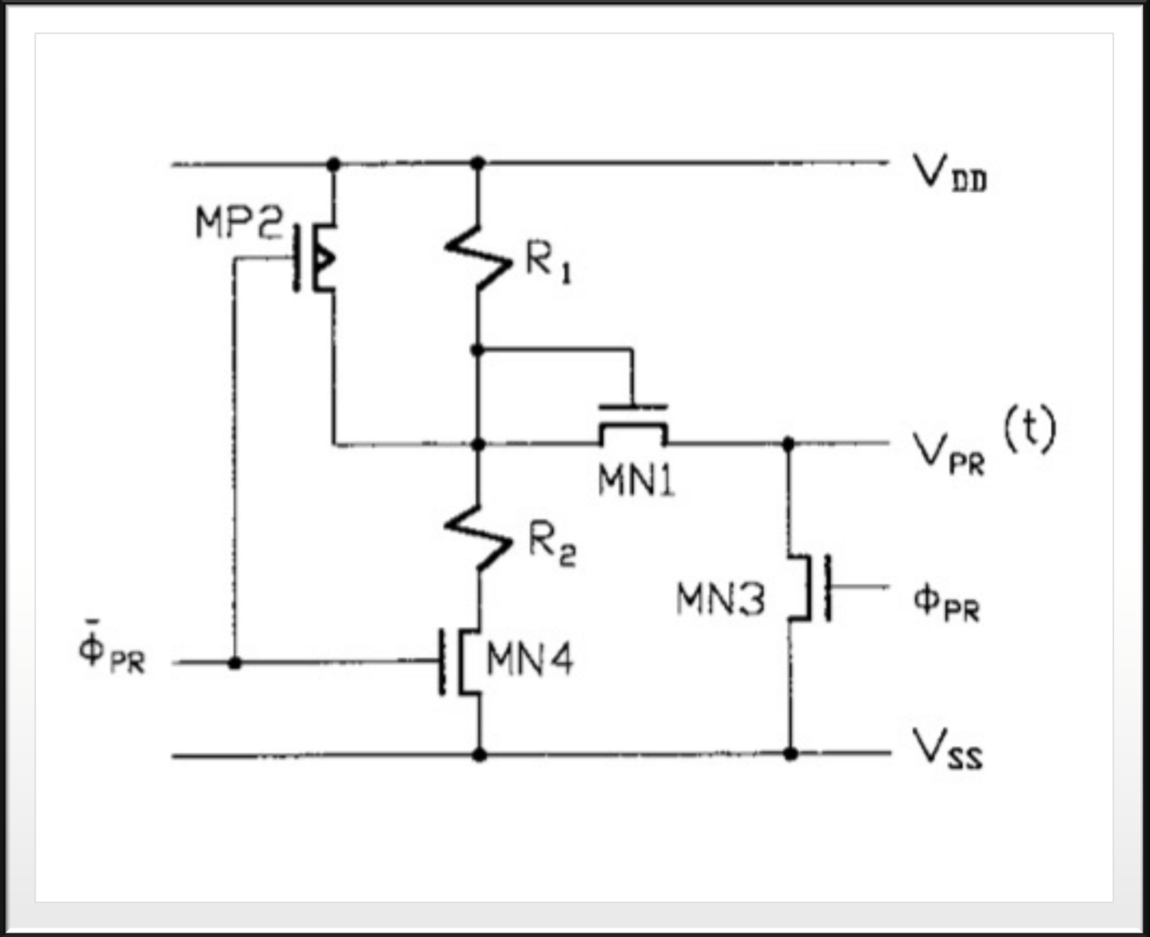
Hardened Sense Amplifier

- Sense circuit is the most susceptible circuit in the memory circuit
- To reduce radiation sensitivity differential amplifiers, self-compensation and voltage-bias limitation can used.
- The circuit is an example of a sample and feedback amplifier.



Parameter Tracking Reference Circuits

- Tracking threshold voltage improves radiations hardening
- The figure on the side shows a tracking circuit.
  - The circuit should follow the Vth of MN1 And the access transistors.

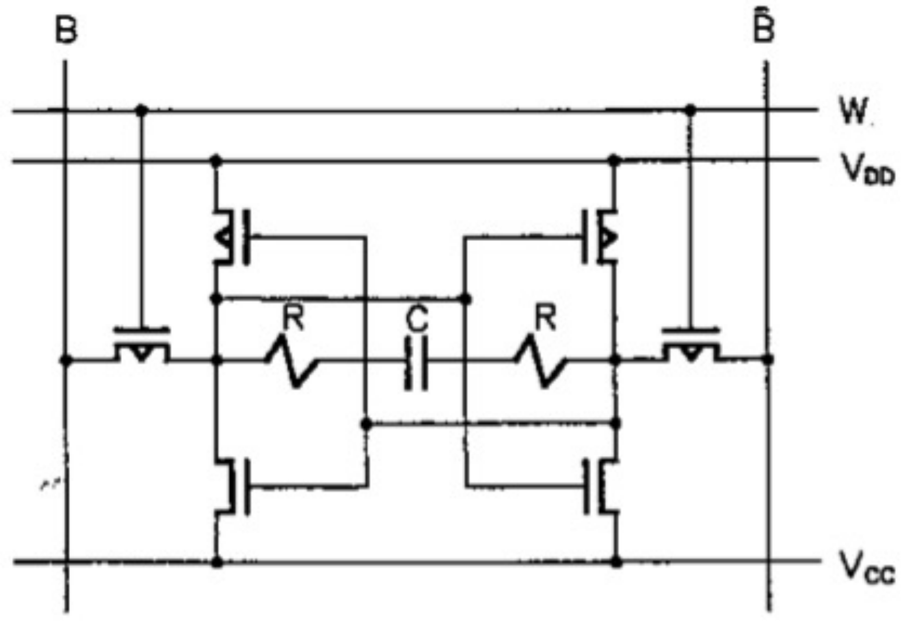


State Retention in Memory Cells

Radiation hard cells of choice is the 6T complementary static six transistor memory cells.

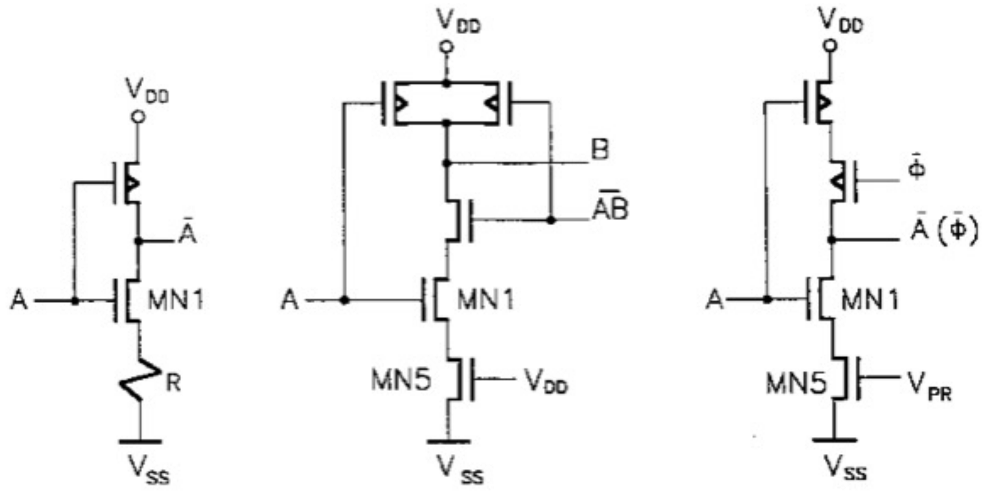
Irradiated p- devices become more negative under any bias conditions, while n-channel may increase or decrease

Additional capacitance and resistors increases t = RC and reduce spurious current



Self Adjusting gates

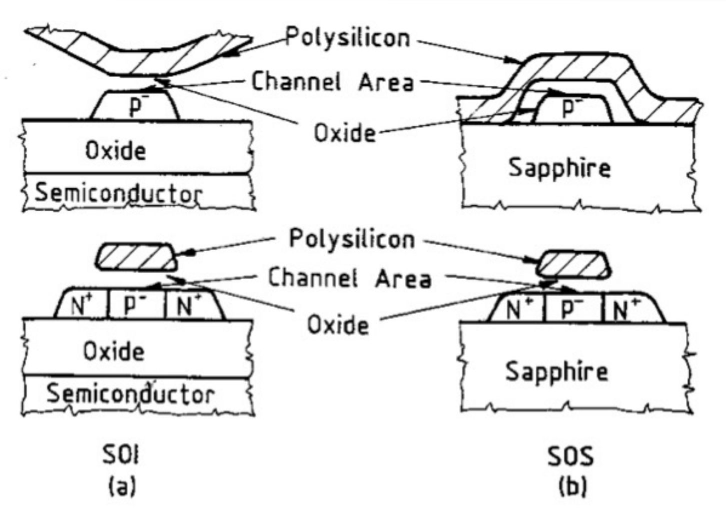
- CMOS periphery circuits are less sensitive to TID.
- Noise margins can be compensated
- A single resistor or a transistor (MN5 on the figure) is sufficient to compensate Vth and I-leakeage

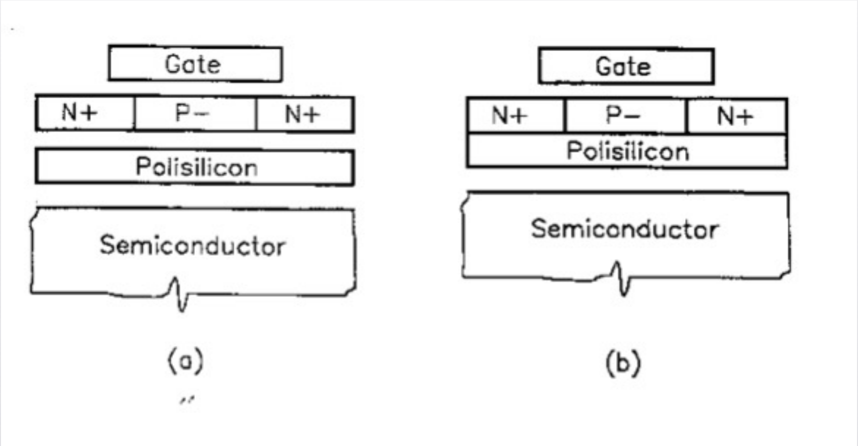


Process to decrease SET on CMOS

CMOS Silicon on Sapphire is sometimes used to reduced SET and TID damage

It has high current drive (PD devices_, low subthreshold leakage current and high saturation resistance (FD Devices)





References

- [1] *Ionizing Radiation Effects in Electronics : From Memories to Imagers*, edited by Marta Bagatin, and Simone Gerardin, Taylor & Francis Group, 2015. *ProQuest Ebook Central*, http://ebookcentral.proquest.com/lib/unlv/detail.action?docID=4097033. Created from unlv on 2021-12-03 10:49:34.
- [2]R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," IEEE Trans. Device Materials and Reliability 5(3), Sept. 2005, pp. 305-316. 2
- [3]C. M. Hsieh, P. C. Murley and R. O'Brien, "A field-funneling effect on the collection of alpha-particle-generated carriers in silicon devices," IEEE Trans. Electron Device Letters 2(4), Dec. 1981, pp. 686-693.
- [4] Haraszti, T. P. (2002). *Cmos memory circuits*. Kluwer Academic.
- [5] Baumann, R., & Kruckmeyer, K. (2020). *Radiation Hanndbook for Electronics*. *Texas Instrument* (A, Vol. 1). Texas instruments.

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