Sense Amp Circuit for a flash memory device

A case study of Patent US6490199B2

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Flash memory

- In 1984, Fujio Masuoka, a Japanese engineer at Toshiba invented the electrical storage medium that does not require any energy.
- The fast erasure of the memory reminded him of the camera “flash”
- The flash memory is non-volatile device that uses floating gate MOSFET to trap the charge in between the floating gate.
- Logic 1 is when there’s no charge trapped and cell is erased. The flow of current is interpreted.
- Logic 0 is when there’s charge trapped. The threshold voltage is interpreted.

NAND and NOR flash

- In NAND flash, all memory cells are aligned in a string to pull down the bit line.
- In NOR flash, at least one memory cell should be set to bring down the bit line.
- NOR flash uses more space than NAND flash, and is more expensive.
- NAND flash has slow reading than NOR flash.
- NOR flash makes random access possible, good for program storage
- NAND flash is good for high-capacity data storage.
- NOR flash has slower erasure than NAND flash.

Sense Amplifier

- Sense Amp is an analog circuit, basically a differential amplifier.
- It detects the difference between bitline and bitline bar faster.
- There are one sense amp per column.
- Bitline and bitline bar will be inversely related.
  - Common mode = VDD/2
- Flash sense amp detects whether a memory cell is in a conducting or non-conducting stage.

Patent No.6490199 B2

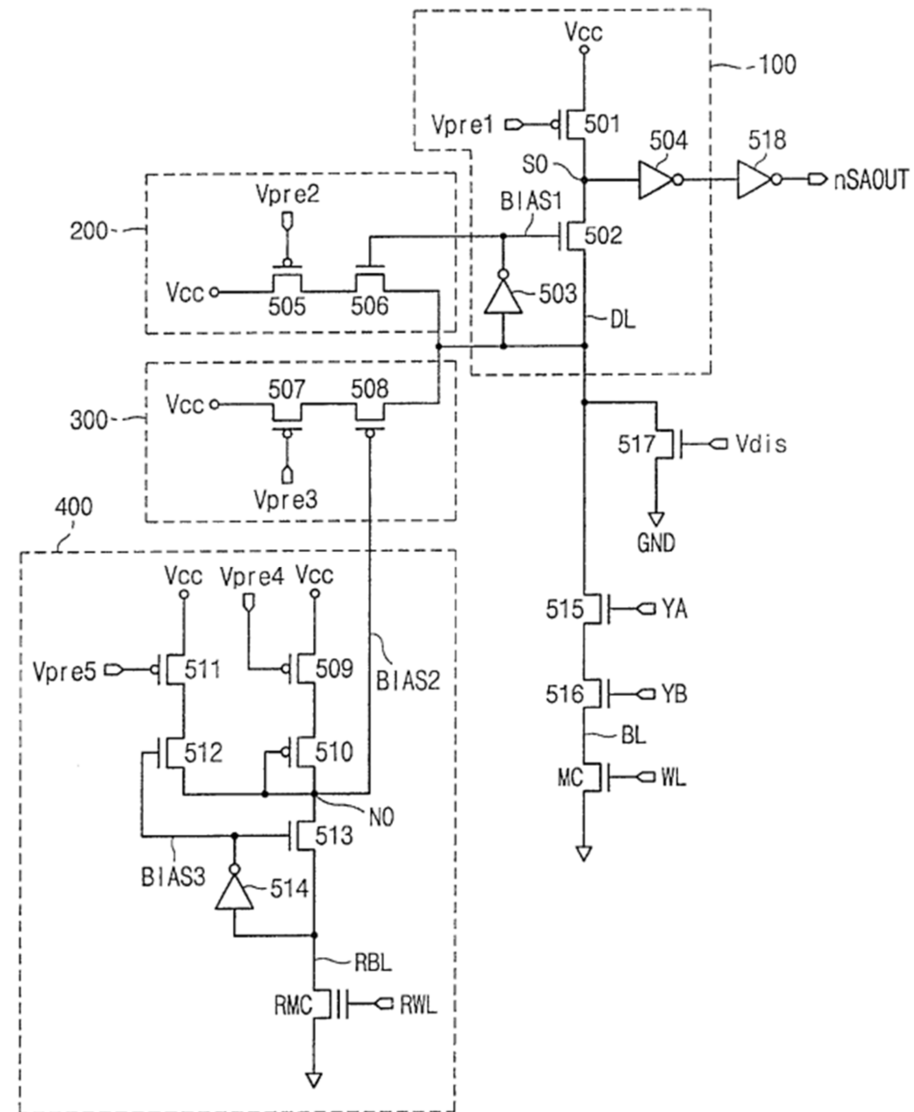
- Name: Sense Amplifier Circuit for a Flash Memory Device
- Inventors: Byeong-Hoon Lee, Young-Ho Lim
- Assignee: Samsung Electronics Co. Ltd.
- Filed: May 30, 2001
- G11C16/28: Sensing or reading circuits; Data output circuits using differential sensing or reference cells, e.g. dummy cells

Claim

- a sense amp that has:
  - a bias circuit for generating a constant bias voltage during pre-charge period.
  - A first pre-charge circuit for providing a variable current to data line, the variable current changing with a voltage fluctuation of data line
  - A detecting circuit connected to data line for sensing the voltage fluctuation of bit line during a sensing period, and for generating data signals corresponding to the on/off state of selected memory cell.

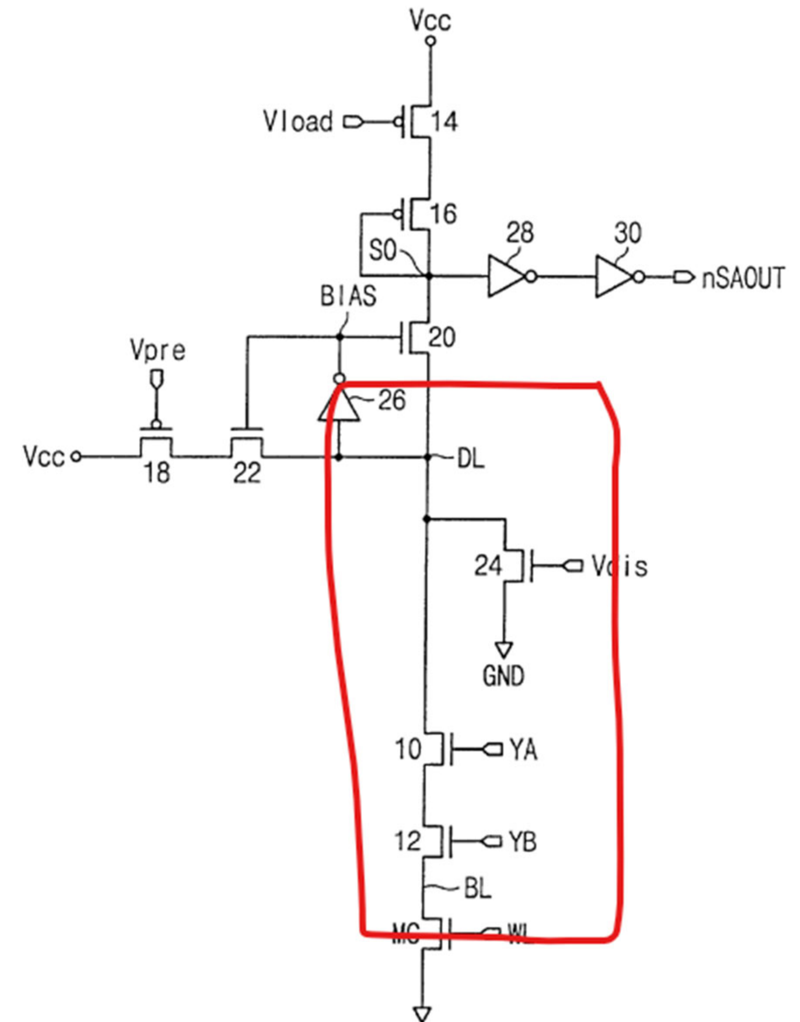
Abstract

- A sense amp circuit is used in flash memory cell to detect whether it is in a conducting or non-conducting stage.
- The conventional sense-amp is a single-ended type.
- The proposed sense amp circuit includes first and second pre-charge circuits for pre-charging a data line.
- The first pre-charge circuit provides a current changed by a fluctuation of the data line voltage to the data line, and the second pre-charge circuit provides a constant voltage regardless of the fluctuation of the data line voltage to the data line.



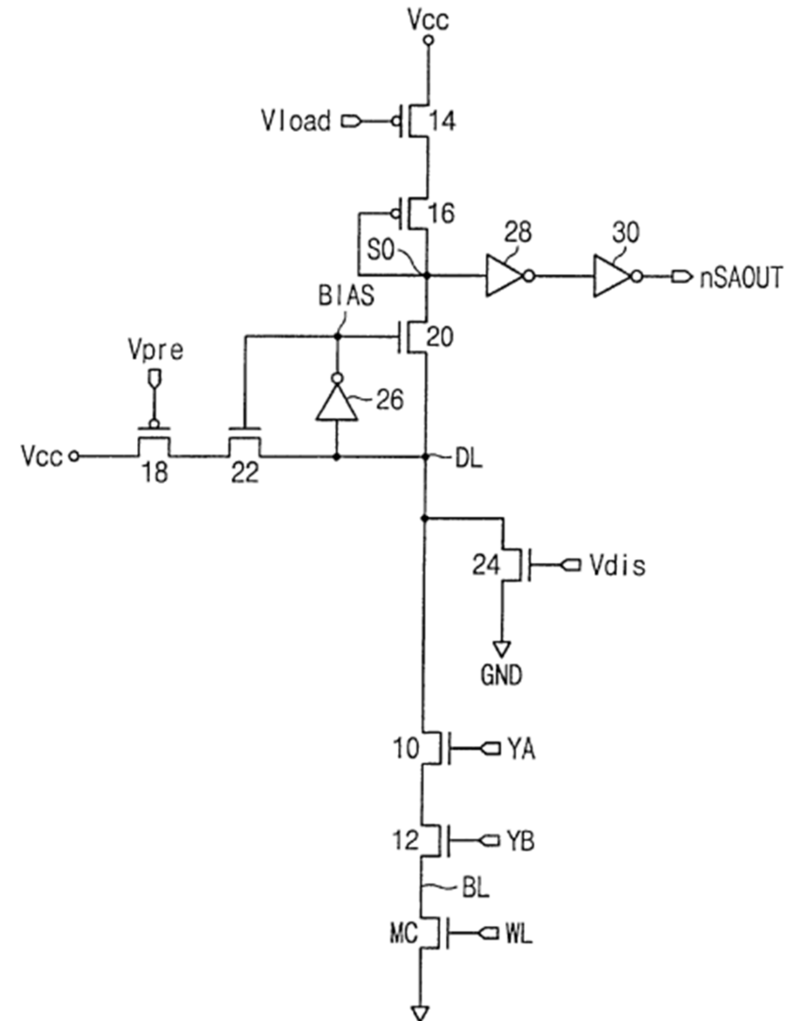
Prior art(1)

- A prior art sense amp is of a single-ended type.
- It is electrically connected to a bit line BL through NMOS 10 and 12, which compose a decoding circuit that couples the BL to a data line DL.
- An EEP memory cell MC is connected to the BL.



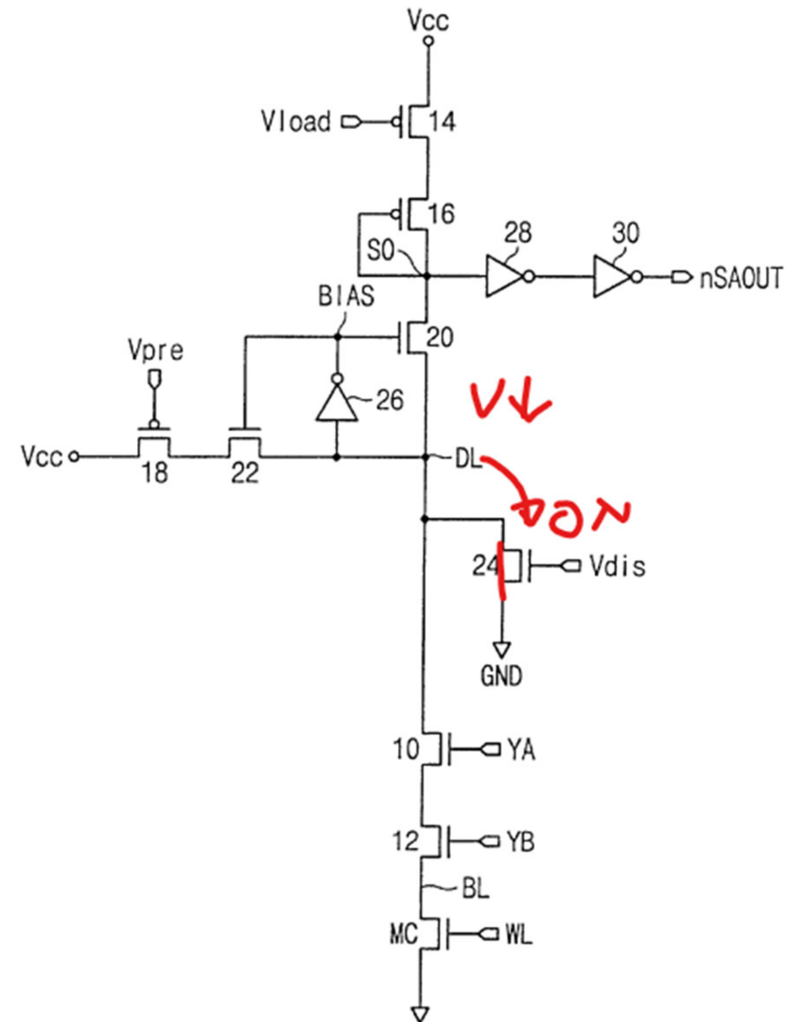
Prior art(2)

- Vcc is a power supply voltage.
- SO is a sense node.
- Vload is a load control signal.
- Vpre is a precharge control signal.
- nSAOUT is a detection on the SO.
- Vdis is a discharge control signal.
- YA/YB are row address decoding signals.



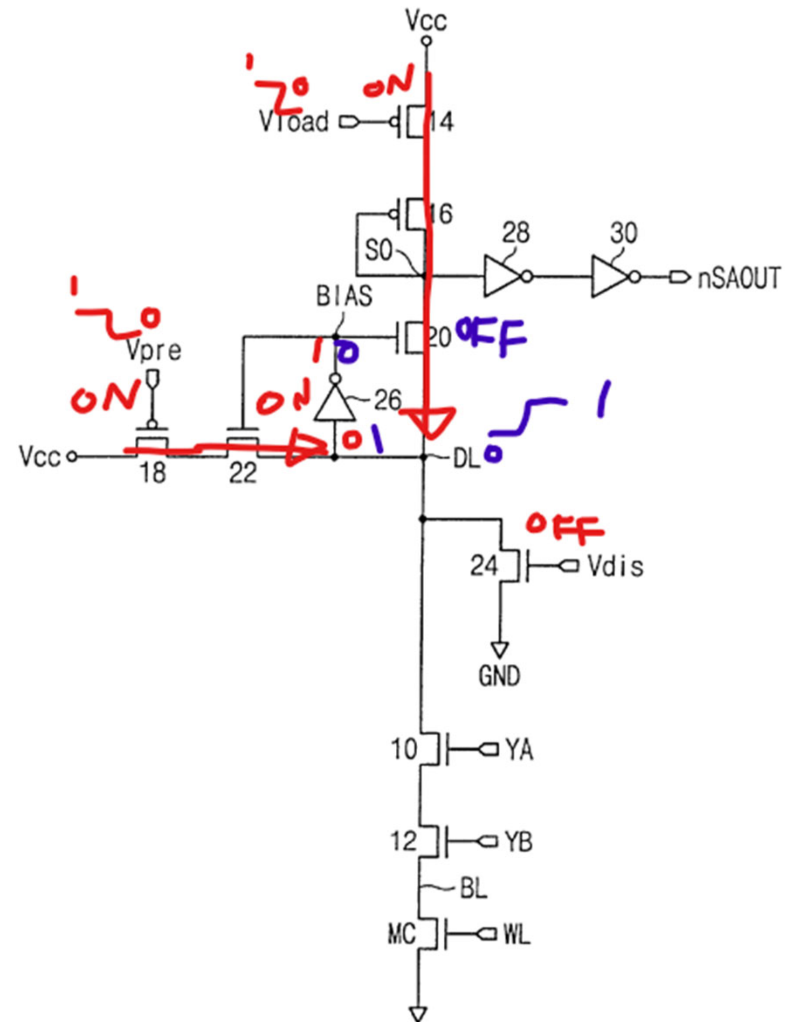
Prior art(3)

1. Vdis is activated high.
2. The voltage of the DL is discharged.
3. DL voltage is initialized to lower than 0.5V.
4. After some time, Vdis is activated low.



Prior art(4)

5. After discharging, Vpre is activated from high to low.
6. Current flows from the Vcc to the DL.
7. The DL voltage increases.
8. The Vload is activated from high to low.
9. As the DL voltage increases, output voltage BIAS starts to attenuate in proportion to the increase of the DL voltage.



Prior art(5)

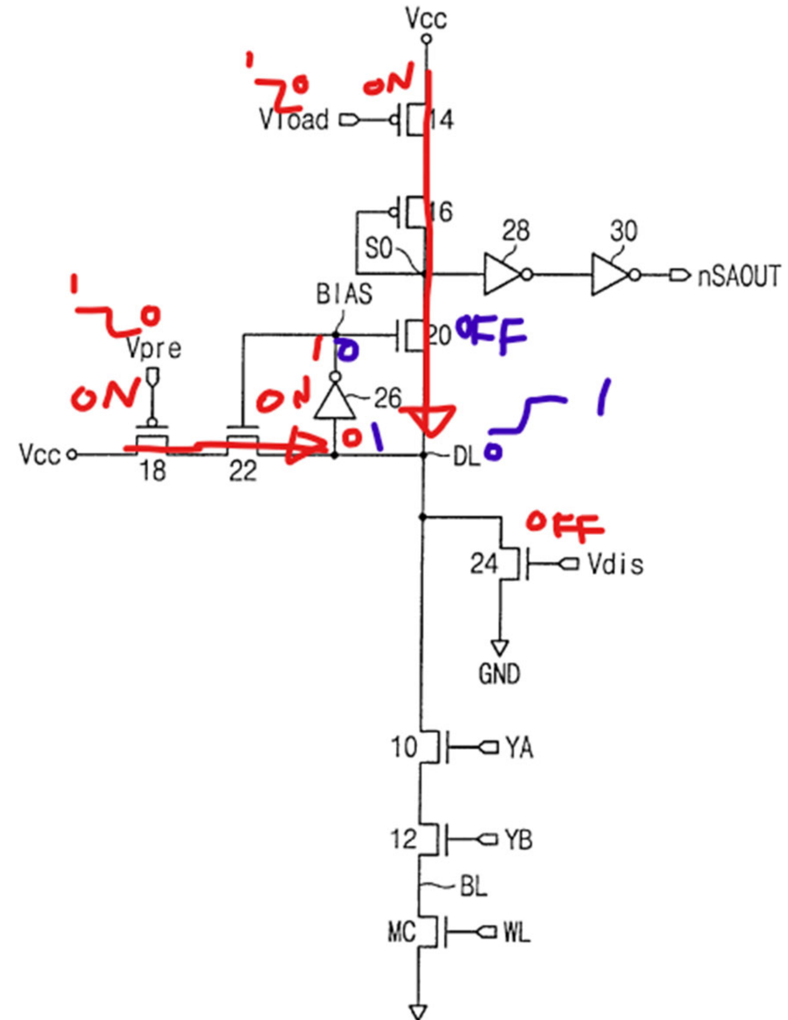
10. The current from NMOS 20 & 22 to the DL decrease by the attenuation of the output voltage BIAS.

11. The DL voltage is changed to a predetermined voltage level, e.g. 0.8V.

12. Vpre is inactivated to high.

(Vload can be designed to be activated to the low at the same time).

13. When the WL voltage increases, the DL voltage is increased or decreased based on the state of the memory cell (whether the cell is conducting or non-conducting state).



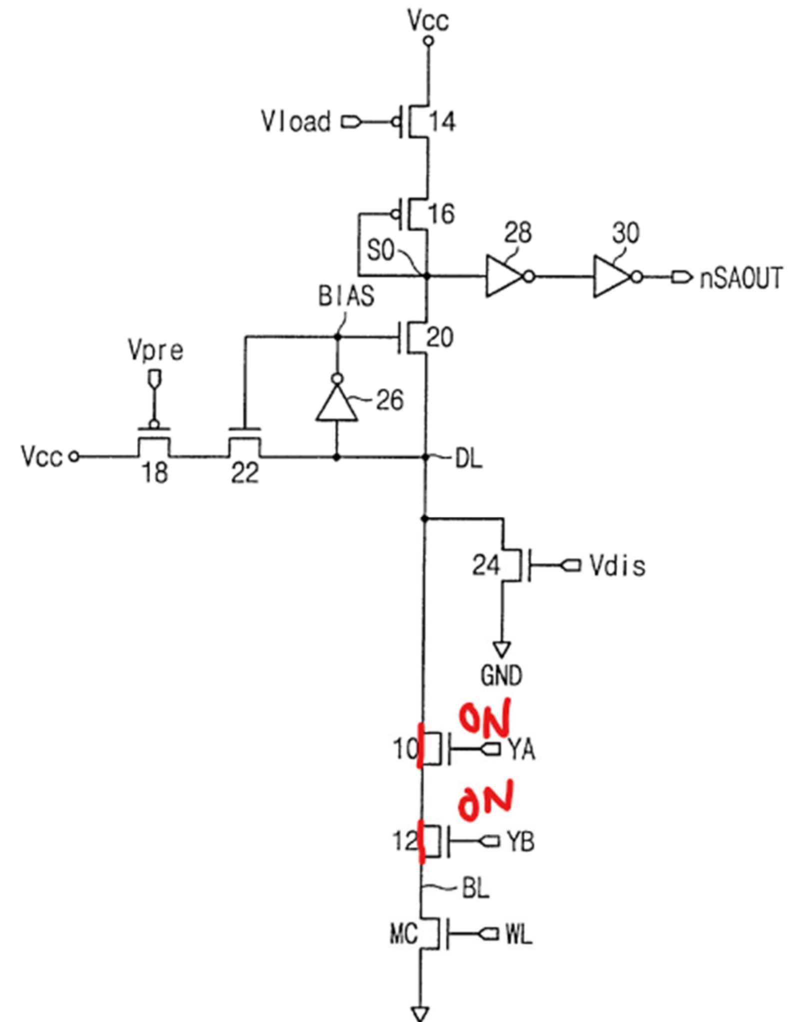
Prior art(6)

14. The address is changed to select a memory cell.

15. YA and YB are activated to high.

16. This turns on the NMOS 10 and 12.

17. When they are turned on, DL and BL are electrically connected.

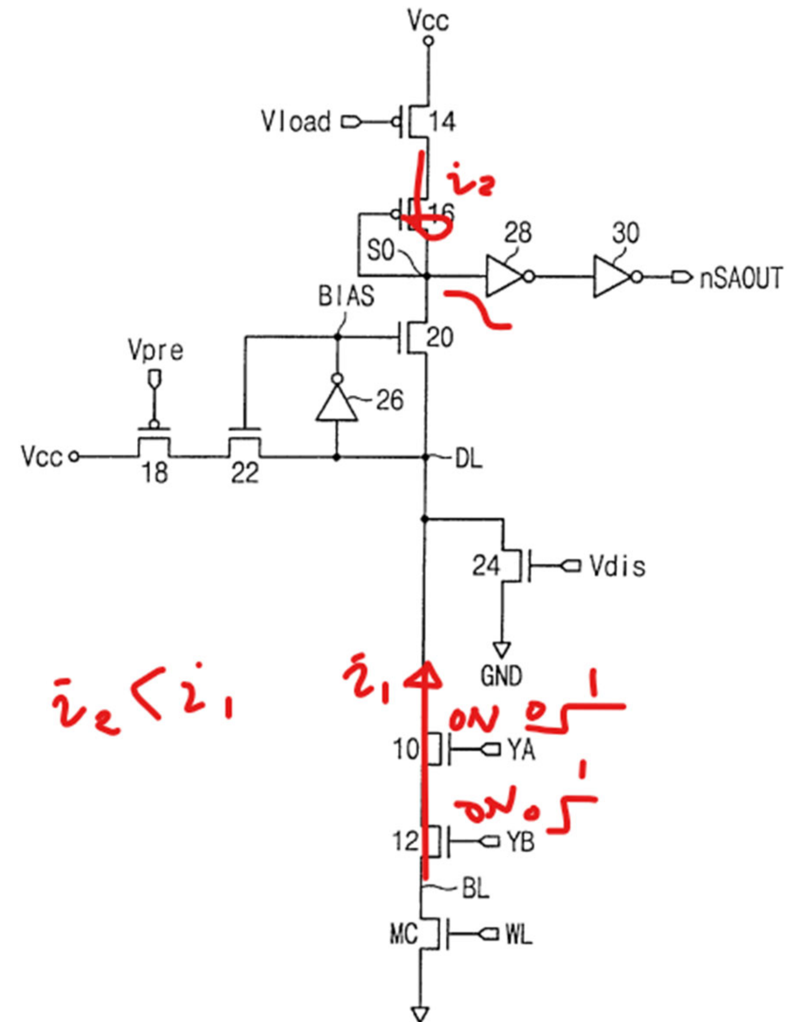


Prior art(7)

18. A current in the conducting state is typically designed to be larger than a current from MOSFET 14 & 20.

19. Then the voltage of the SO is attenuated by the DL voltage to be lower than that of the precharged voltage.

20. The SO voltage is converted into a digital signal nSAOUT.



Prior art(8)

21. If the memory cell is in a non-conducting state, then the current does not flow through the memory cell.

22. The current flows to the DL and the SO through the load PMOS 14.

23. The SO voltage is increased.

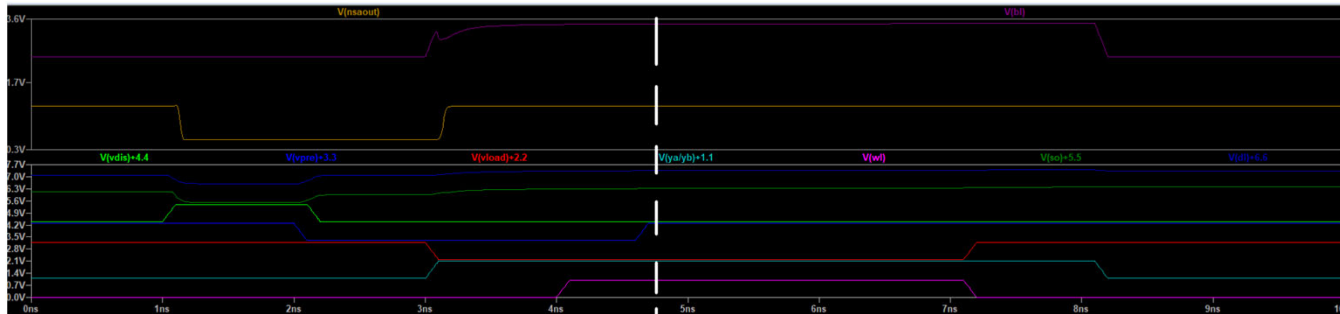
24. The SO voltage is converted into a digital signal nSAOUT.

Prior art(9)

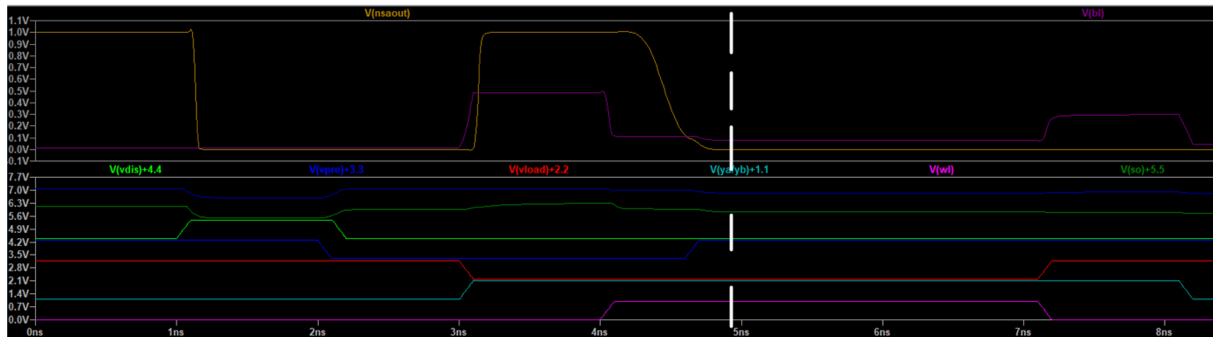
Problems:

- In a latter part of the pre-charge period, the output BIAS voltage is attenuated by the increased DL voltage.
- A difference between the source voltage of NMOS22 and the gate voltage BIAS is reduced where a current I22 is sharply attenuated.
- It typically takes more time to pre-charge the DL to a desired voltage.

Prior art simulation



When the current from BL is greater(conductive), the nSAOUT is logic 1 during the sensing



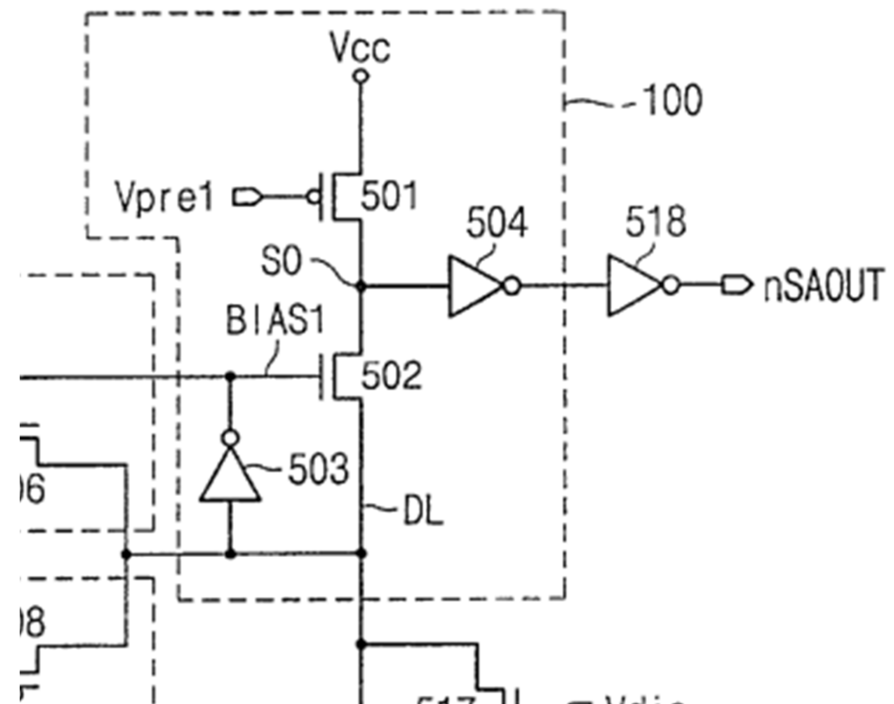
When the current from BL is zero(non-conductive), the nSAOUT is logic 0 during the sensing

Preferred embodiments(1)

- The setup:
  - A data line DL is electrically connected to a bit line BL through NMOS 515 and 516.
  - NMOS 515 and 516 are connected to the DL and compose a decoding circuit.
  - The number of memory cell is more than 1 in a typical Flash memory(1 here)
- Part 100 is a detecting circuit.
- Part 200 is a first pre-charge circuit.
- Part 300 is a second pre-charge circuit.
- Part 400 is a bias circuit.
- NMOS 517 and Vdis is activated during a discharge period.

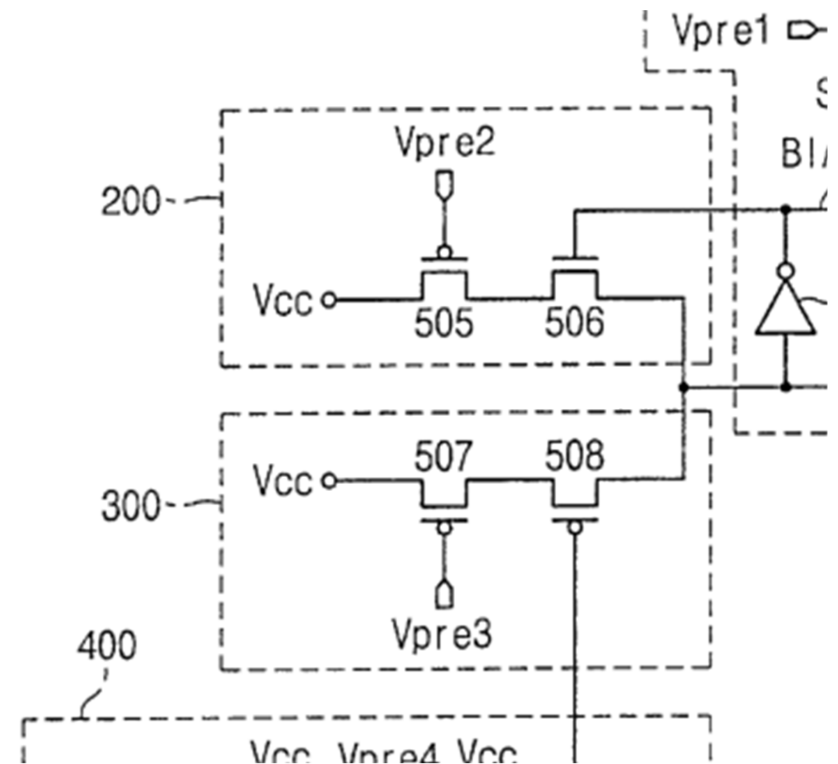
Preferred embodiments(2)

- Detecting circuit(100):
  - Electrically determine a high signal or low signal in response to a BL voltage level.
  - It includes a PMOS 501 as a load transistor.
    - Receives a Vpre1 control signal.
  - It includes an NMOS 502 as an insulation transistor.
    - Controlled by an output voltage of the inverter 503.
  - Inverter 503 functions to maintain the bias voltage BIAS1 to be a constant voltage level.
  - Inverters 504 and 518 are for digital signal output.



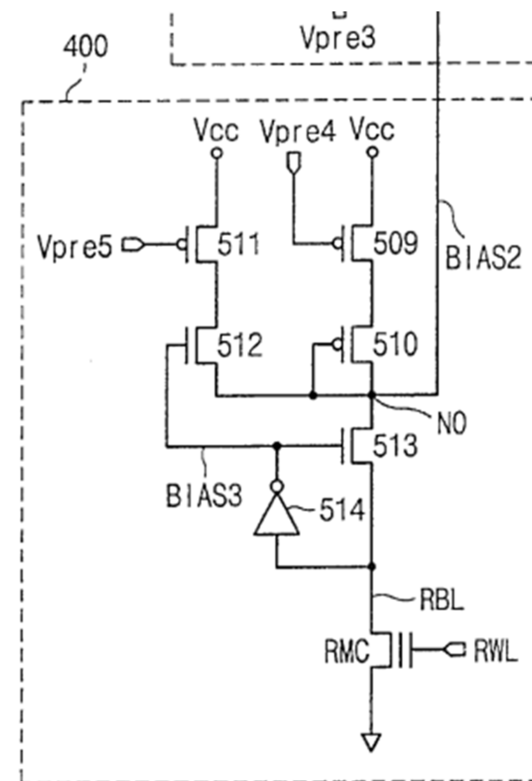
Preferred embodiments(3)

- First and second pre-charge circuit(200, 300):
    - First pre-charge circuit is connected to DL and provides a current to DL during the pre-charging period.
    - Second pre-charge circuit is connected to DL and provides a current to DL that doesn’t change when the voltage of DL fluctuates during the pre-charge period.
        - The PMOS 508 is controlled by a bias voltage BIAS2 from the bias circuit(400).



Preferred embodiments(4)

- The bias circuit(400):
  - RMC is a reference memory cell.
  - The output node NO generates the bias voltage from the PMOS 509 and 510.
  - The PMOS 510 is controlled by NO.
  - RBL is a reference bit line.
  - The PMOS 509 is controlled by Vpre4 and the PMOS511 is controlled by Vpre5.
  - The NMOS 513 is connected between the NO and RBL.



Preferred embodiments(5)

- The PMOS 510 and 508 make a current mirror.
- A current flowing through the PMOS 508 can be controlled by other form of bias circuit:
  - 4A uses a fuse.
  - 4B has an Adjusting circuit That uses switch Control signals.

Fig. 4A

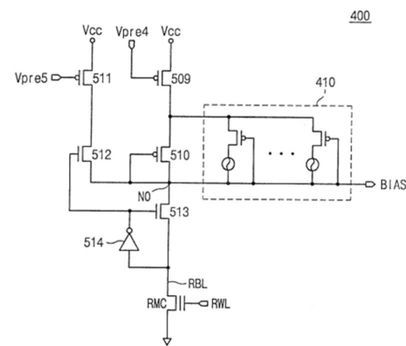
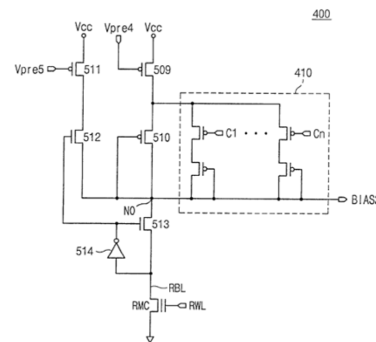
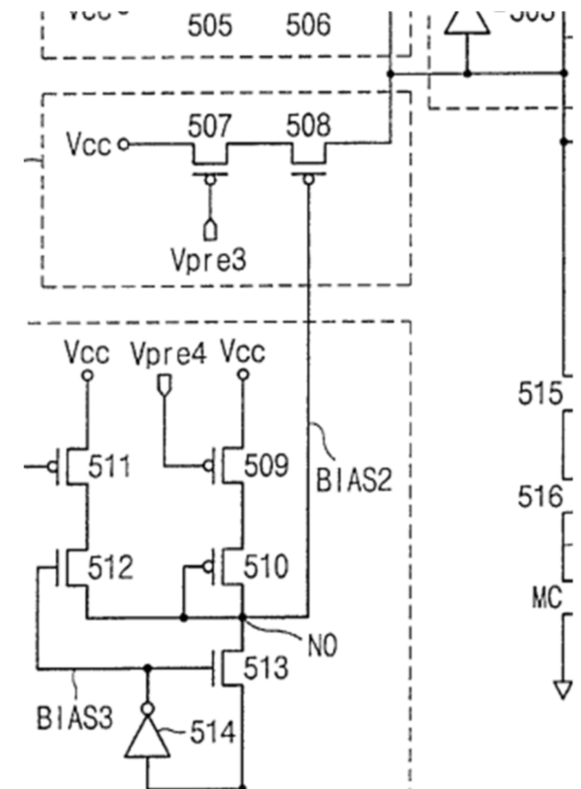


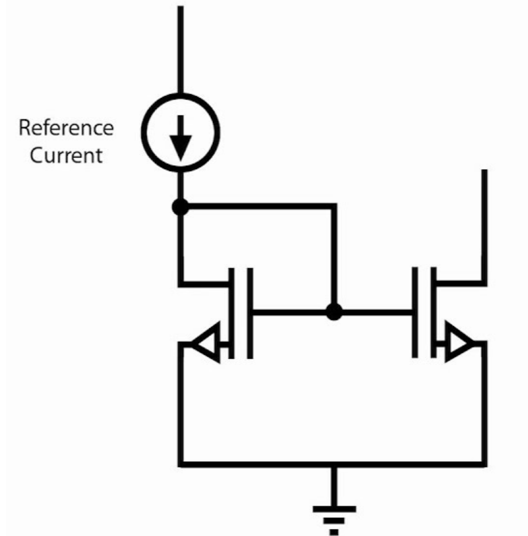
Fig. 4B





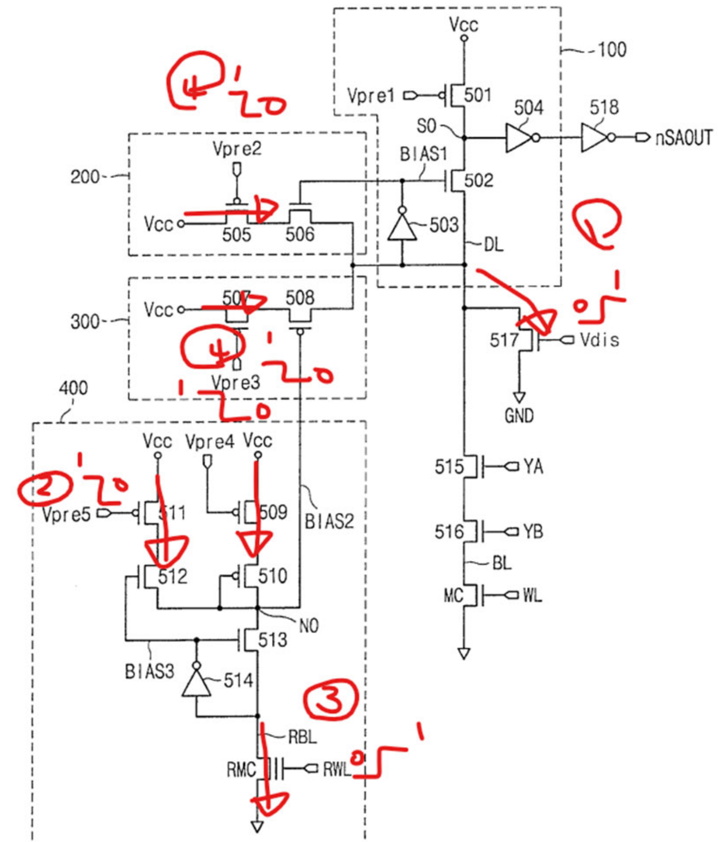
Preferred embodiments(6)

- Current meter:
  - It's hard to maintain the bias voltage.
  - Also the drain current is based on the temperature.
  - A current generated from a reliable source is copied with the current meter.
  - By connecting the drain and gate, Vgs is proportional to the reference current.
  - Vd = Vg, Vds >= Vgs – Vth : saturation region
- By generating the W/L ratio, the multiple can be adjusted



Preferred embodiments(7)

1. Before the decoding, Vdis is activated to the high level for discharging the DL voltage.
2. The DL voltage is initialized to lower than 0.5V.
3. The pre-charge signals Vpre-Vpre4 are all activated low and then the RWL is activated high.
4. Pre-charge signal Vpre5 is activated low in between the DL voltage discharge and the other pre-charge signals.



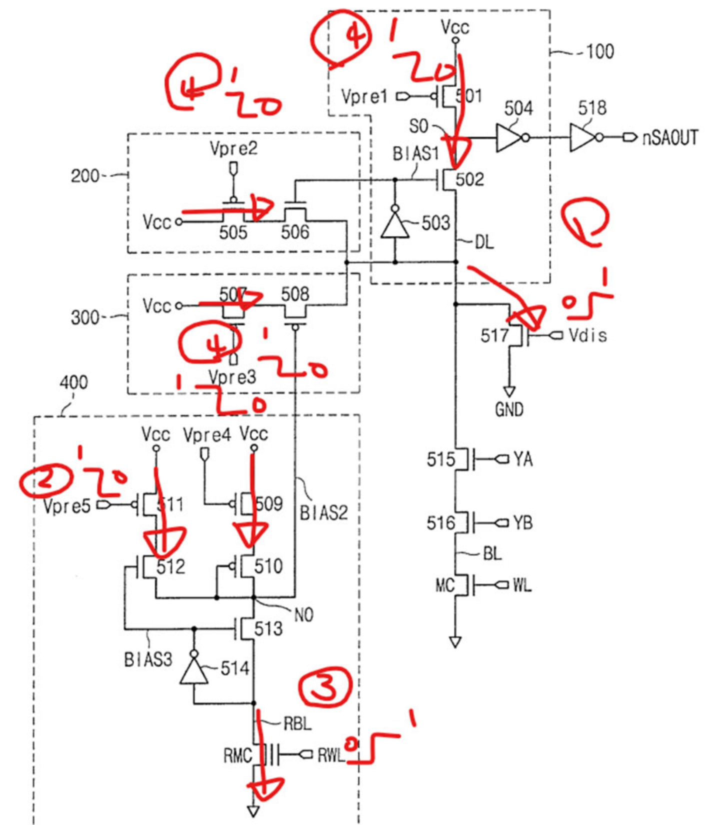
Preferred embodiments(8)

5. When Vpre4 and Vpre5 are activated, the bias circuit 400 provides a constant level bias voltage BIAS2 to the second pre-charge circuit 300.

6. A current flows from Vcc to the DL and from first pre-charge circuit 200 to the DL.

7. A current also flows from the detecting circuit 100 as well.

8. The voltage of the DL starts to increase from all the current supplies.



Preferred embodiments(9)

9. Then, the output voltage BIAS1 starts to attenuate in proportion to the DL voltage increase.

10. A current Ii flowing throught the detecting circuit and the first pre-charge circuit gradually decreases from that attenuation.

11. In the latter half of the pre-charge period when the DL voltage is changed to a level like 0.8V, the current I1 is sharply decreased.

12. A current I2 flows through the PMOS 507 and 508 of the second pre-charge circuit 300 flows regardless of the voltage increase of the DL.

13. When the pre-charge is finished, the signals are inactivated.

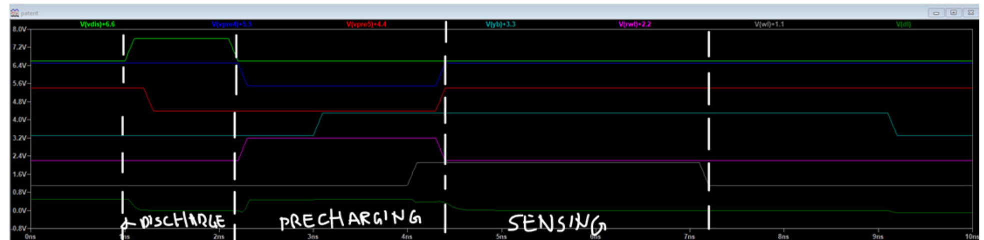
14. RWL is inactivated to low level.

Preferred embodiments(10)

15. During the pre-charge period, the gate voltage and drain voltage is reduced where a current through the NMOS 506 is decreased.

16. When a voltage of the WL is increased, the voltage of the DL is increased or decreased based upon the state of the MC.

17. If the MC is in a conducting state, then a voltage of the DL is lower than pre-charge voltage. And vice versa.



The MC is in a conducting state,
And the voltage of DL is lower than
Pre-charge voltage.

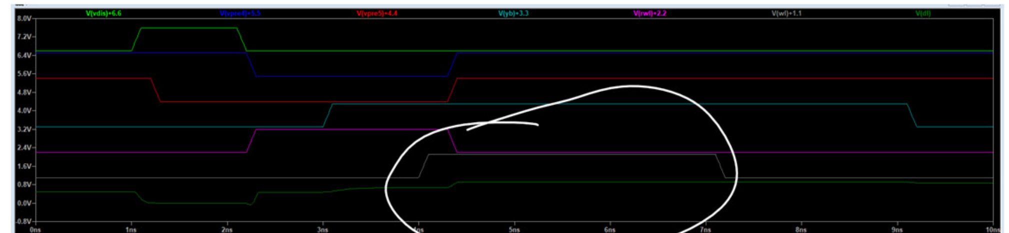
Preferred embodiments(11)

18. Before the decoding, Vdis is activated to the high level for discharging the DL voltage.

19. The DL voltage is initialized to lower than 0.5V.

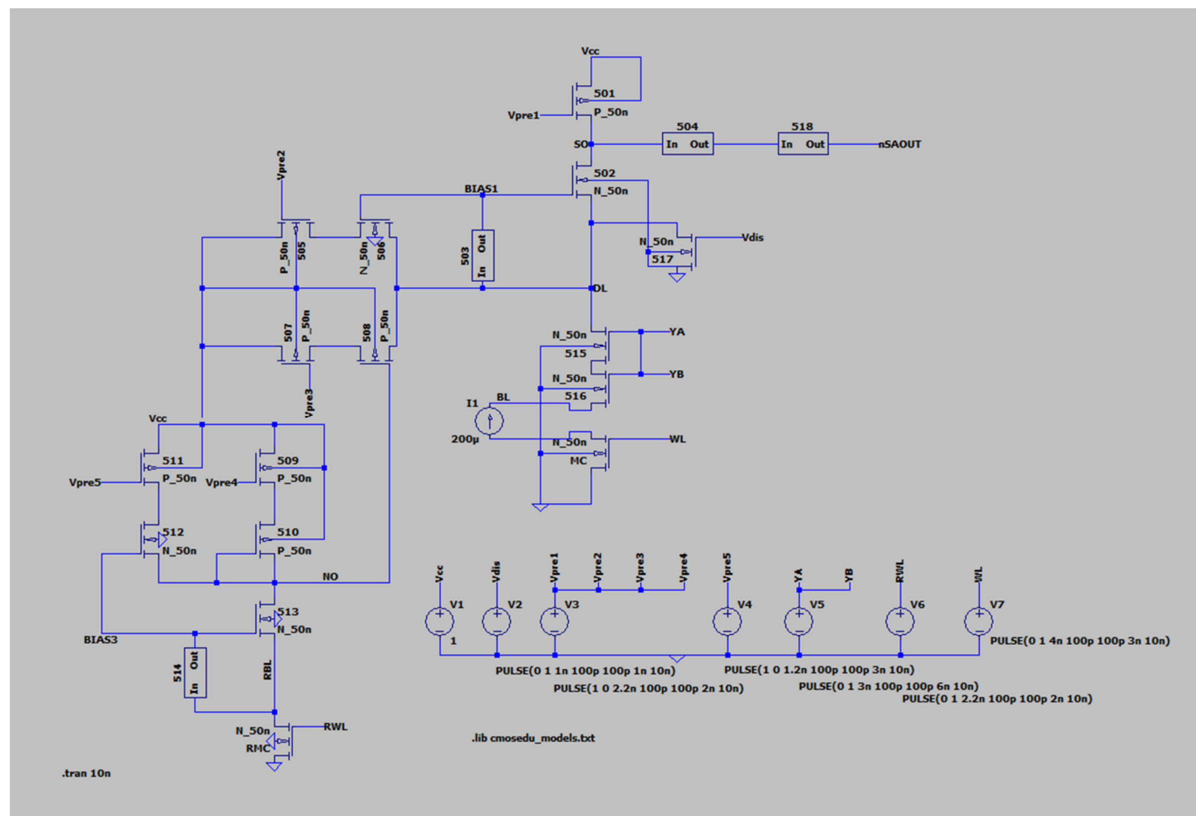
20. When an address is changed, row address decoding signals YA and YB are activated high.

21. The BL and DL are electrically connected.



The MC is in a non-conducting state,
And the voltage of DL is higher than
Pre-charge voltage.

Simulation of preferred embodiment



Future of flash memory technology

This patent studied was registered 20 years ago and was never renewed.

It is not an understatement to say that flash technology should have gotten farther than the period when this patten was filed.

Companies nowadays are shooting for an ultra-capacity and high speed flash memory chip that is cheap.

The patent’s sense amp design is bulky even though it is faster than the ‘prior art’.

Leading memory chip makers

- Micron
- Kioxia
- Samsung eUFC
- Western Digital
- SK hynix