

Practice Final Exam – ECG 721 Memory Circuit Design, Final Exam
University of Nevada, Las Vegas

NAME: _____

- Show your work to get credit.
 - Open book and closed notes.
 - Show your work on the attached sheets of paper **in order and on one side only in a neat manner.**
 - Do not do work on these test sheets.
 - Turn this test sheet in with your test. Failing to return this sheet will result in a 0 on the exam.
1. Explain how signal-to-noise ratio is determined by the memory-bit and bit-line capacitances in a DRAM. (5 points)
 2. Sketch the schematics for a bitline pair in a folded DRAM architecture with the n-sense amp, p-sense amp, equilibration circuitry, and I/O devices. Sketch, and label what's going on, the voltage signals used during a read operation. (10 points)
 3. What is the biggest concern with increasing the number of rows in a memory array? with increasing the number of columns? (5 points)
 4. Why do we need to ensure that the parasitic bitline capacitances connected to a sense amplifier are balanced? (10 points)
 5. Sketch the layouts of DRAM cells used in both folded and open arrays. Comment on the pros and cons of each layout. (5 points)
 6. From a circuit designer's point of view what is the difference between CHE and FNT? (10 points)
 7. Sketch a sense amplifier useful for regenerating logic levels outside of the array (on the side opposite the I/O devices) in a memory. Sometimes this sense amplifier is called a helper flip-flop. Using this topology discuss kickback noise, clock feedthrough, how the previous comparison's results (memory) is erased, and how power is minimized. (20 points)
 8. Sketch the schematic of a 6T SRAM memory cell. Describe why you need to precharge the bitlines high. (5 points)
 9. Sketch the IV curves for an erased and a programmed Flash memory cells and describe the state of charge on the floating gate in your own words. (5 points)
 10. Explain, in your own words, why a VCO is represented as an integration when analyzing PLLs. (5 points)
 11. Sketch the schematic of a delta-sigma sensing circuit useful for determining the value of a capacitor based upon the delta-sigma techniques from Ch. 17. Discuss the operation and derive equations governing the circuit's operation. (20 points).