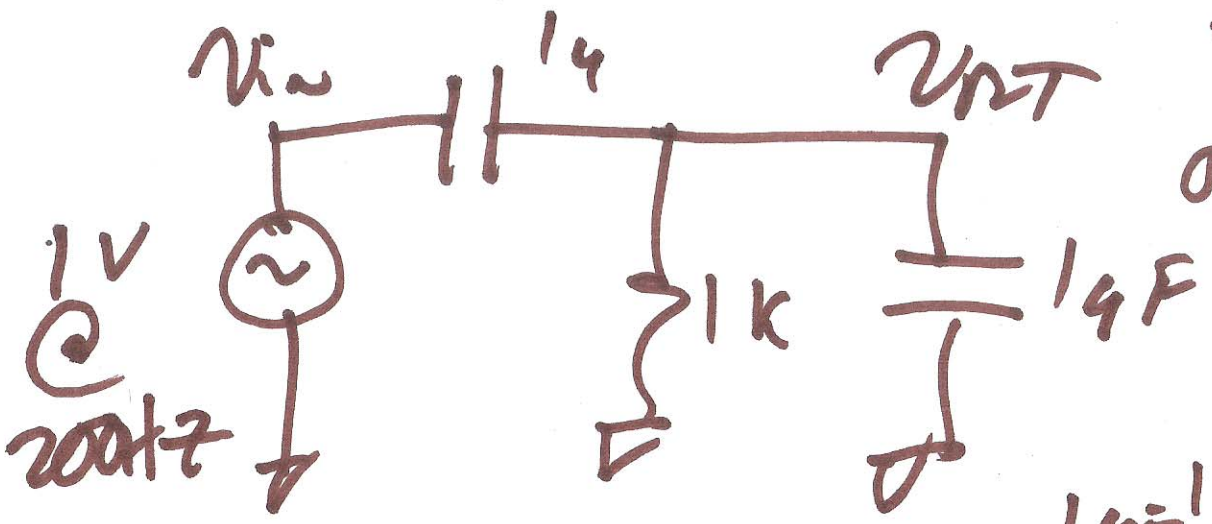
Review for final } Closed Book } final Monday Dec. 8 1-3 here sabbath

1) Ch. 1 → circuits problem

RC → AC response time domain

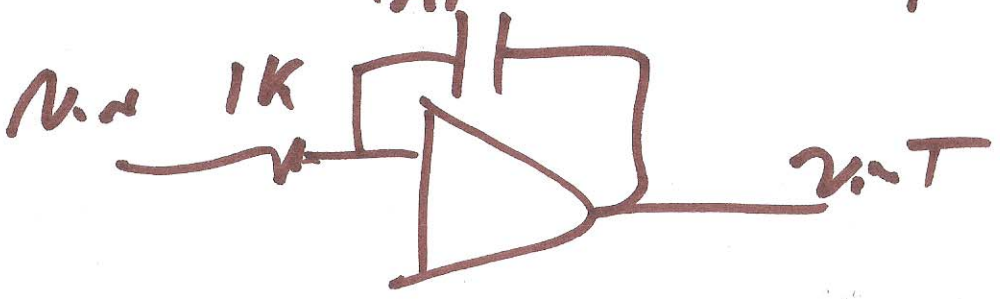
op-Amp → gain & freq resp



Inductor problem

$\left|\frac{V_{OUT}}{V_{in}}\right|$

$L\frac{V_{OUT}}{V_{in}}$



Ch. 2

N-well

$t_d = 0.7 r c \frac{\ell(\ell+1)}{2}$

layouts → x-sect views

depletion C

diffusion C

reverse recovery time

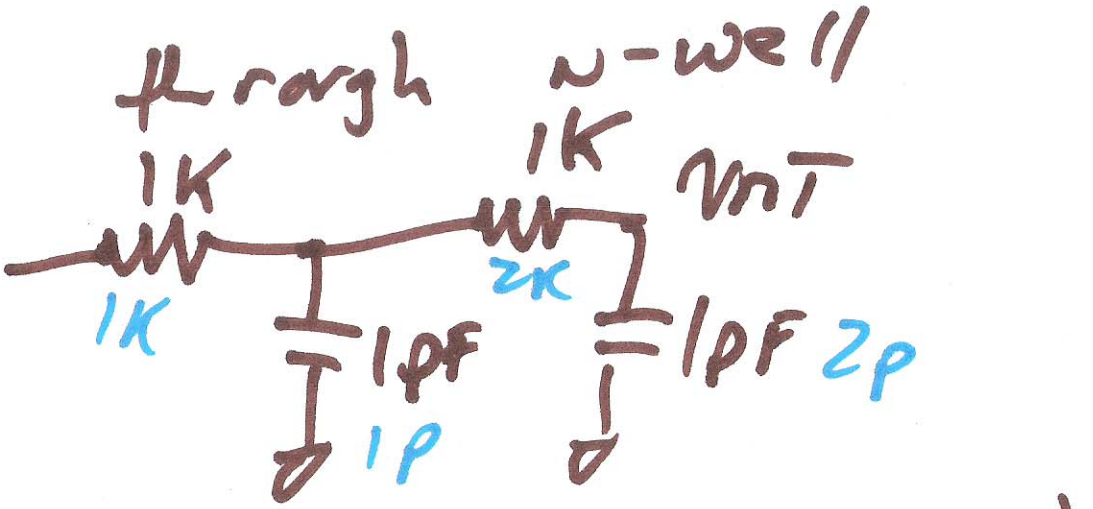
Resistance - sheet R

delay through n-well

Quiz

Test

Stage time

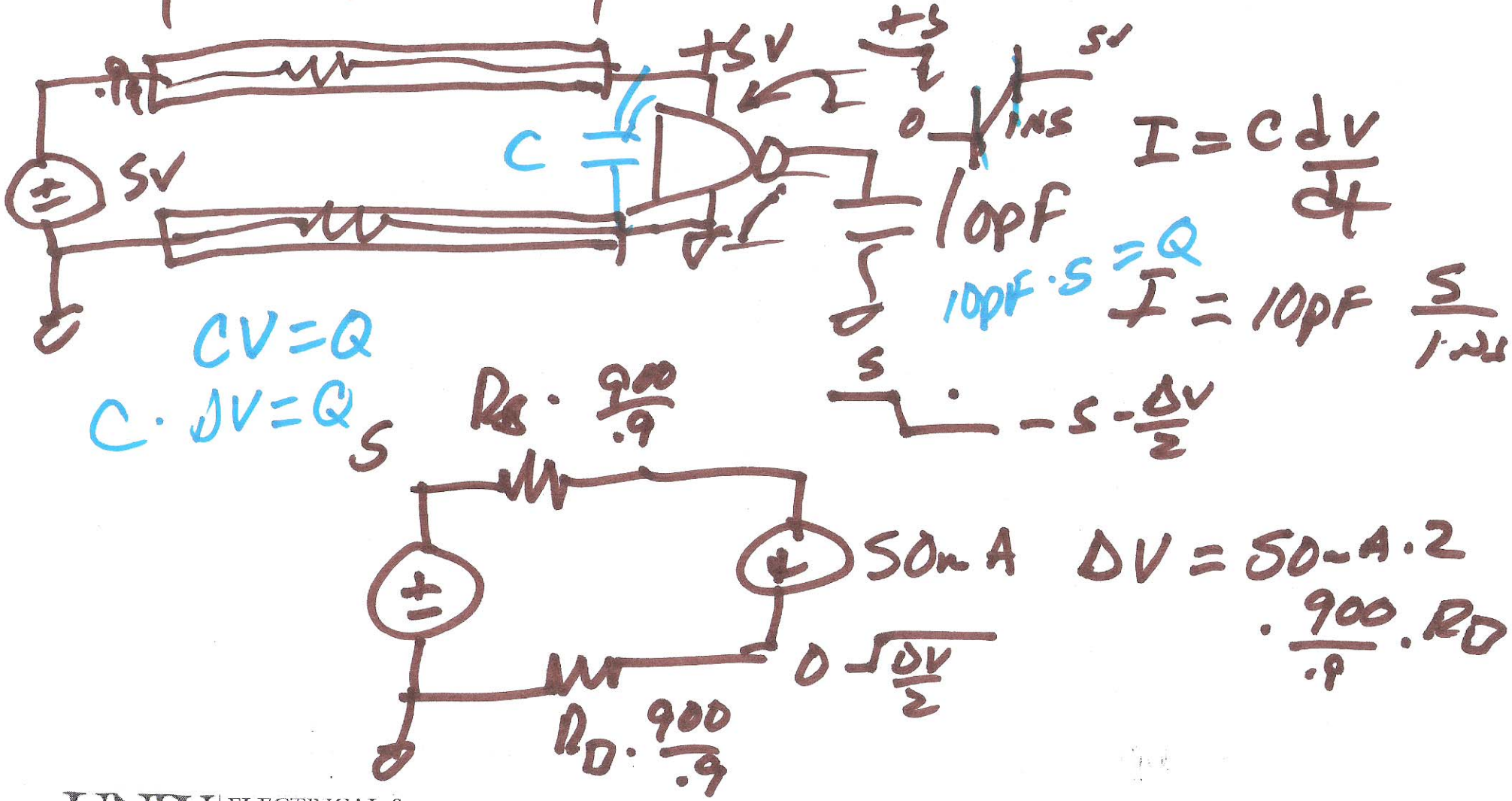


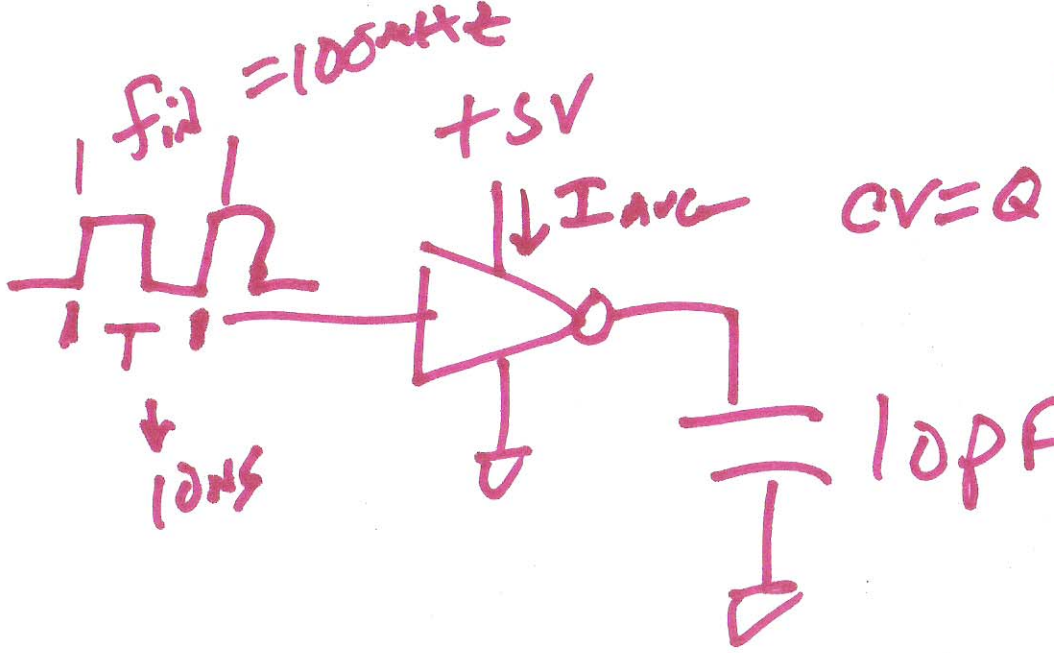
$$t_d = 0.7(1K \cdot 1pF + 2K1pF)$$

Ch. 3 → Metal Layers

Electromigration

Size metal layers





a) Calculate power disp. by: load C inverter & pmos/nmos

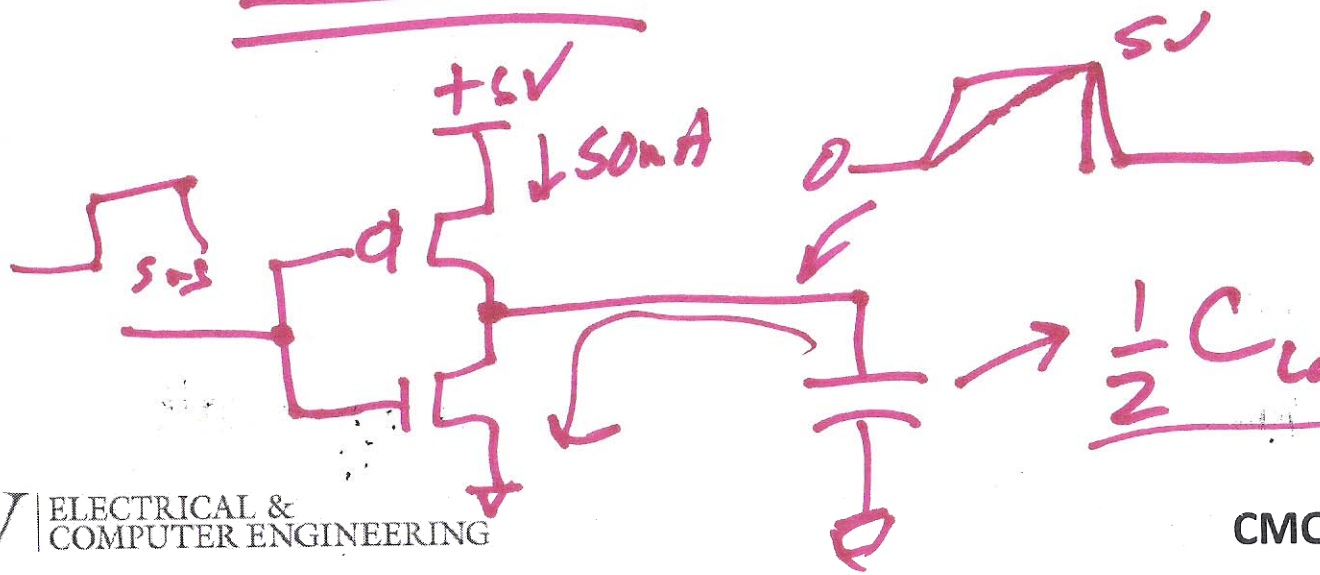
$CV = Q$

$Q = 50pC$

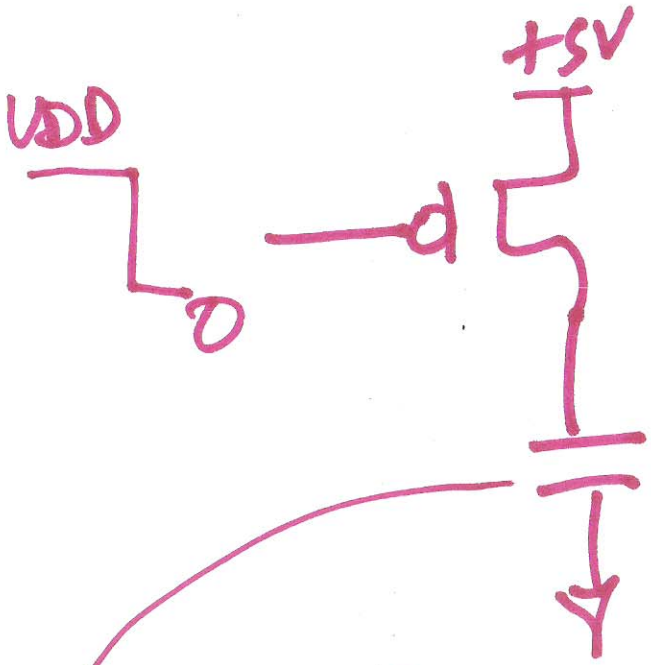
$P_{diss} = 5 \cdot I_{AVG} = VDD \cdot VDD \cdot \frac{Q}{10ns}$

$I_{AVG} = \frac{50pC}{10ns} = 5mA$

$= \underline{\underline{250\,mW}}$



$\frac{\frac{1}{2} C_{load} VDD \cdot VDD}{5ns}$



Estimate the power diss. by the pmos while it's charging the load.

$$Q = 5 \cdot 10pF = 50pC$$

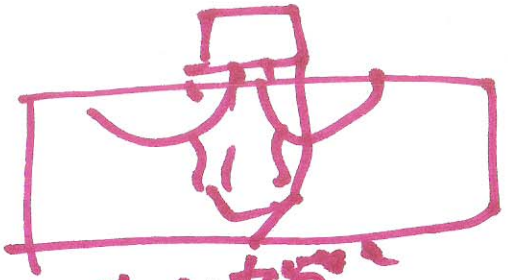
$$\frac{1}{2}CV^2 = \frac{1}{2} \cdot 10p \cdot 5^2$$

Ch 4 & 5

Layout of wide MOSFETs

oxide encroachment

lateral diffusion



Ch. 6 MOSFETs

Sketch I V

I_D v. V_{DS} with vary V_{GS}

$V_{GS} = 0$ $V_{DS} = V_{DD}$

I_D v V_{DS} with vary V_{GS}

I_{off}

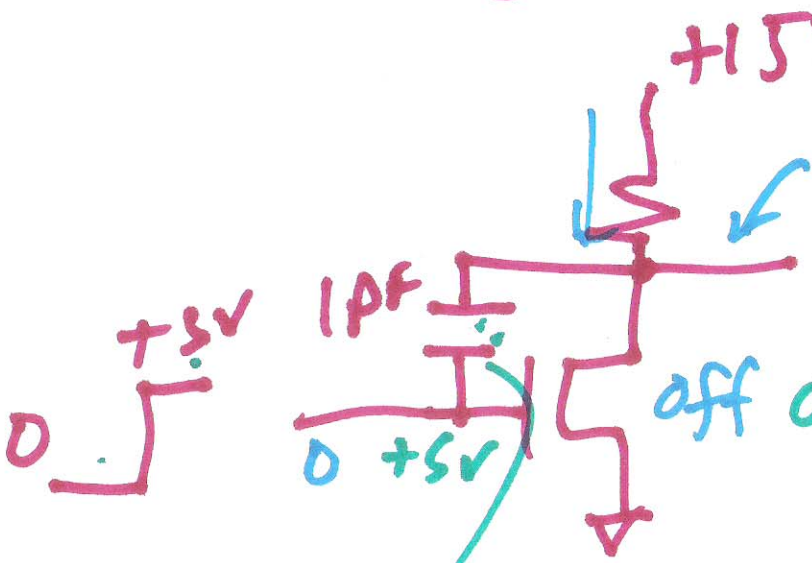
$V_{DS} = V_{DD}$ ← I_{on}

$V_{DS} = V_{DD}$ $I_{D,SAT}$

Threshold

Ch. 10

Derive Digital



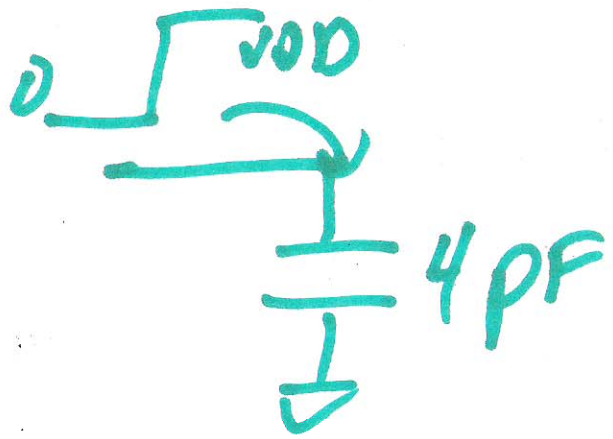
(0-15)1pF -

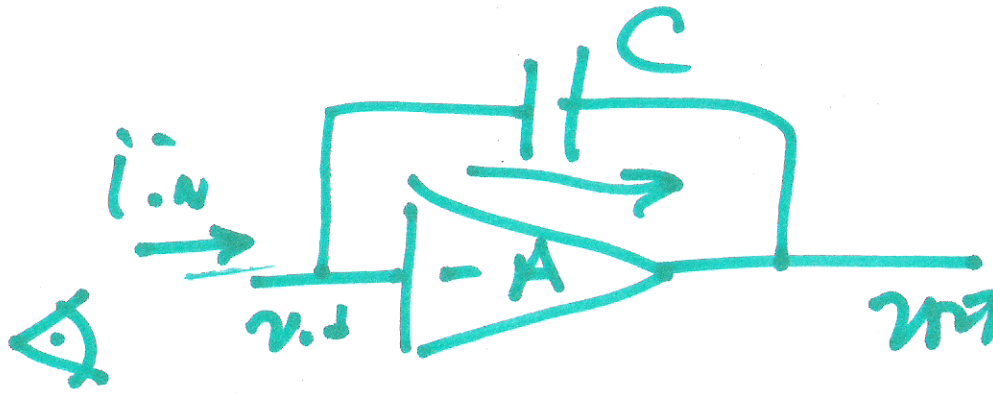
(5-0)1p ⇒ -201pF

= -100.4pF

-3

What is C_{ON} & C_{OFF}?





$$i_{IN} = \frac{v_{IN} - (-A \cdot v_{in})}{1/j\omega C} = v_{IN}(1+A)j\omega C$$

$$\frac{v_{in}}{i_{in}} = j\omega \underbrace{C \cdot (1+A)}_{C_{IN}}, \quad C_{IN} = C\left(1+\frac{1}{A}\right)$$

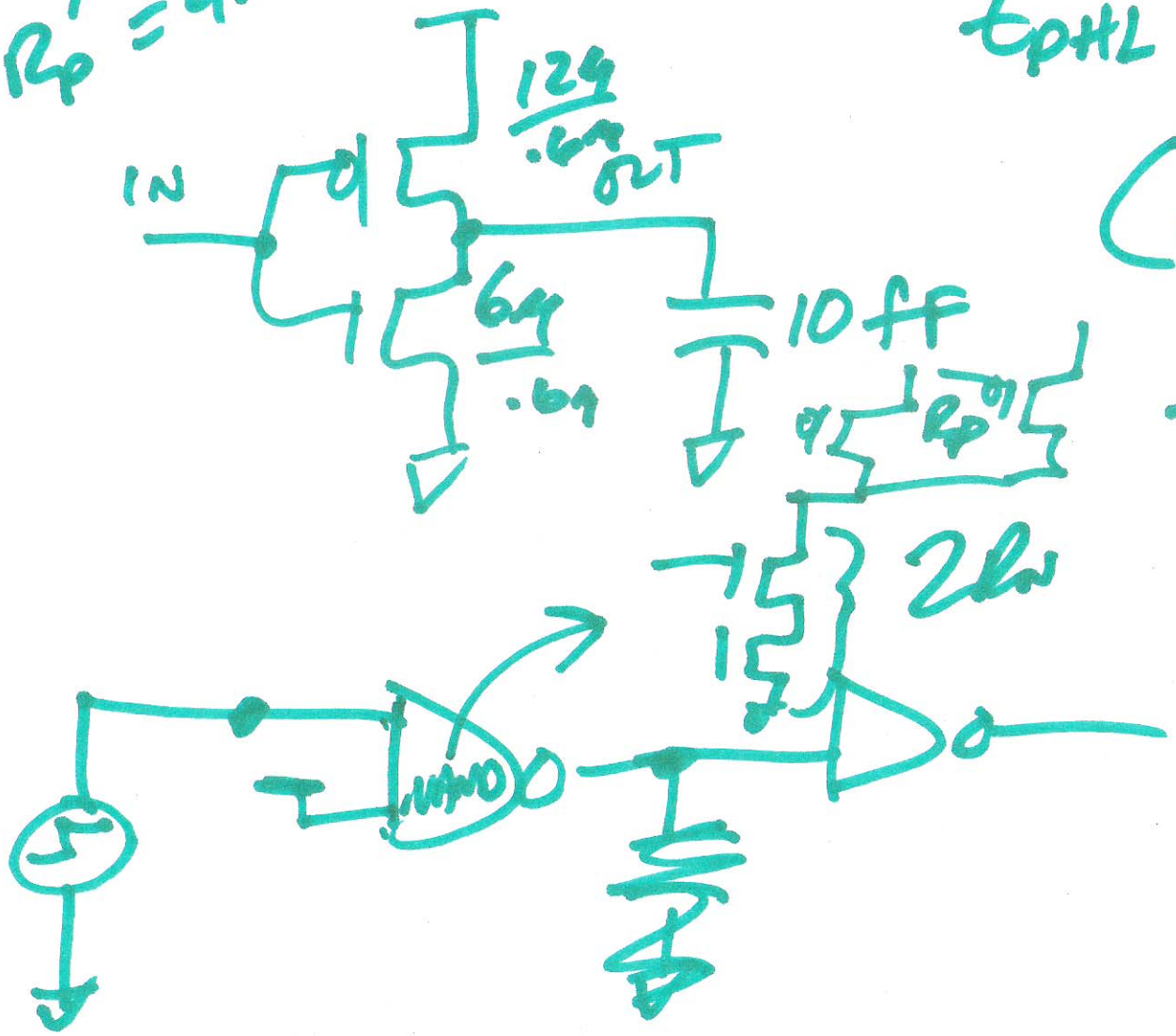
Calculate delays

$R_N' = 20k$

$R_P' = 40k$

$t_{pHL} = 0.7 \cdot 20k \cdot \frac{6}{6}$

$\left(10ff + C_{ox}' \cdot 6_4 : 6_4 + C_{ox}' \cdot \frac{12}{12} \cdot 6_4\right)$



DFF

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Sketch schematic

positive edge triggered

negative edge triggered

Be able to describe operation.

setup & hold times