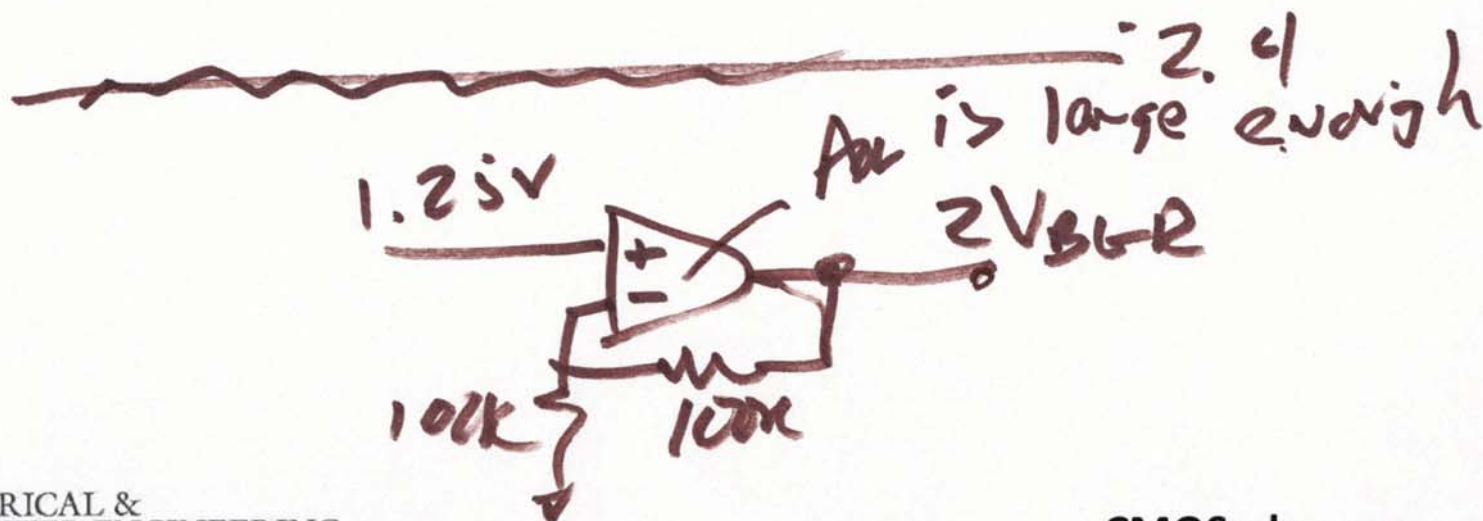


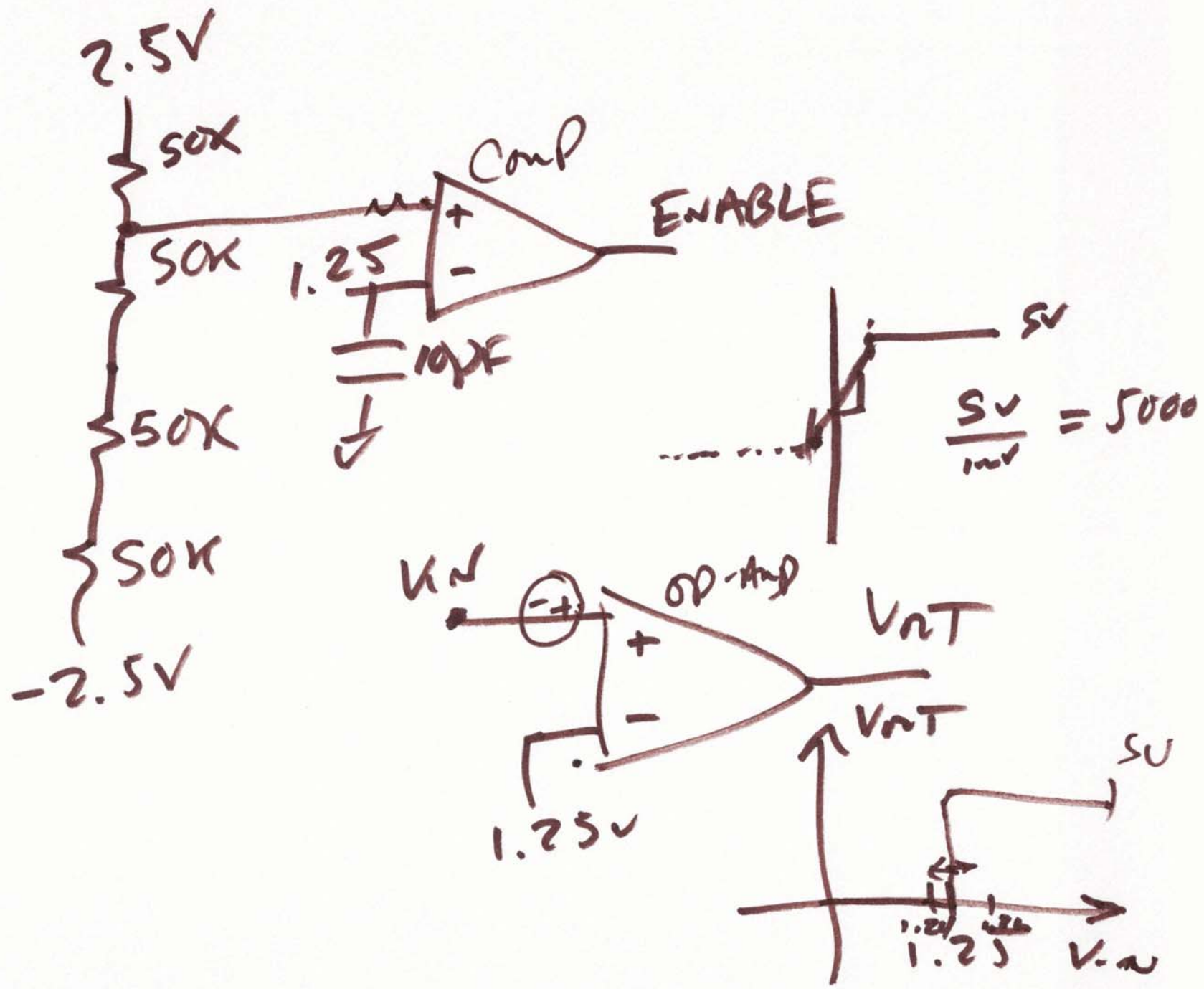
EE 421 / ECE 621

Digital IC Design

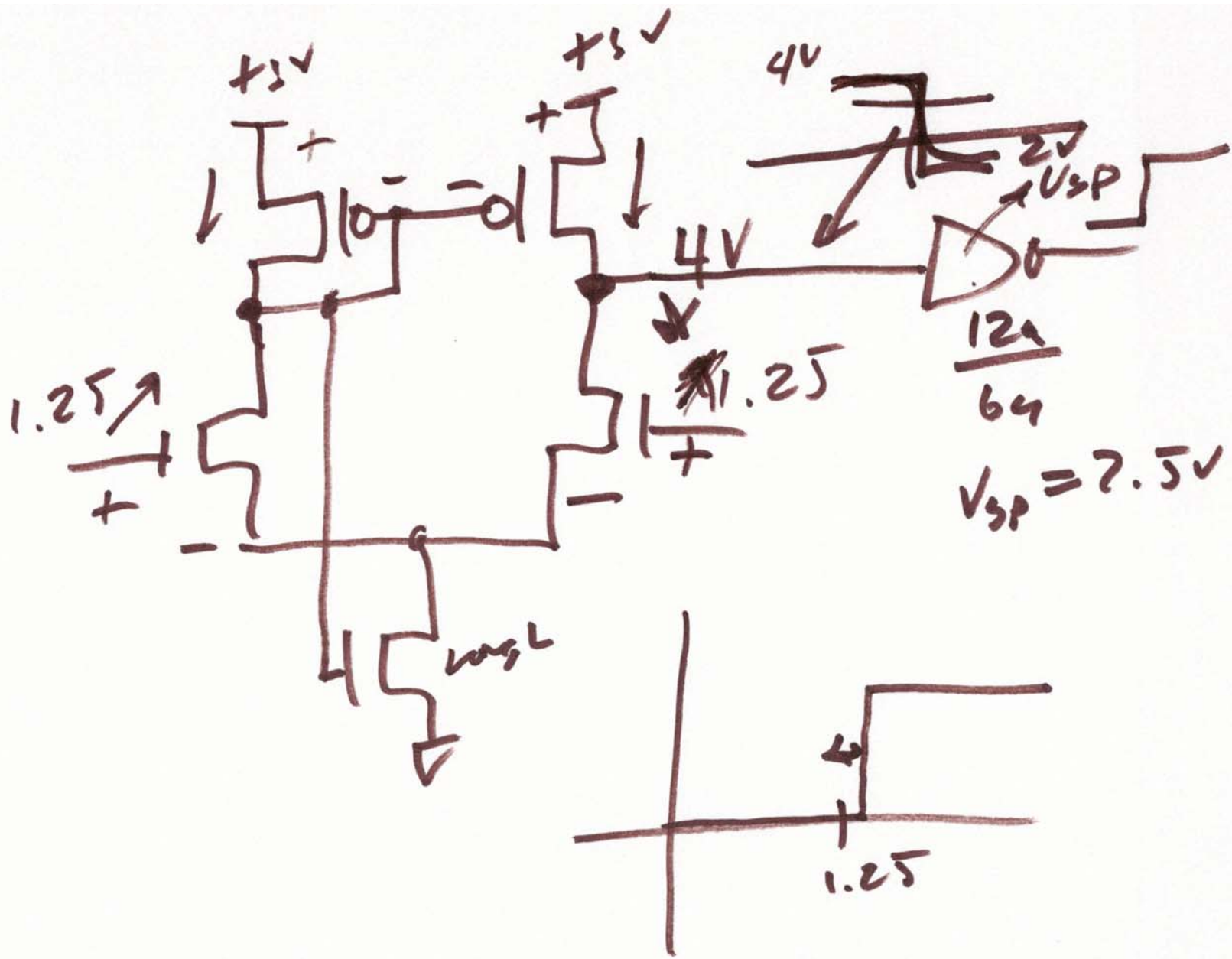
11/23/2015

Lecture 24

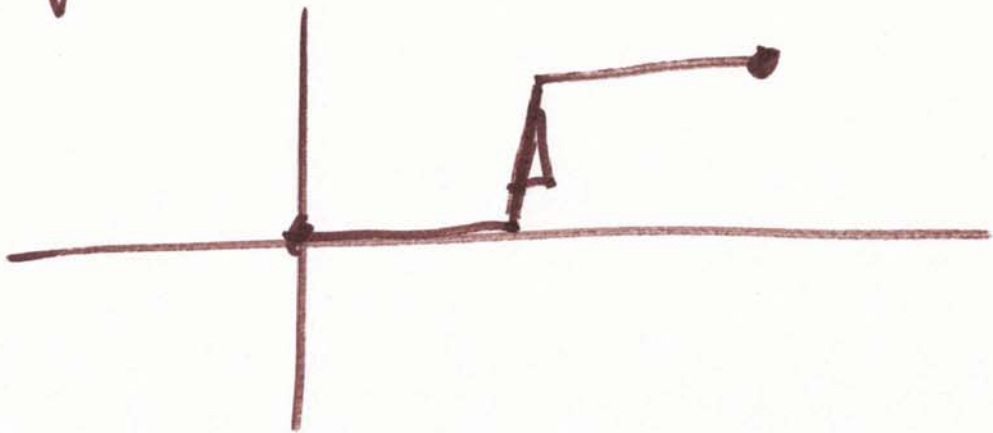
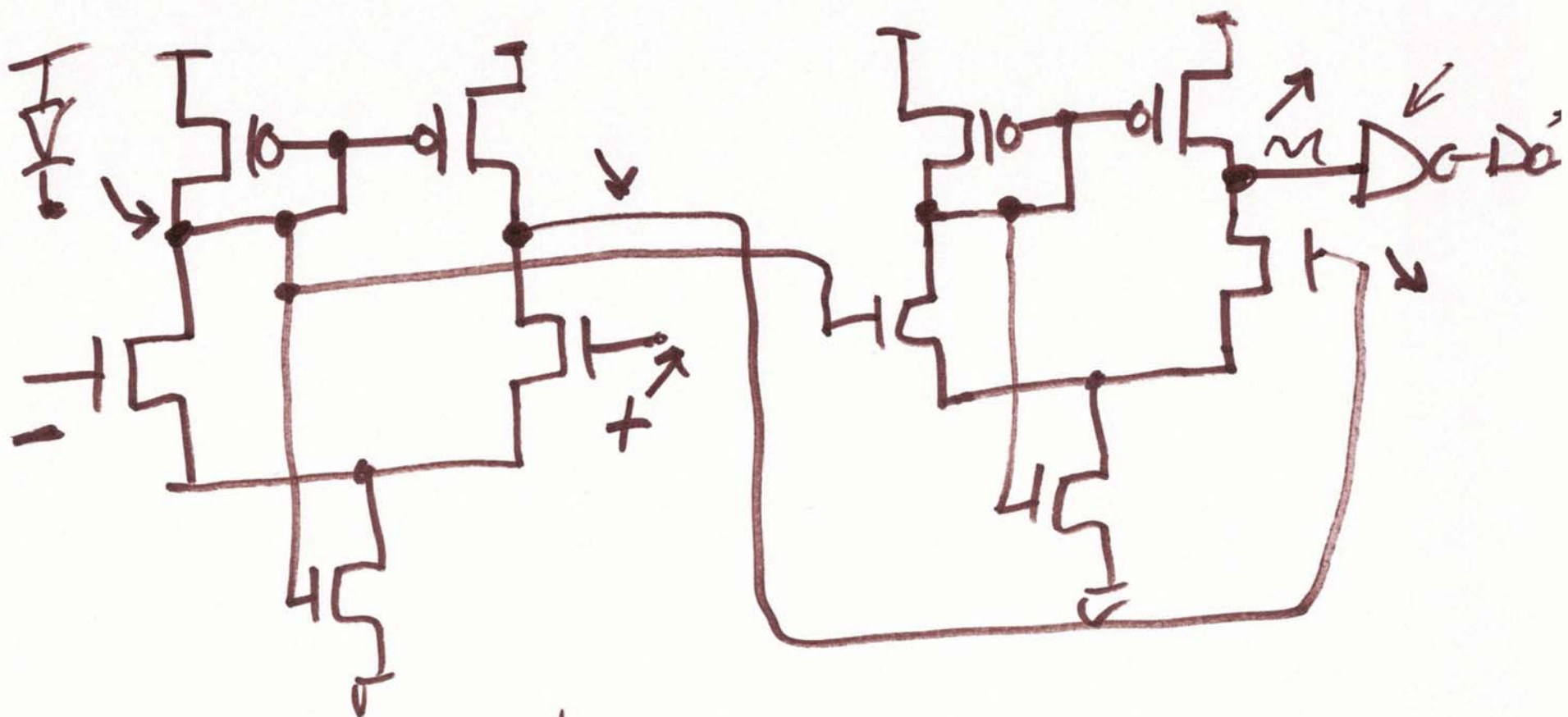




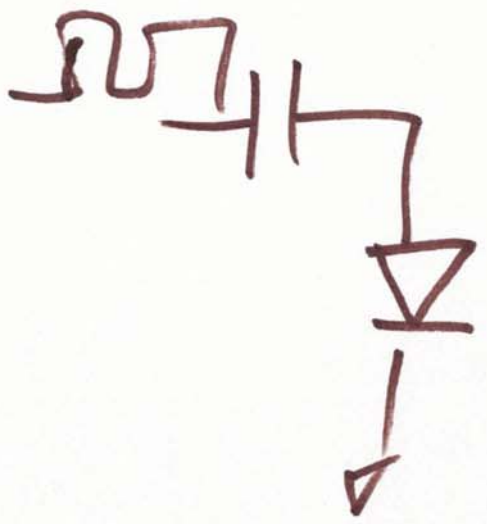
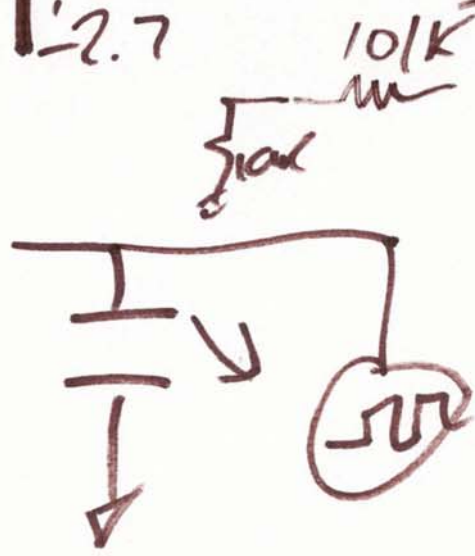
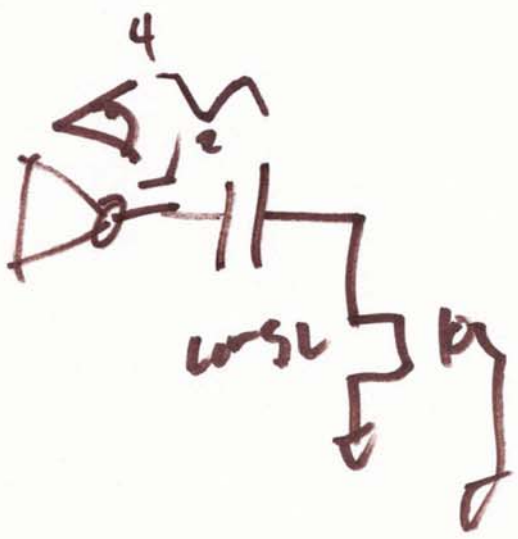
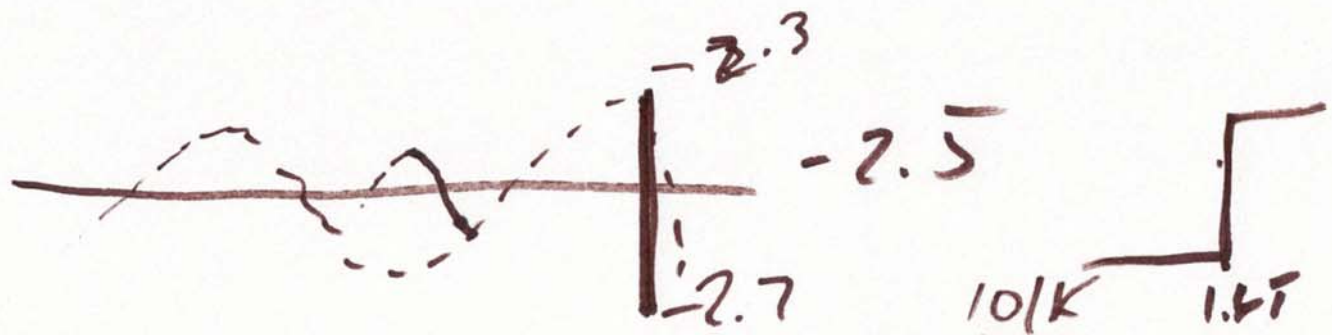
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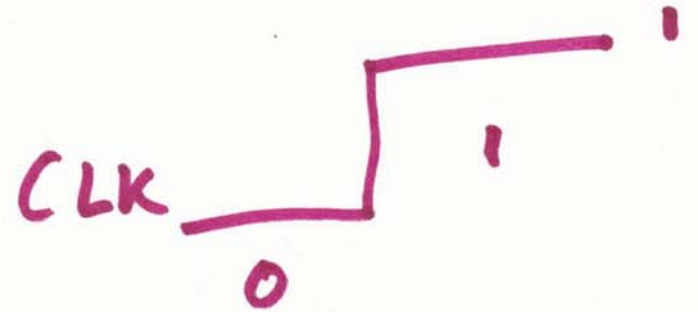
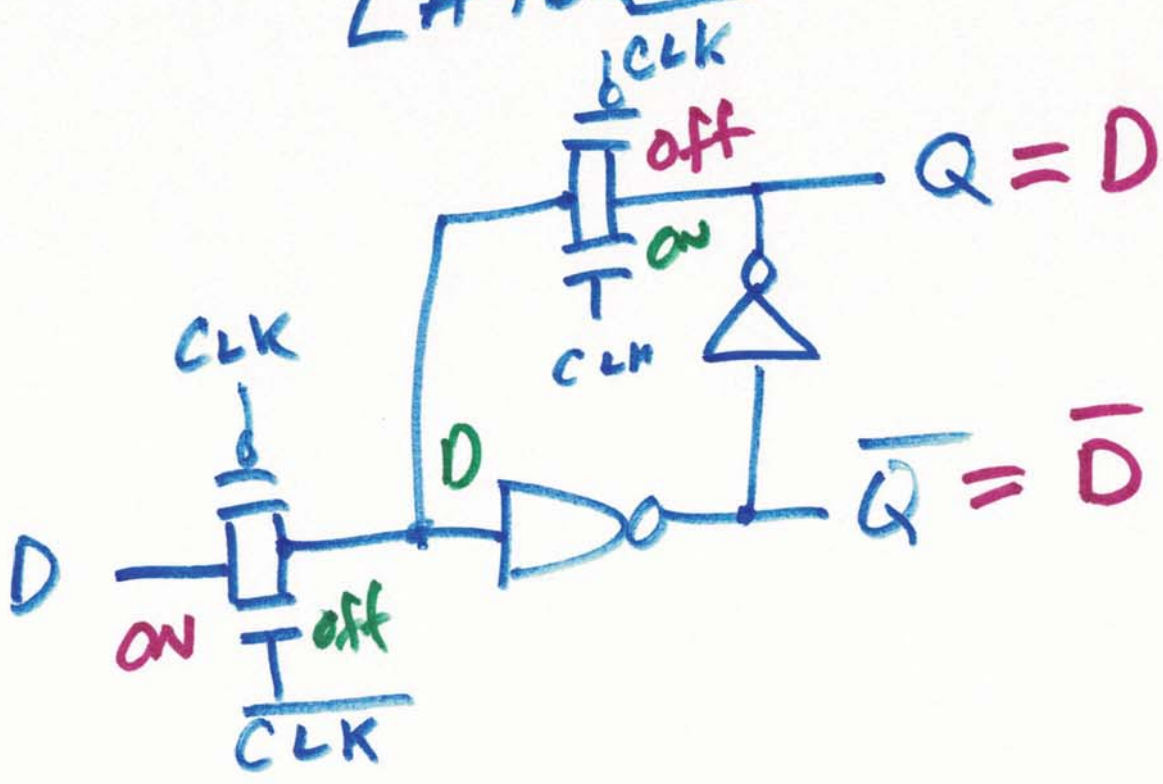
3)



4)

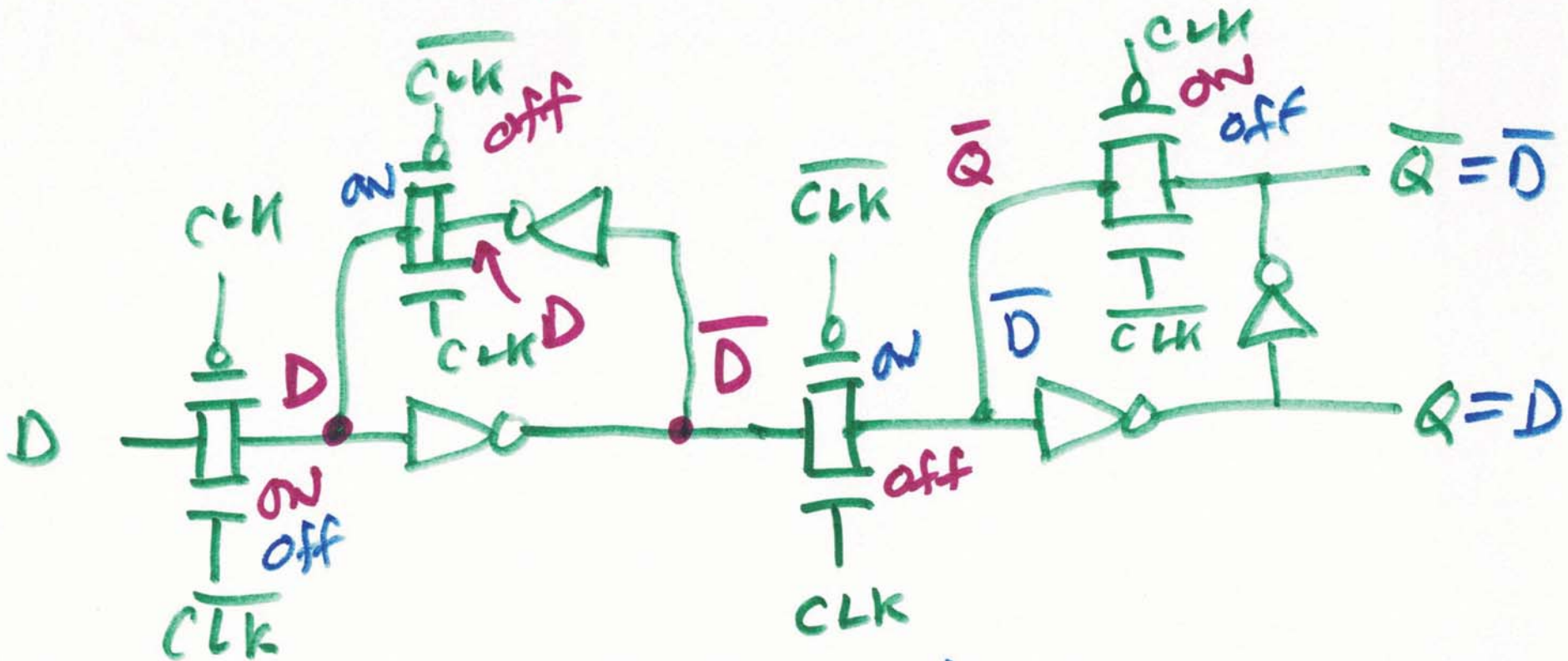


Latch

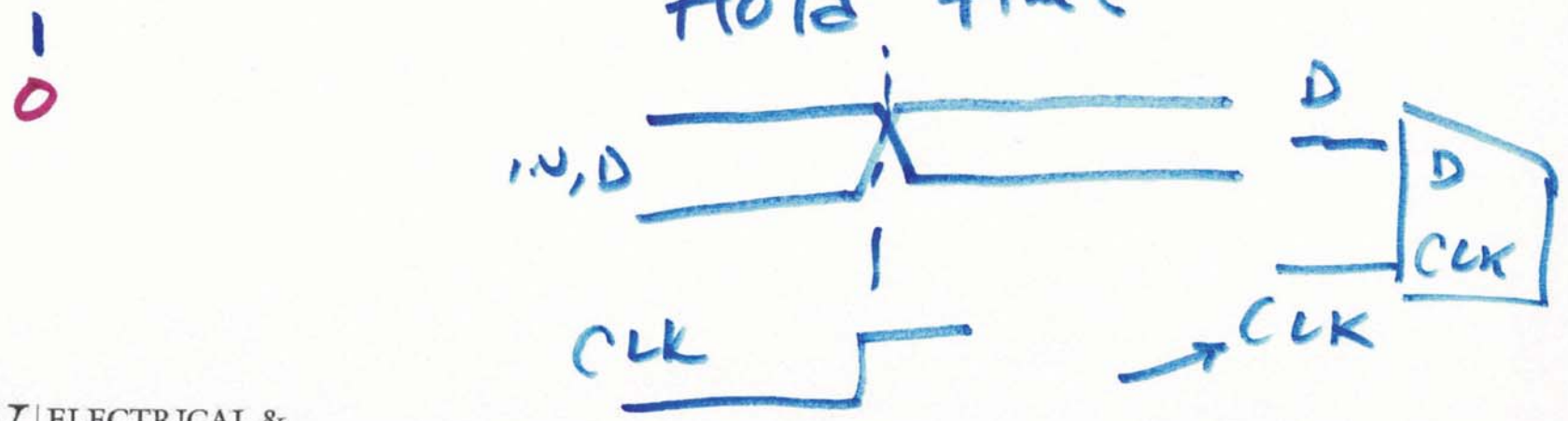


6)

Edge triggered D-FF

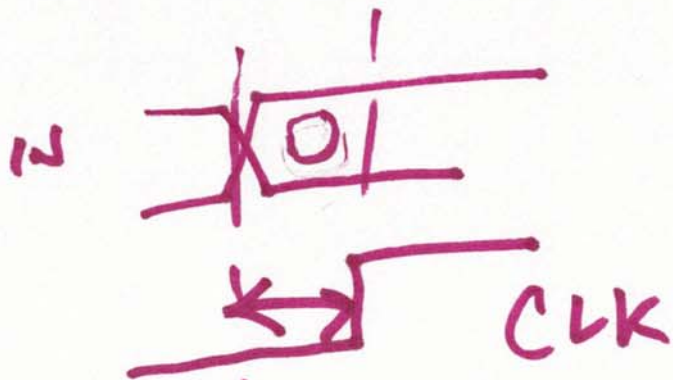


Hold time

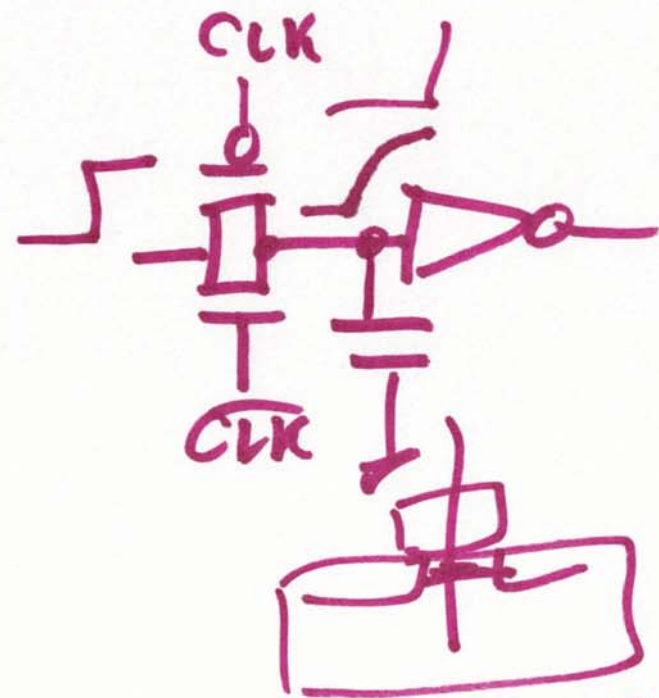
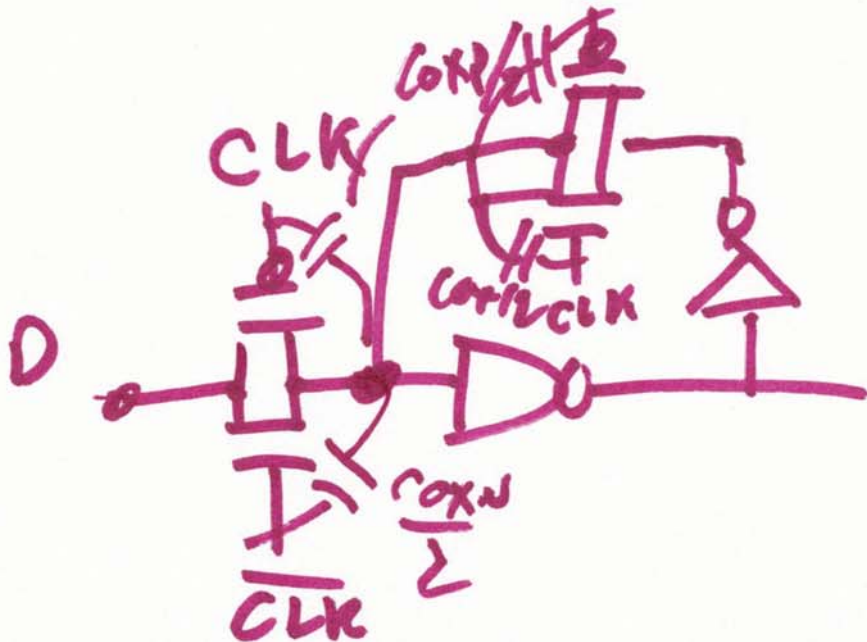


7)

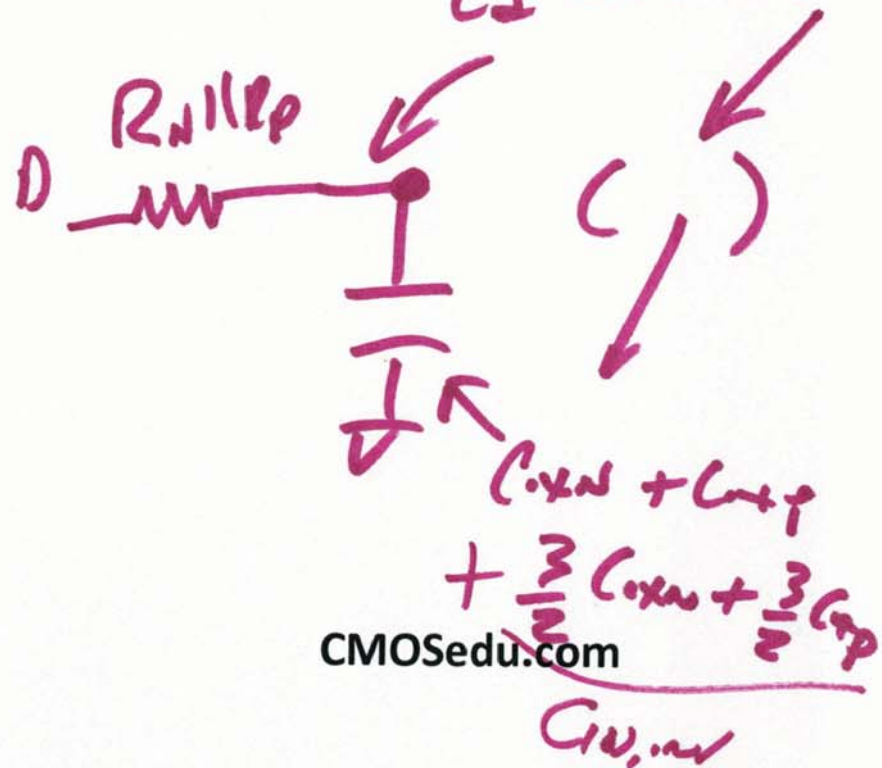
setup time

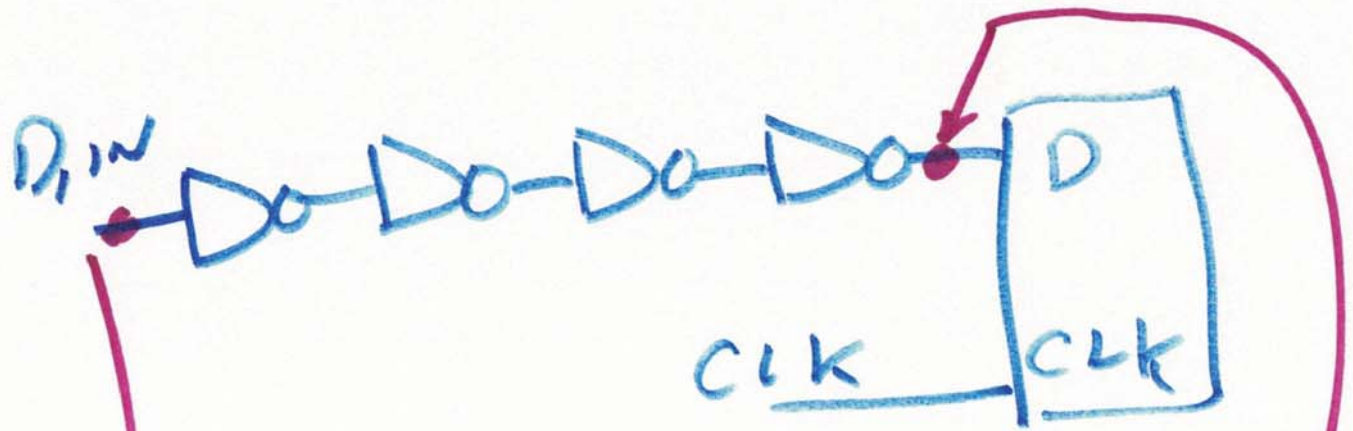


$$t_s \approx \frac{C_{in} V_{DD}}{I_{CLK}}$$

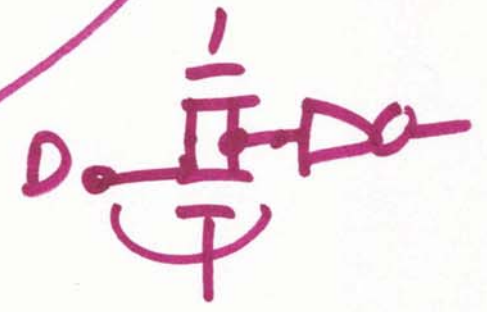
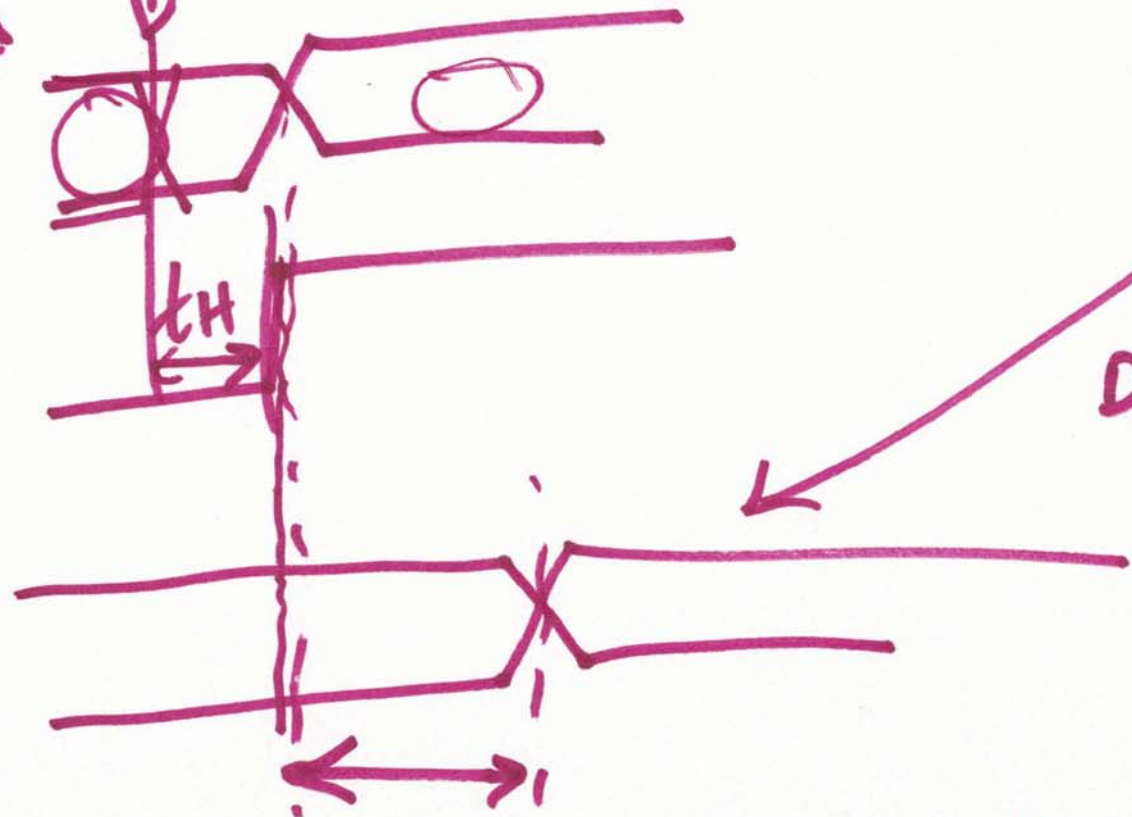


$$t_d \approx 0.7 R_{in} I_{CLK}$$



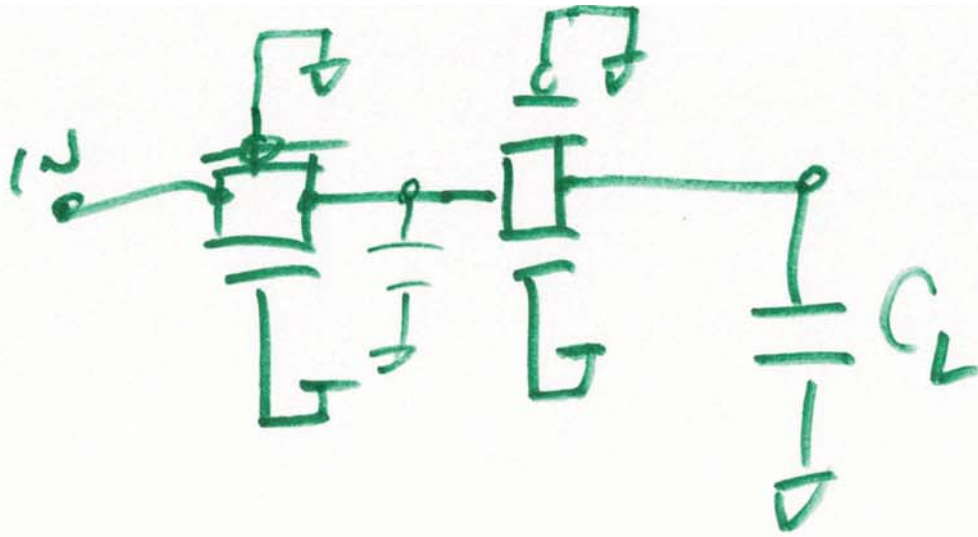


Negative hold time



4 inverter delays

8)



$$t_d = 0.7 \cdot 2 \cdot R_{n1} \parallel R_{p1} \cdot C_L +$$

$$\frac{2(l+1)}{2}$$

$$0.7 R_{n1} \parallel R_{p1} \cdot (C_{oxn} + C_{oxp}) +$$

$$0.7 \cdot R_{n1} \parallel R_{p1} \cdot$$

$$0.7 \cdot 2 R_{n1} \parallel R_{p1} (C_{oxn} + C_{oxp}) +$$

$$C_{oxn} + C_{oxp}$$

$$0.7 \cdot 3 \cdot R_{n1} \parallel R_{p1} (C_{oxn} + C_{oxp})$$

9)