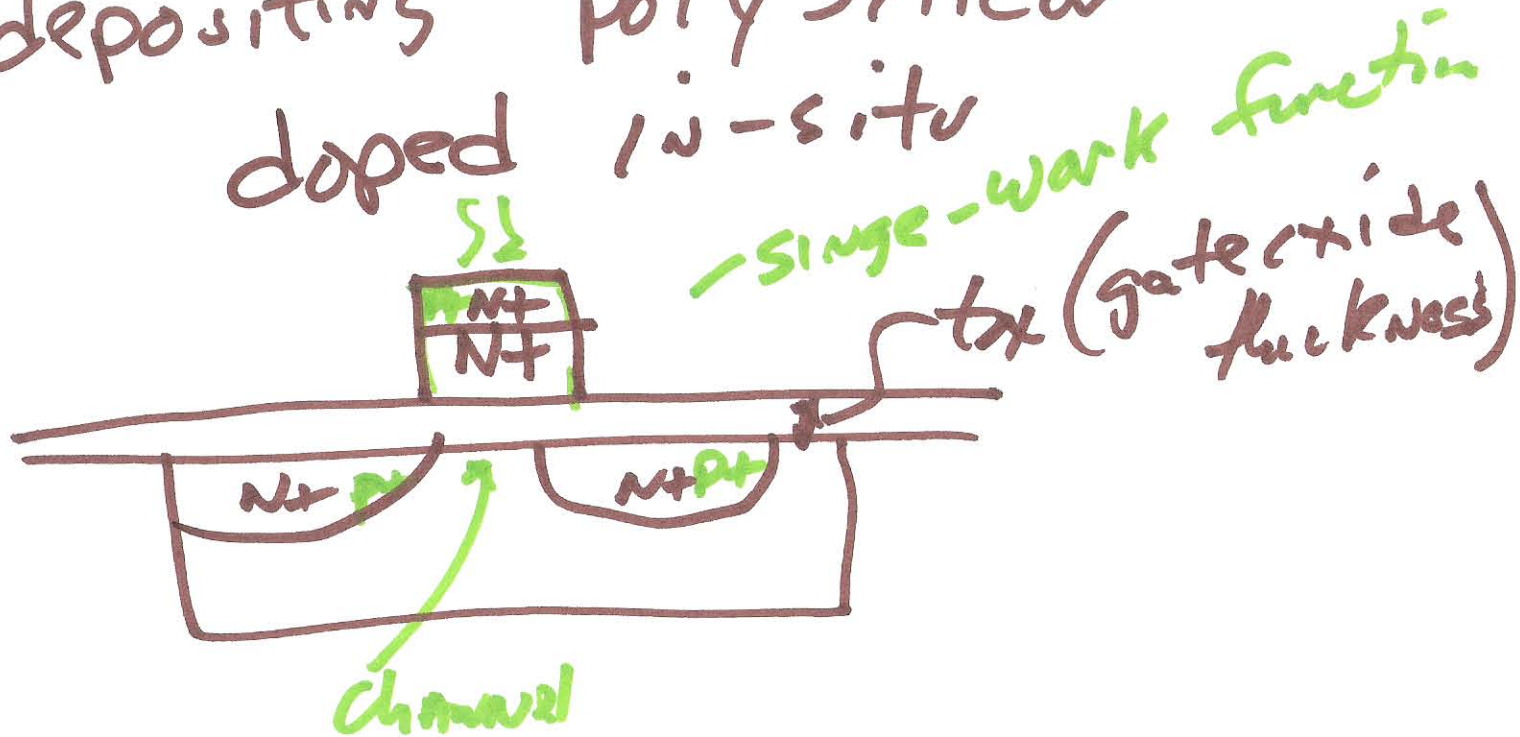
EE 421 / ECG 621

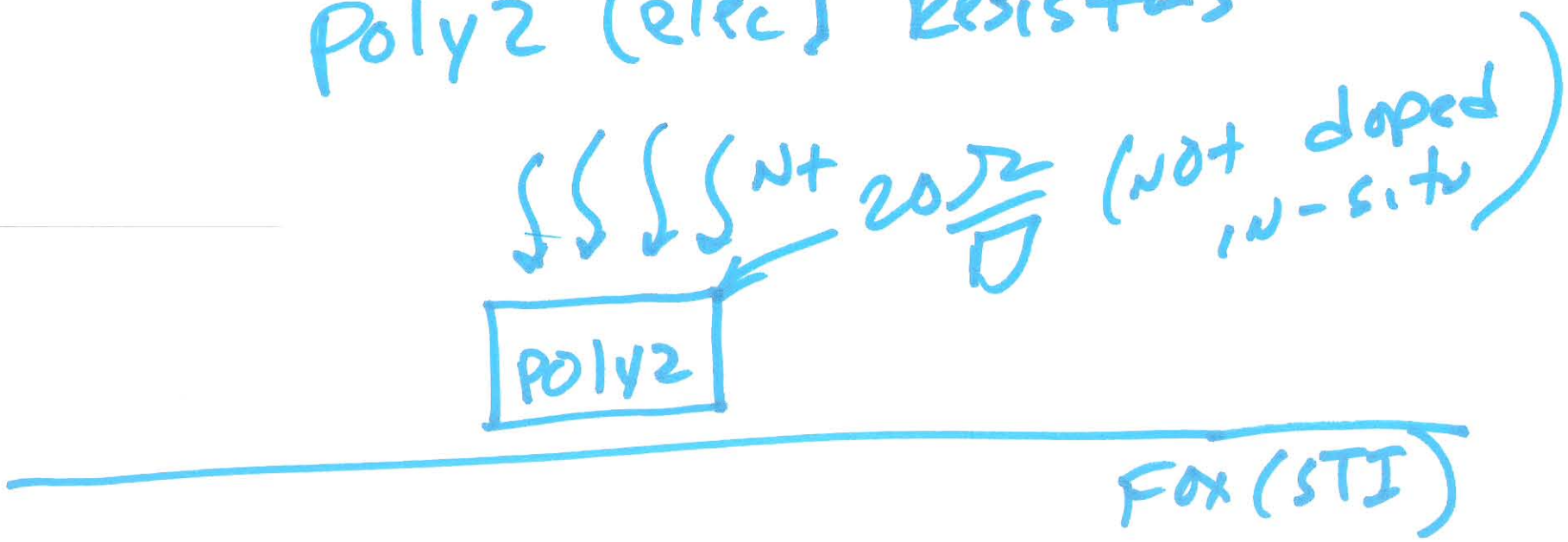
Digital IC Design

Lecture 9, 9/23/2015

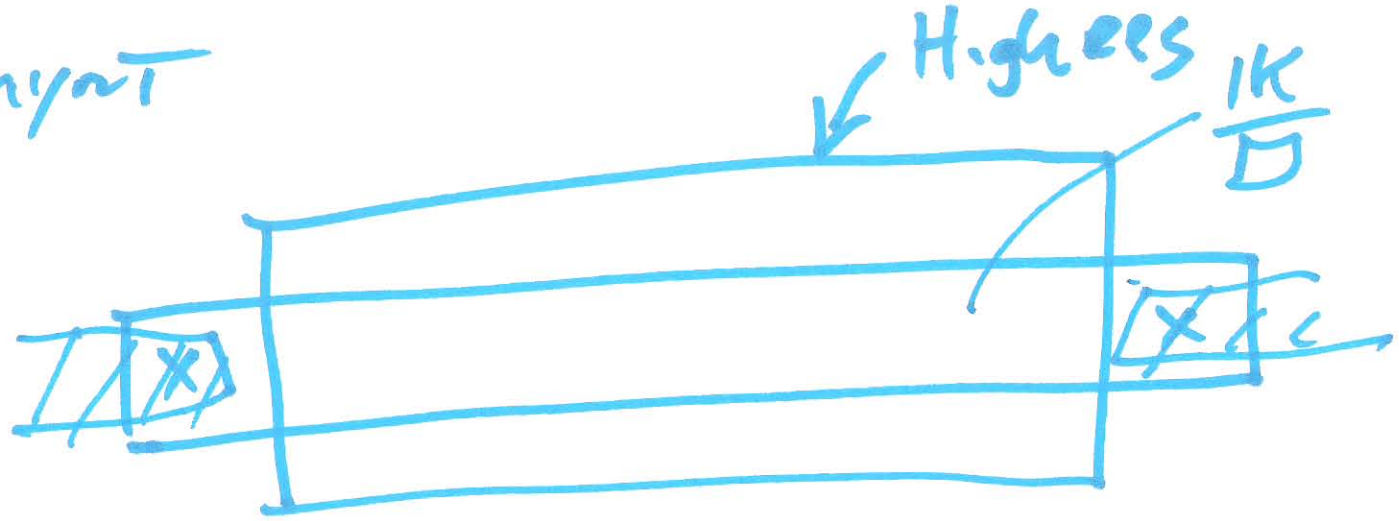
depositing polysilicon doped in-situ

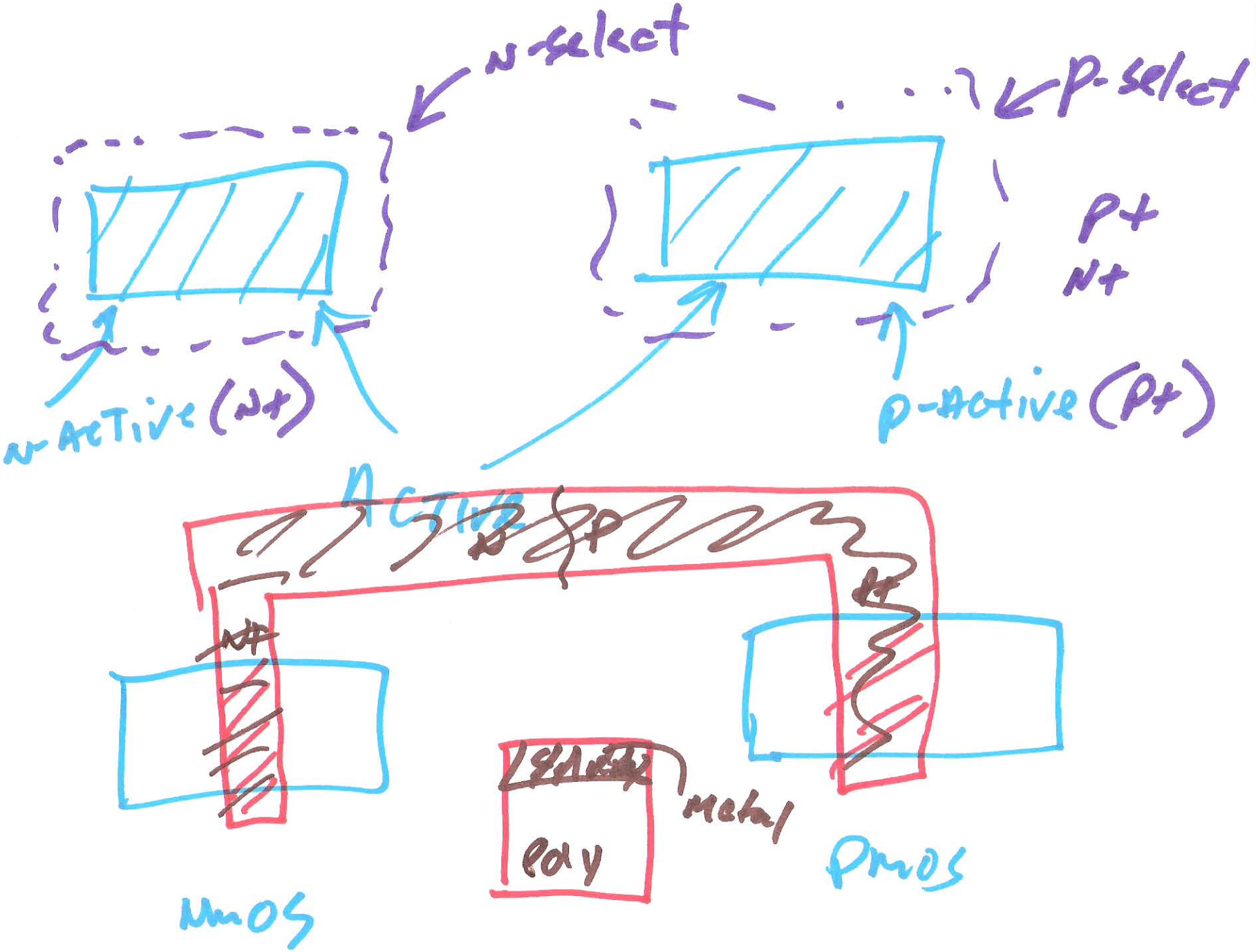


Poly2 (elec) Resistors

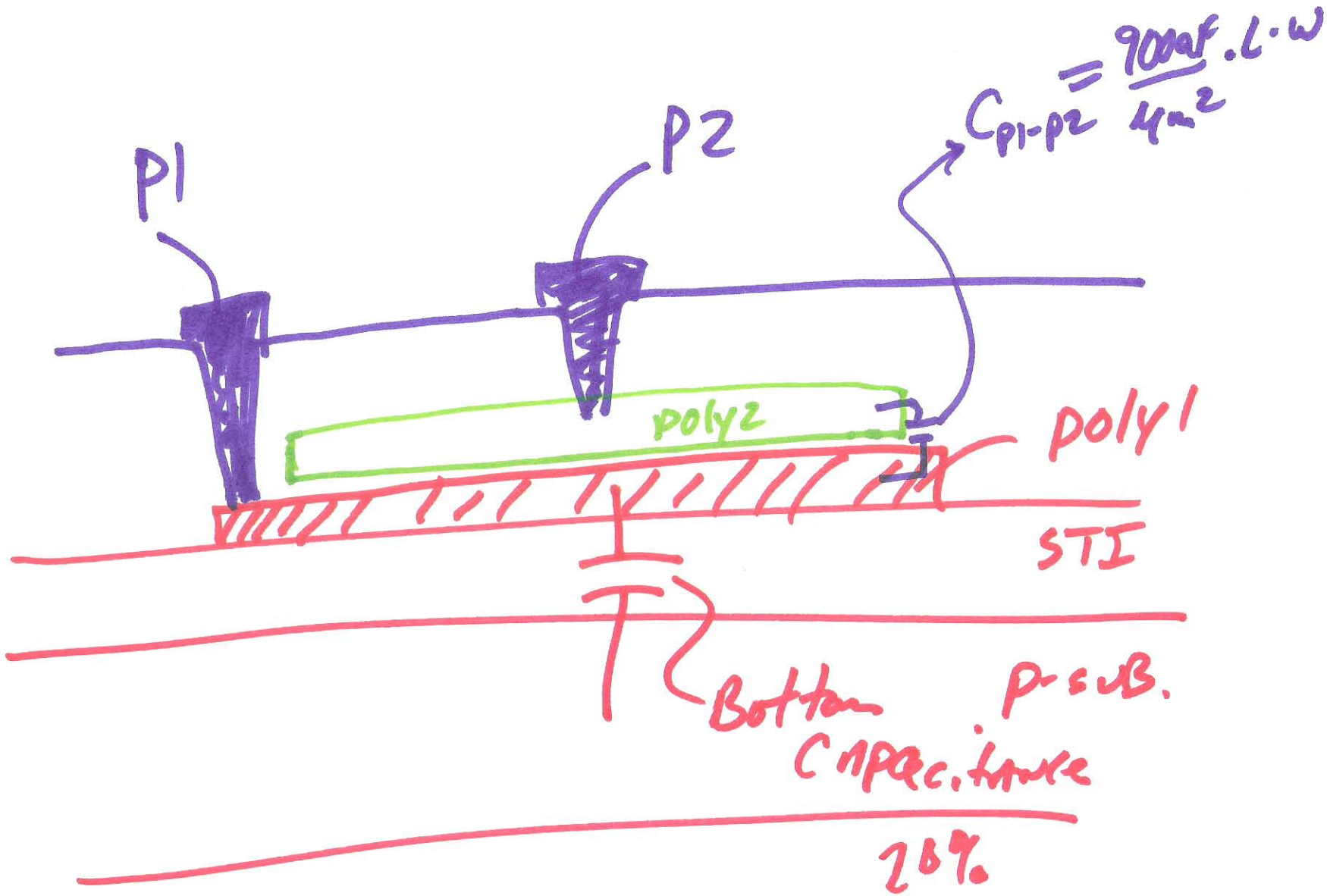


Layout

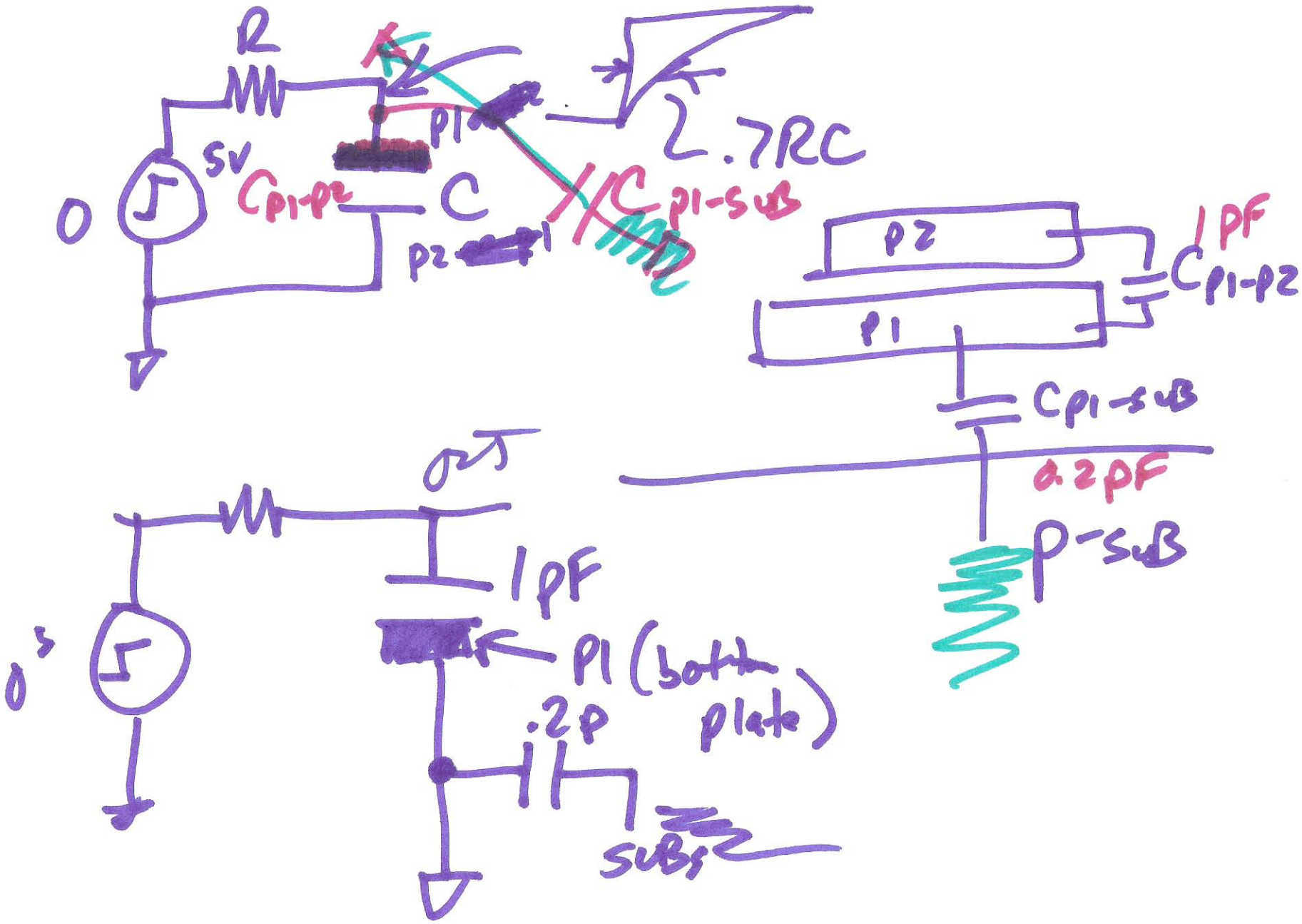



N-select
P-select
P+
N+
N-Active (N+)
P-Active (P+)
Active
Metal
Poly
NMOS
PMOS

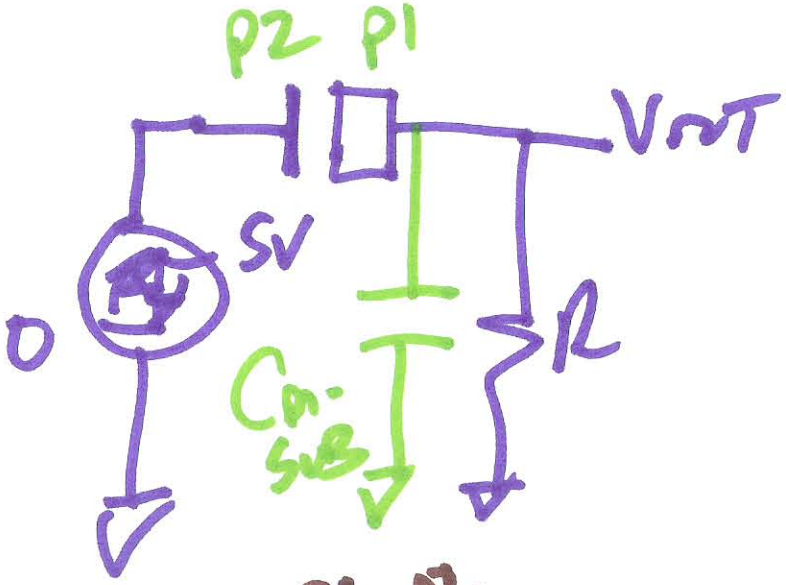
3)

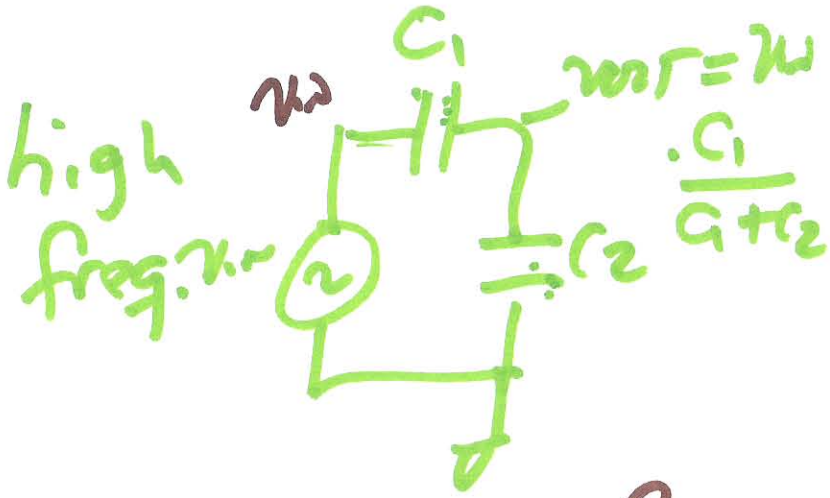

P1
P2
$C_{P1-P2} = \frac{900aF}{4m^2} \cdot L \cdot W$
poly2
poly1
STI
Bottom
P-sub.
Capacitance
20%

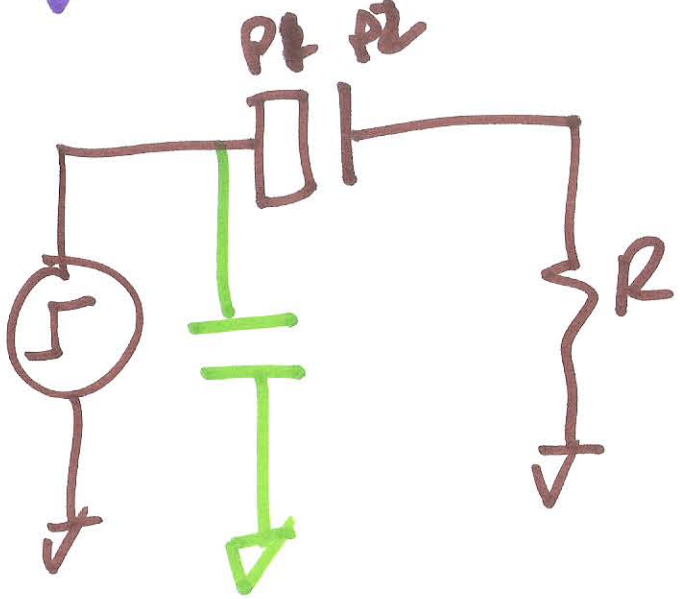
4)



5)

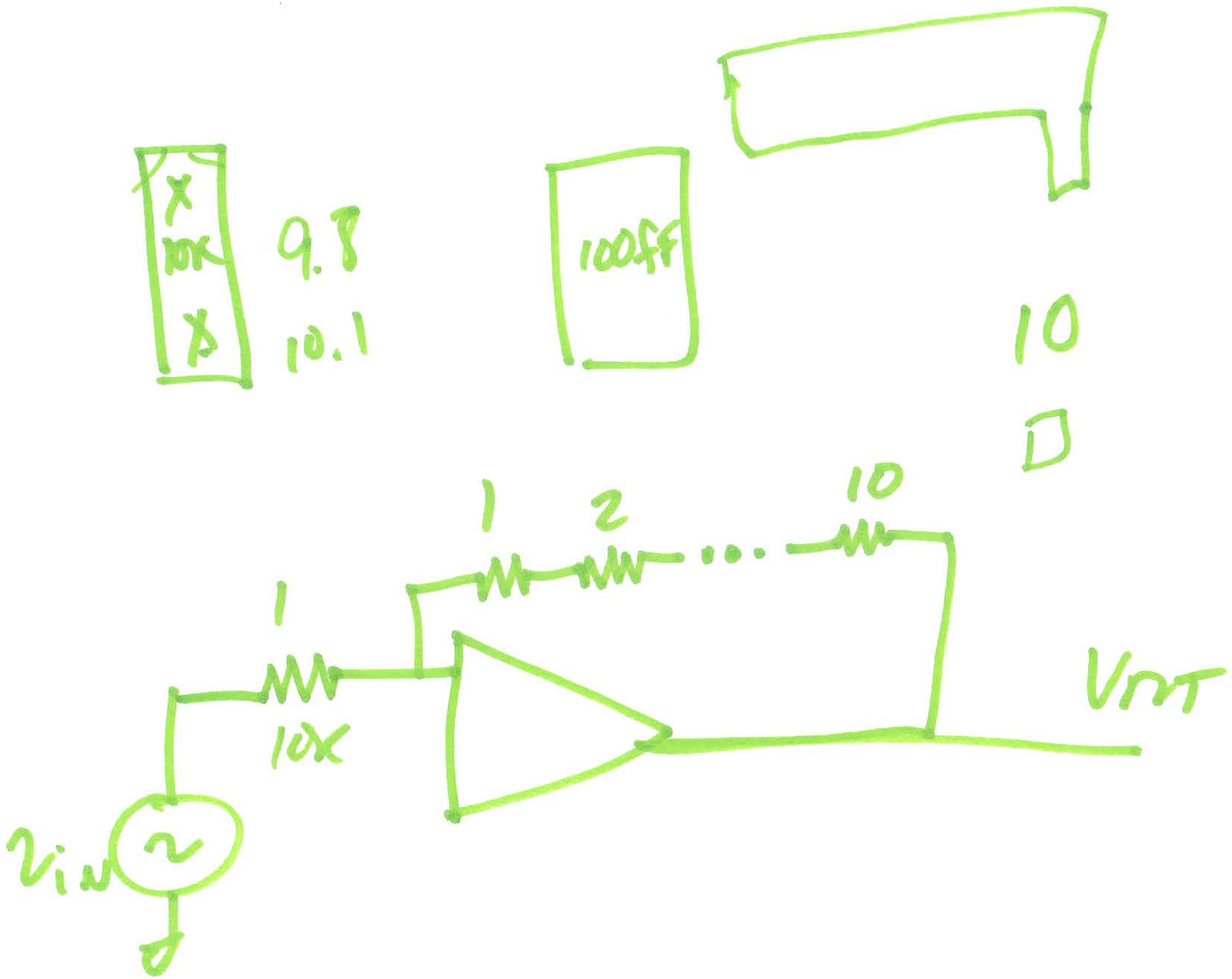






$$V_{OUT} = V_{IN} \cdot \frac{C_1}{C_1 + C_2}$$

MIM capacitors

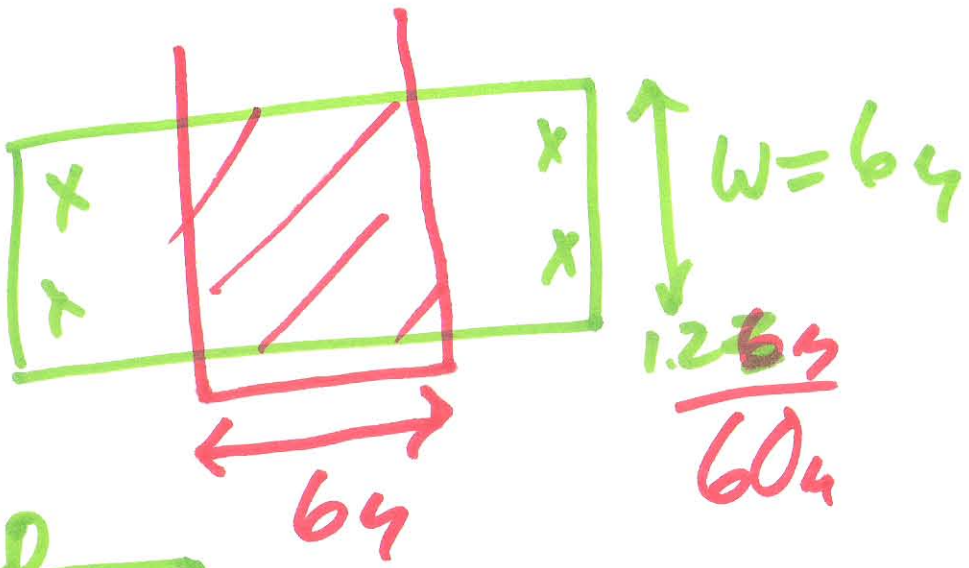


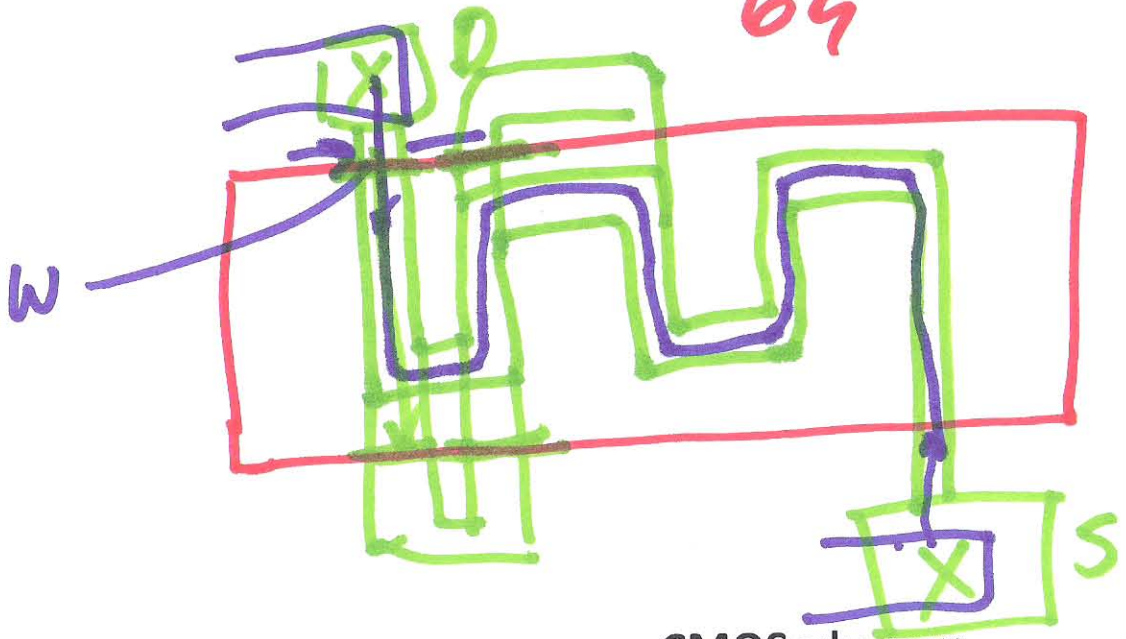
7)

Long L devices

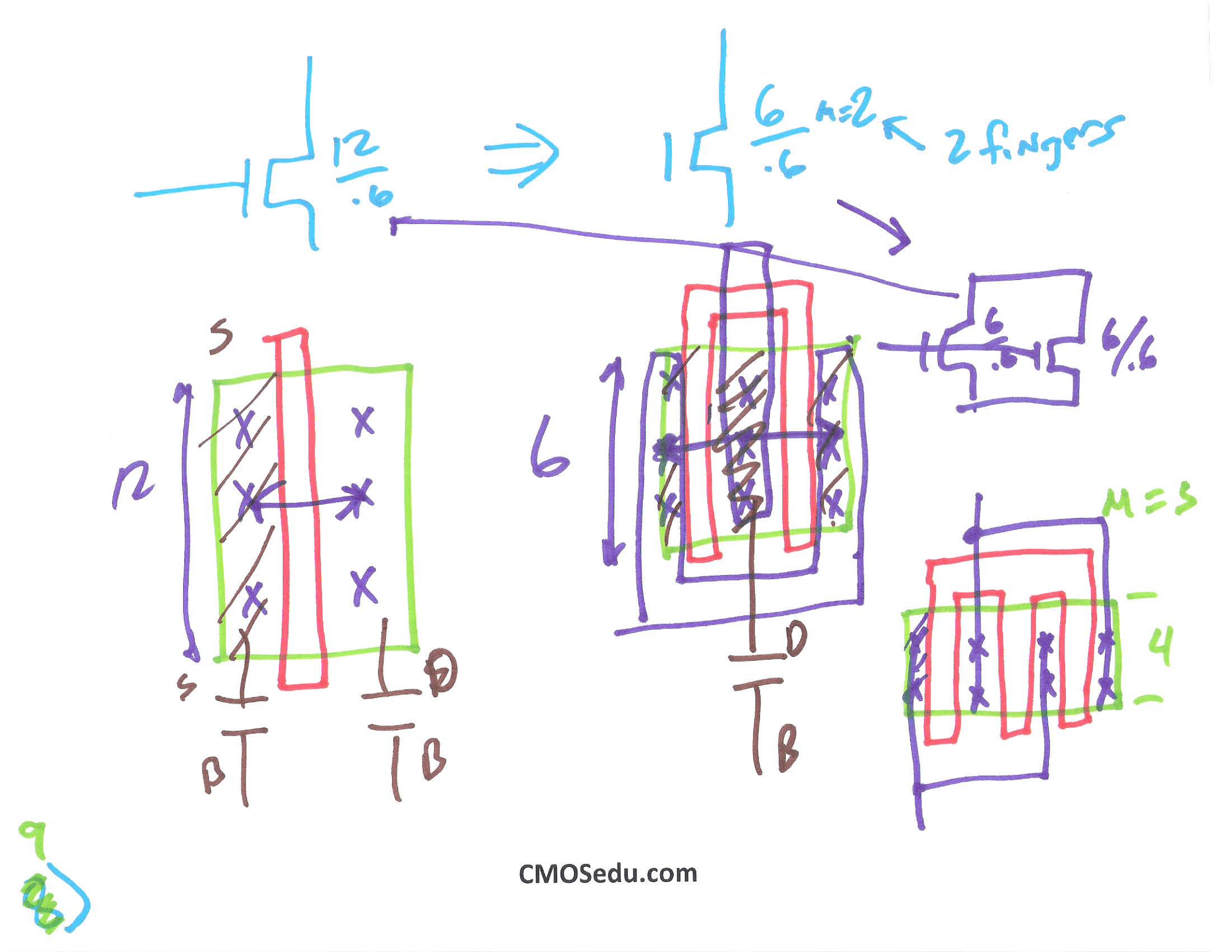
Length

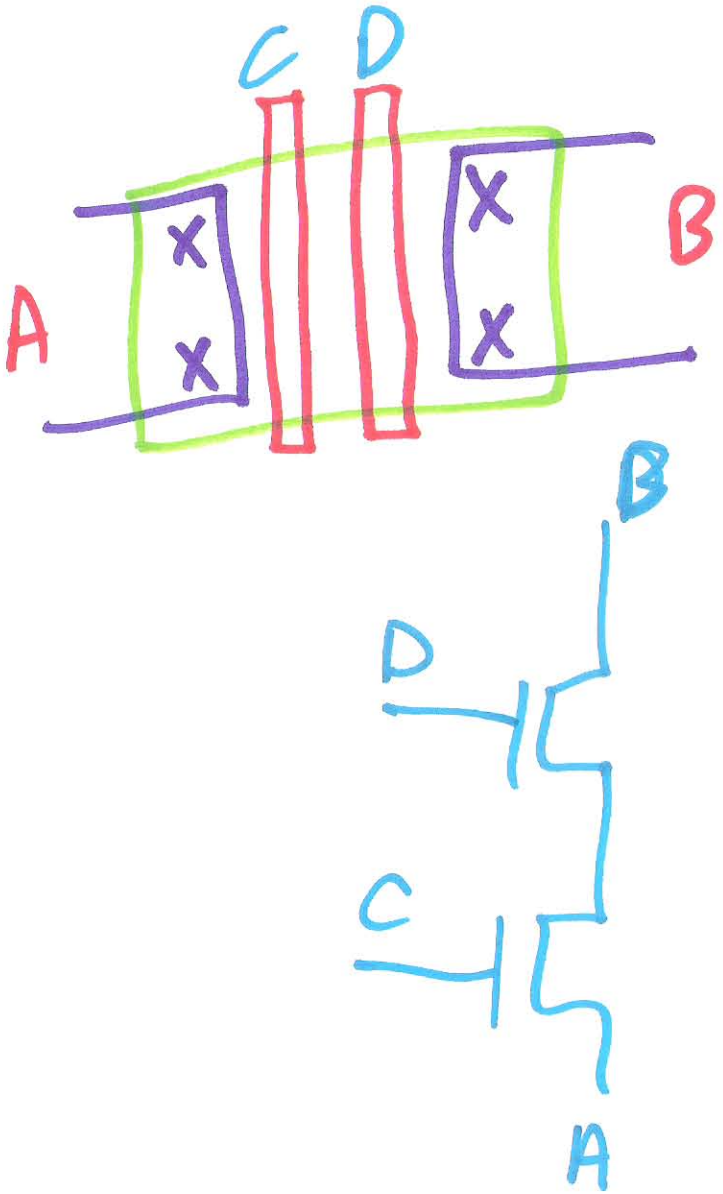
64/6μ

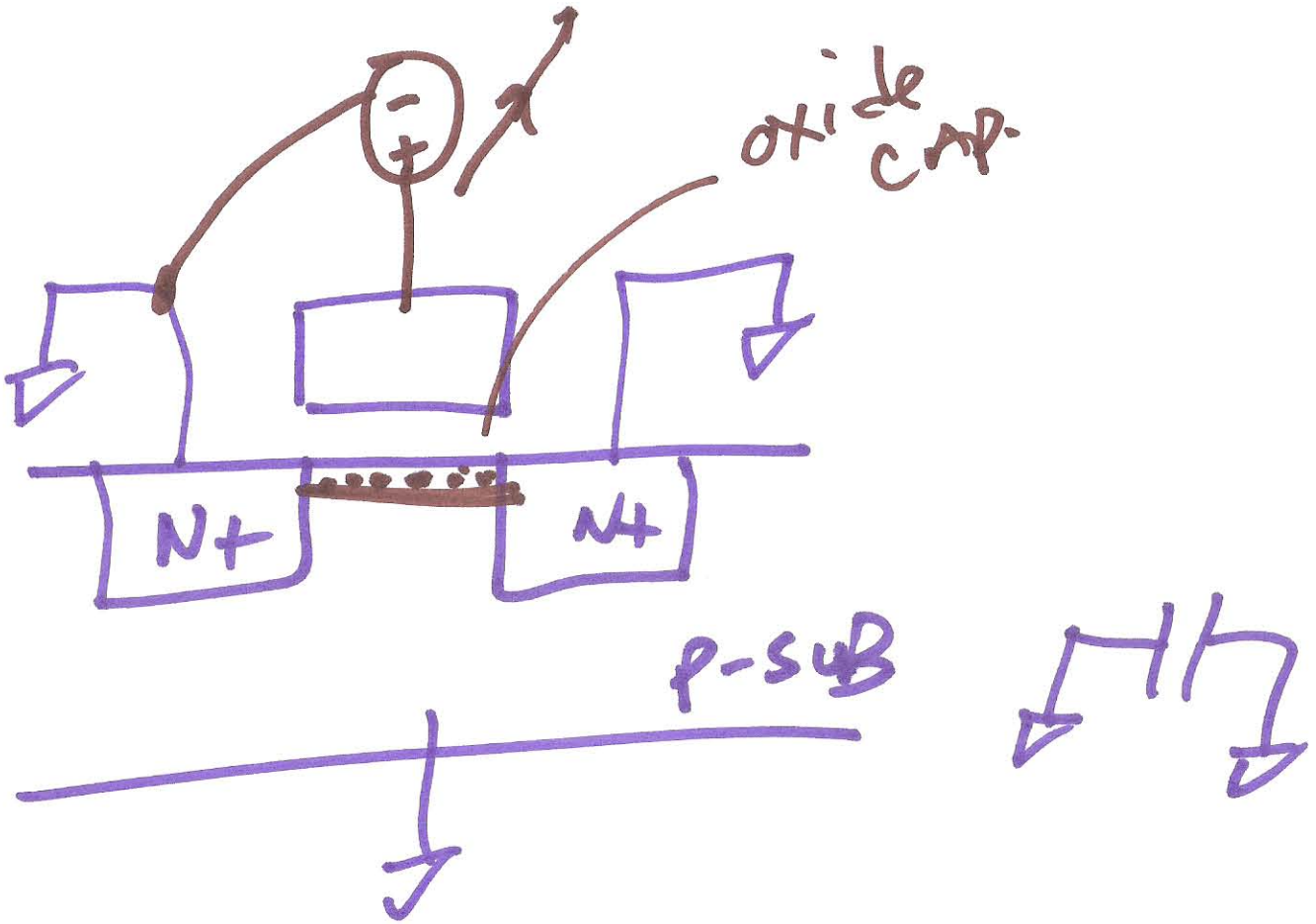




8)


12/.6
6/.6 M=2
2 fingers
S
12
S
D
TB
6
D
TB
6/.6
M=3
4





11)