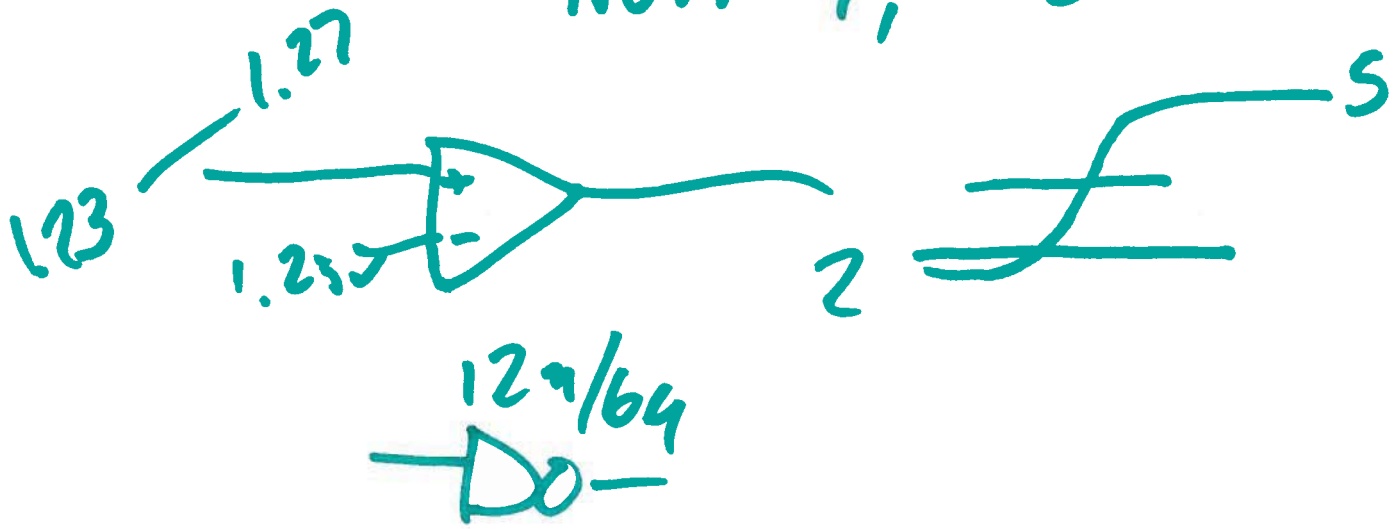
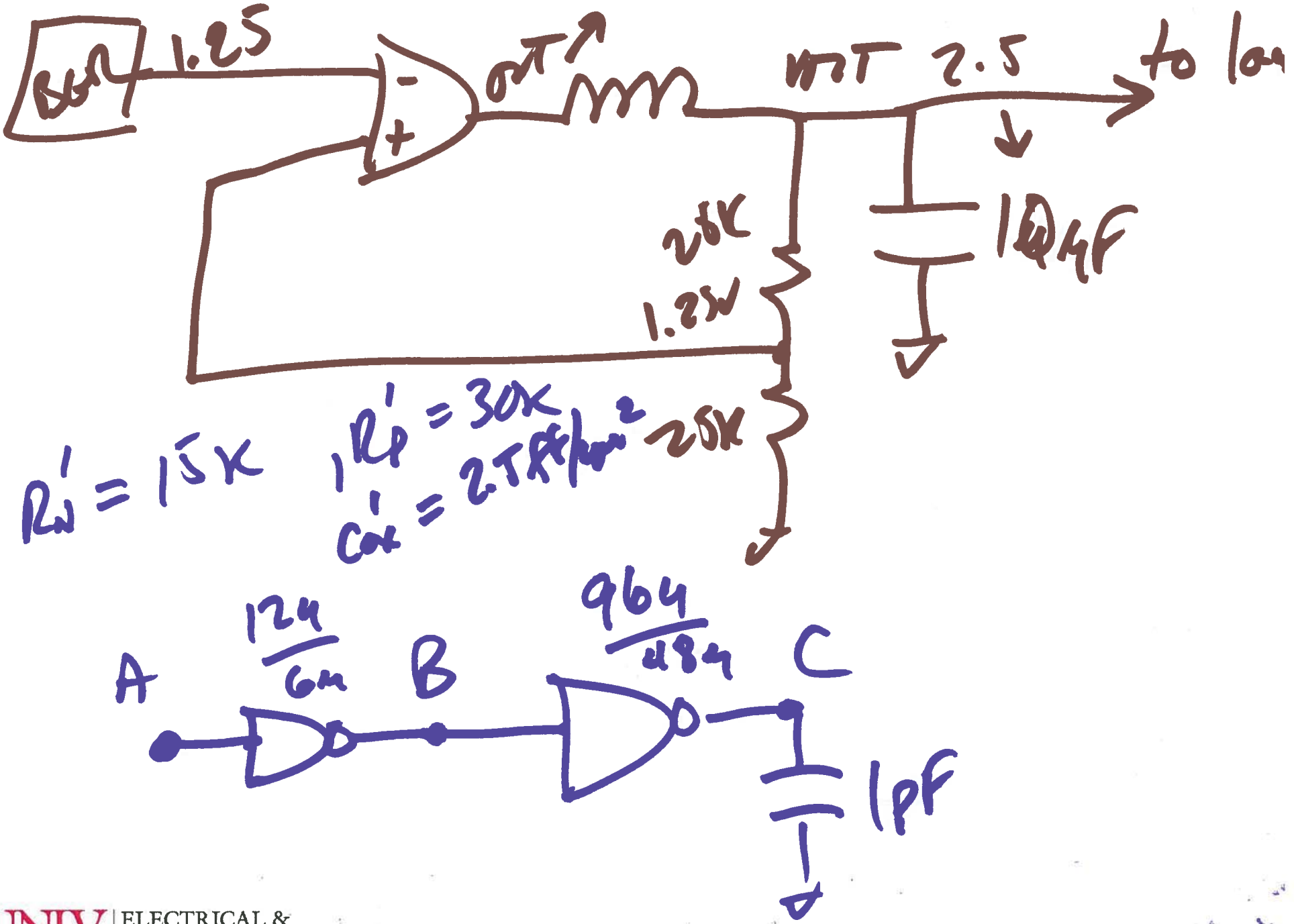
EE 421/ECG 621

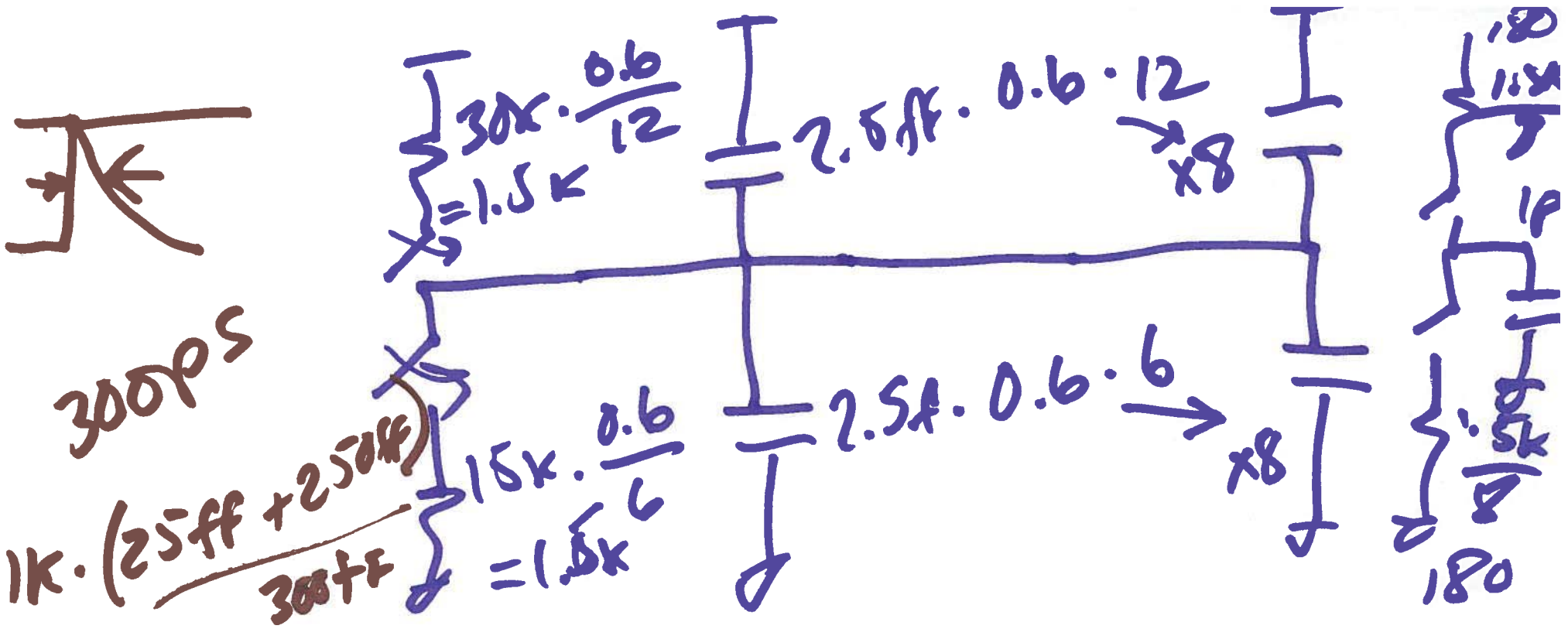
Digital IC Design

Lecture 18

NOV. 7, 2016




1.25
OUT
2.5
to load
25K
1.25W
100pF
$R_N' = 15K$
$R_P' = 30K$
$C_{ox}' = 2.5fF/\mu m^2$
25K
A
12μ/6μ
B
96μ/48μ
C
1pF



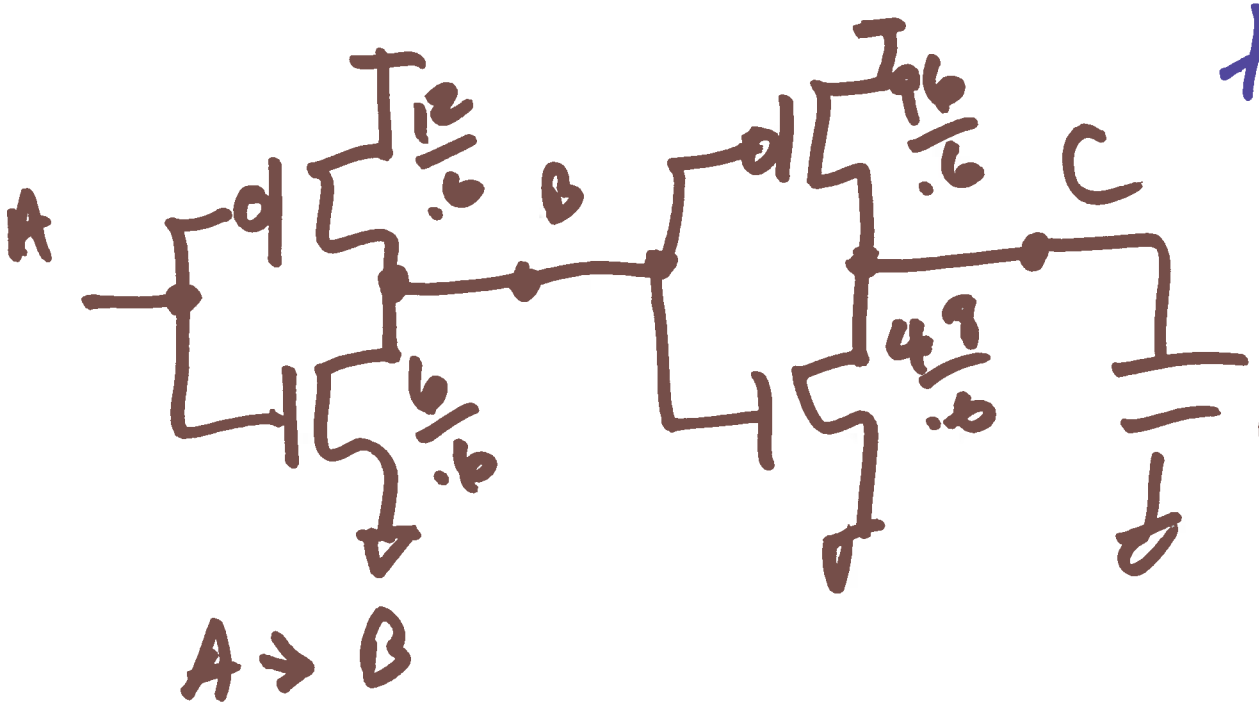
$A \rightarrow B$

$$t_{PHL} = t_{PLH} = 1.5k \cdot .7 \left(9 \cdot 2.5ff \cdot 0.6 \cdot (6+12) \right)$$

$$= 1.5k \cdot .7 \cdot \left[(2.5ff \cdot .6 \cdot 18) + \tfrac{3}{2} 2.5ff \cdot .6 \cdot 18 \cdot 8 \right)$$

$\approx 3ns$

3)



$t_{PHL} = t_{pLH} =$

$0.7 \cdot \frac{1.5K}{8} \cdot (1pf + 2pf)$

$\simeq 150ps$

$26ff$

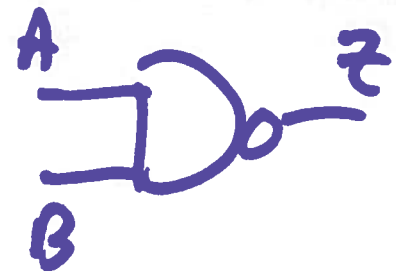
$t_{PHL} = t_{pLH} = 0.7 \cdot 1.5K \cdot (2.5ff \cdot 0.6 \cdot (12+6)$

$+ \frac{3}{2} 2.5ff \cdot 0.6 (12+6) \cdot 8)$

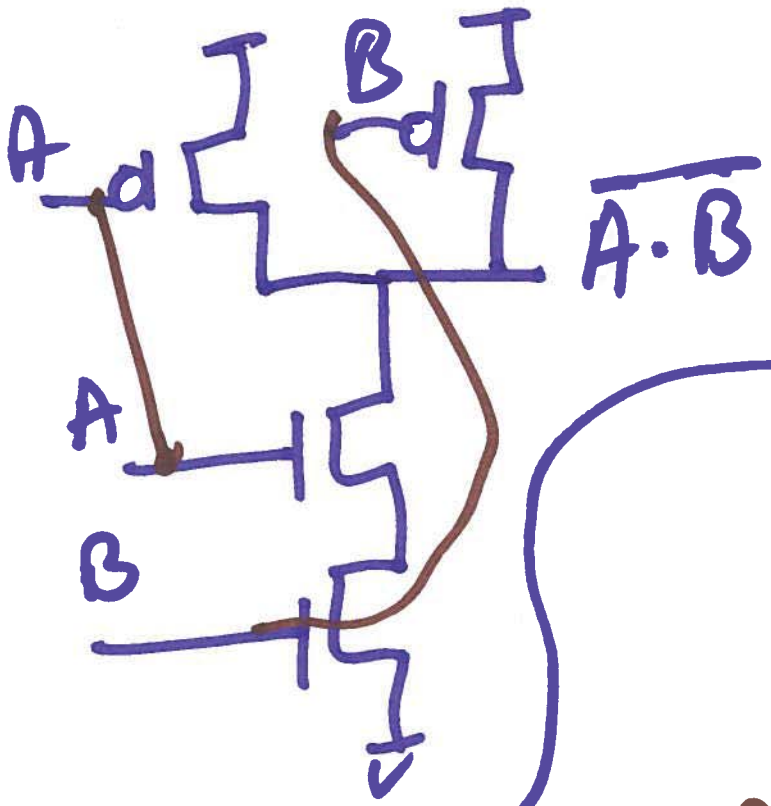
$300ff$

$\simeq 380ps$

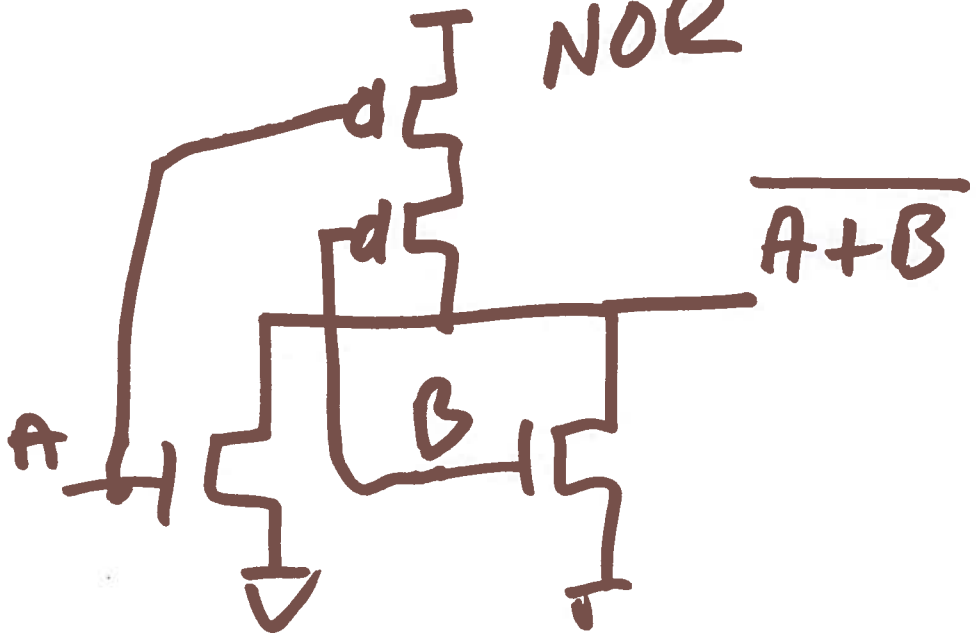
NAND GATE



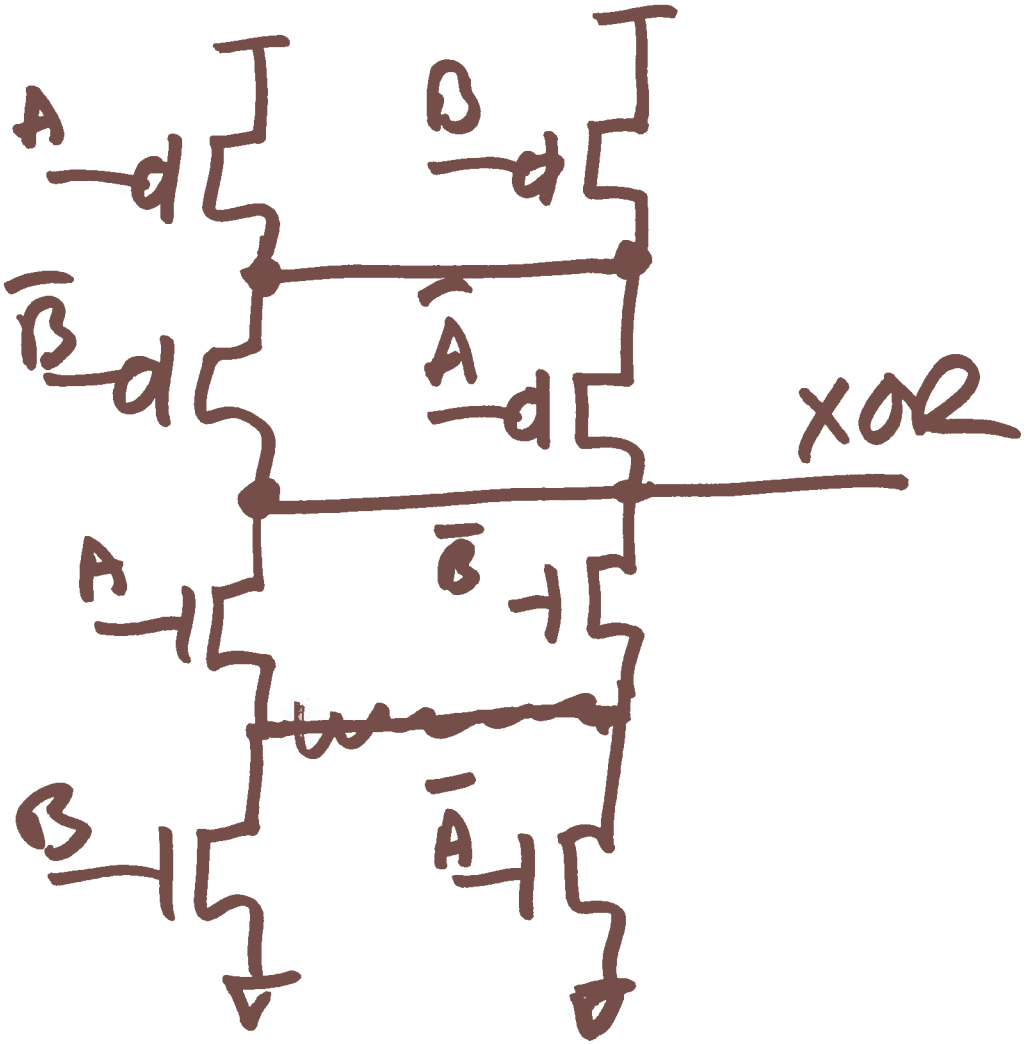
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0



NOR



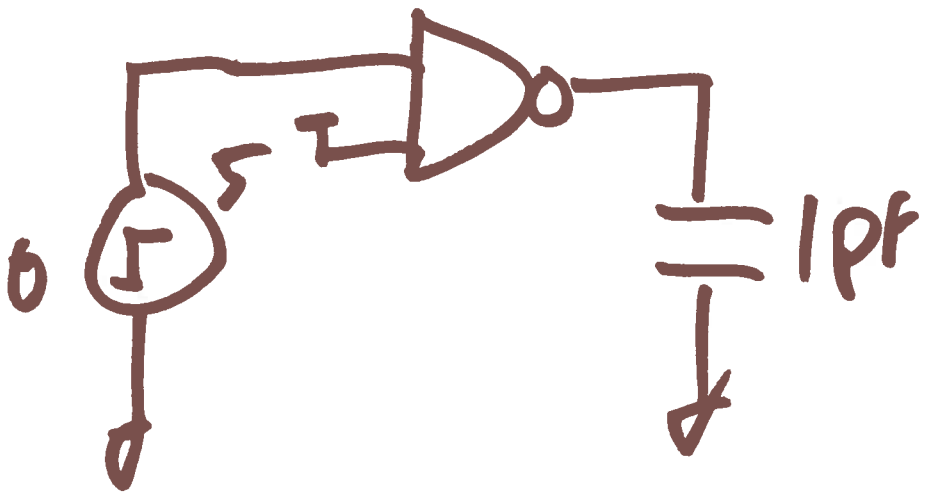
CMOS XOR



A	B	S
0	0	0
0	1	1
1	0	1
1	1	0

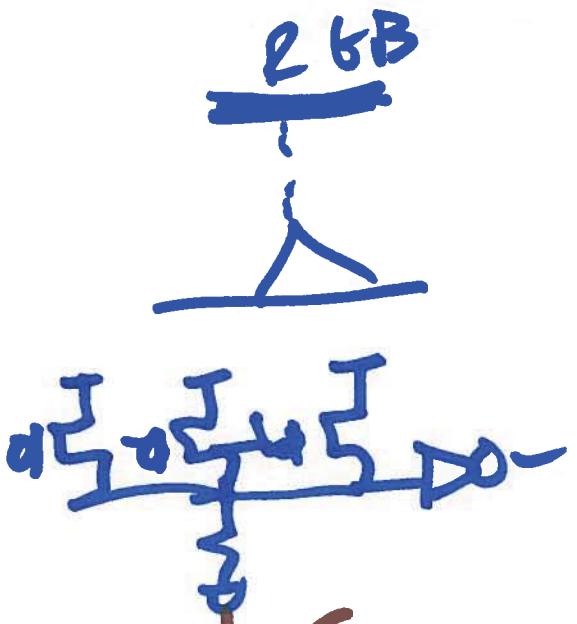
→ C

$$Z = \bar{A}B + A\bar{B}$$

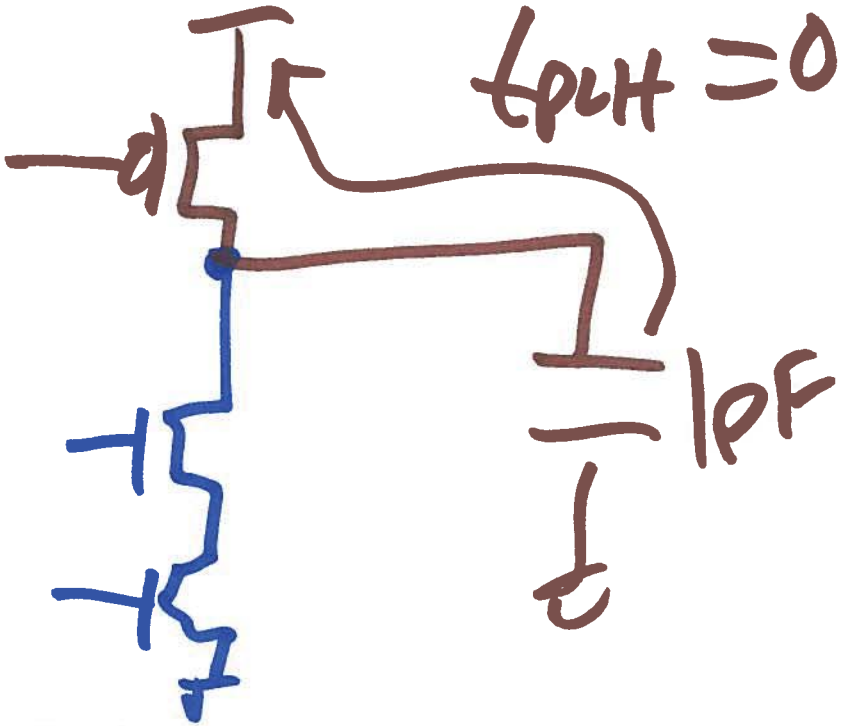


t_{PHL}

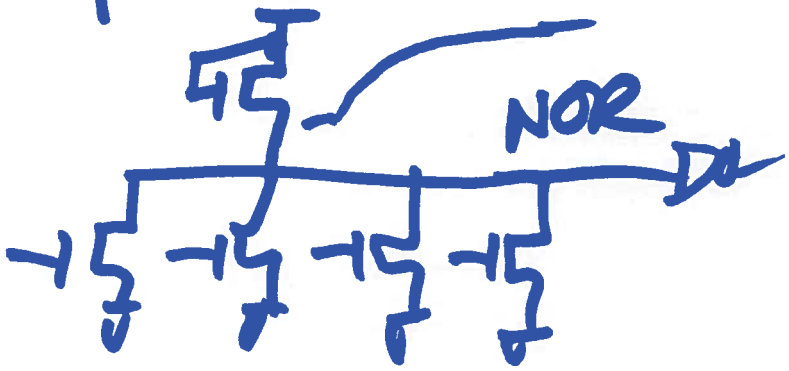
t_{PLH}



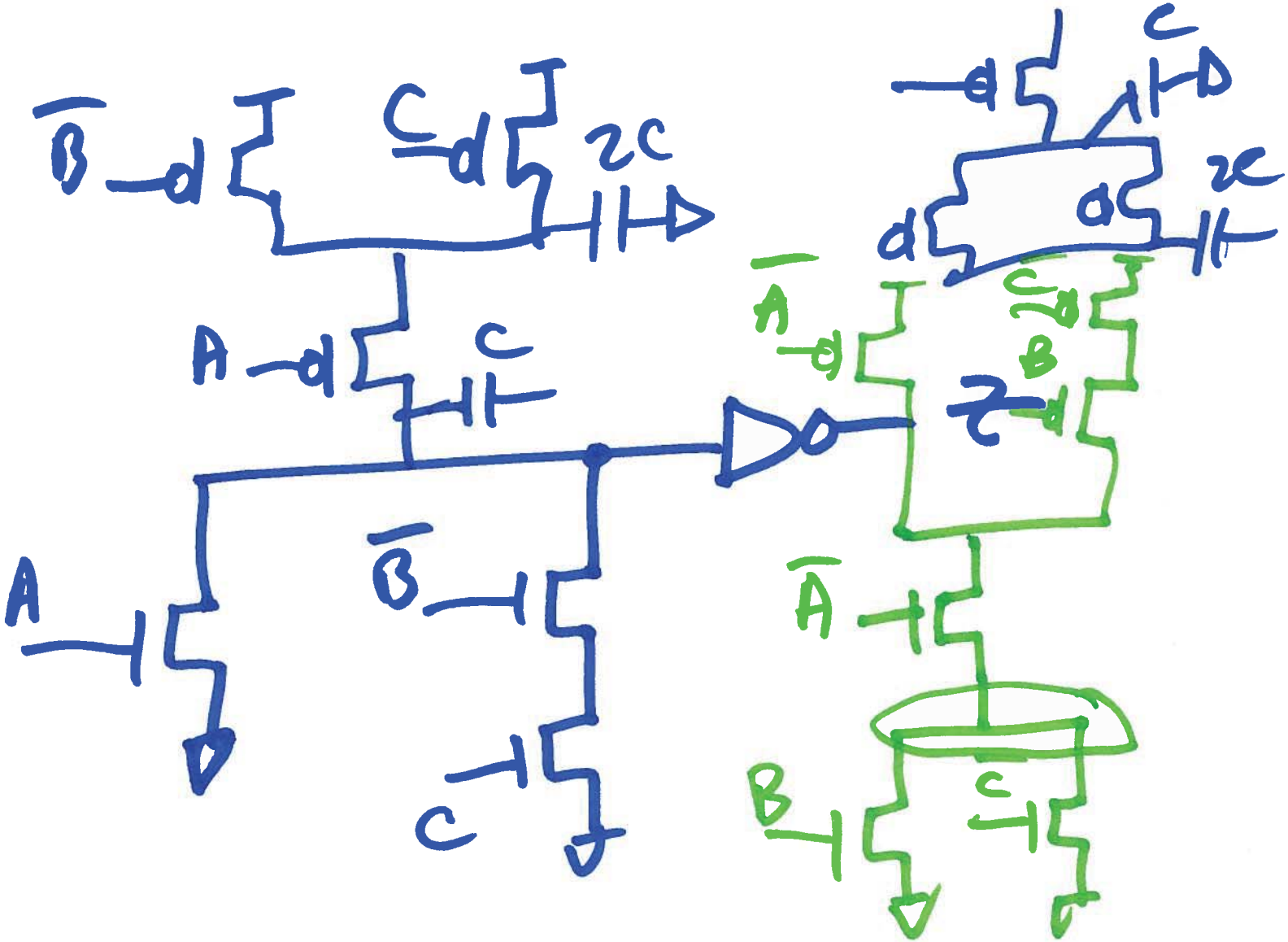
$t_{PLH} = 0.7 \cdot R_p \cdot 1pF$

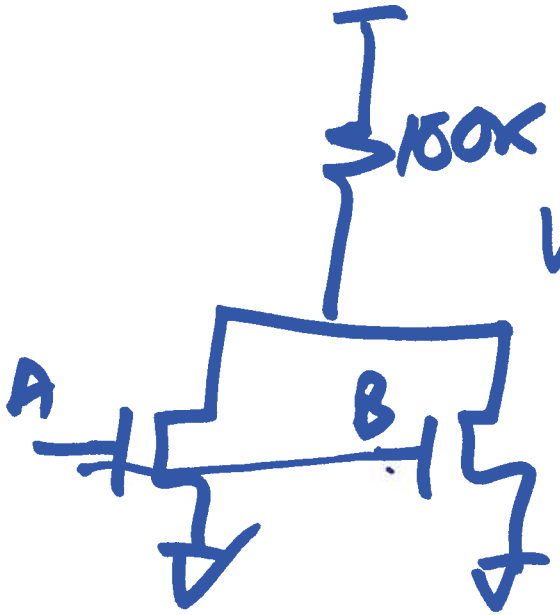


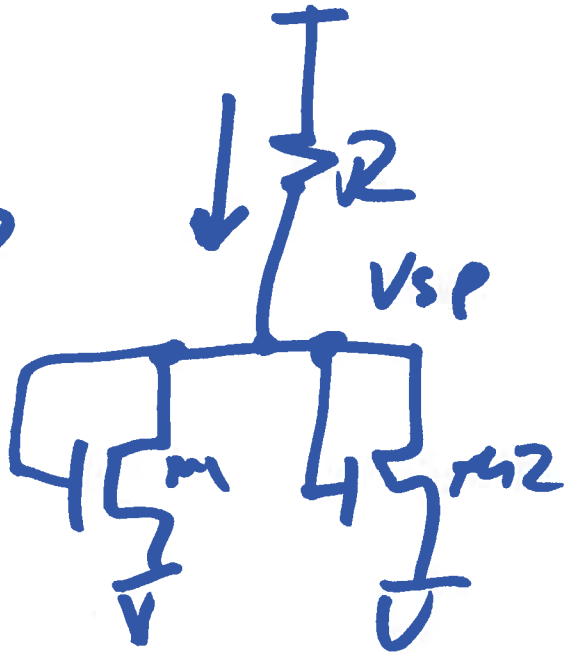
$t_{PHL} = 0.7 \cdot 2R_n \cdot 1pF$



$$Z = A + \bar{B}C$$







$$\frac{VDD - VSP}{R} = I_{M1} + I_{m2}$$

$$\frac{VDD - V_{O2}}{R} = I_{D1} \text{ in triode}$$

$$I_{D2} = \frac{K_n W}{2 L}\left((V_{GS} - V_{TH})\,VDS - \frac{VDS^2}{2}\right)$$

VDD

V_{OL}