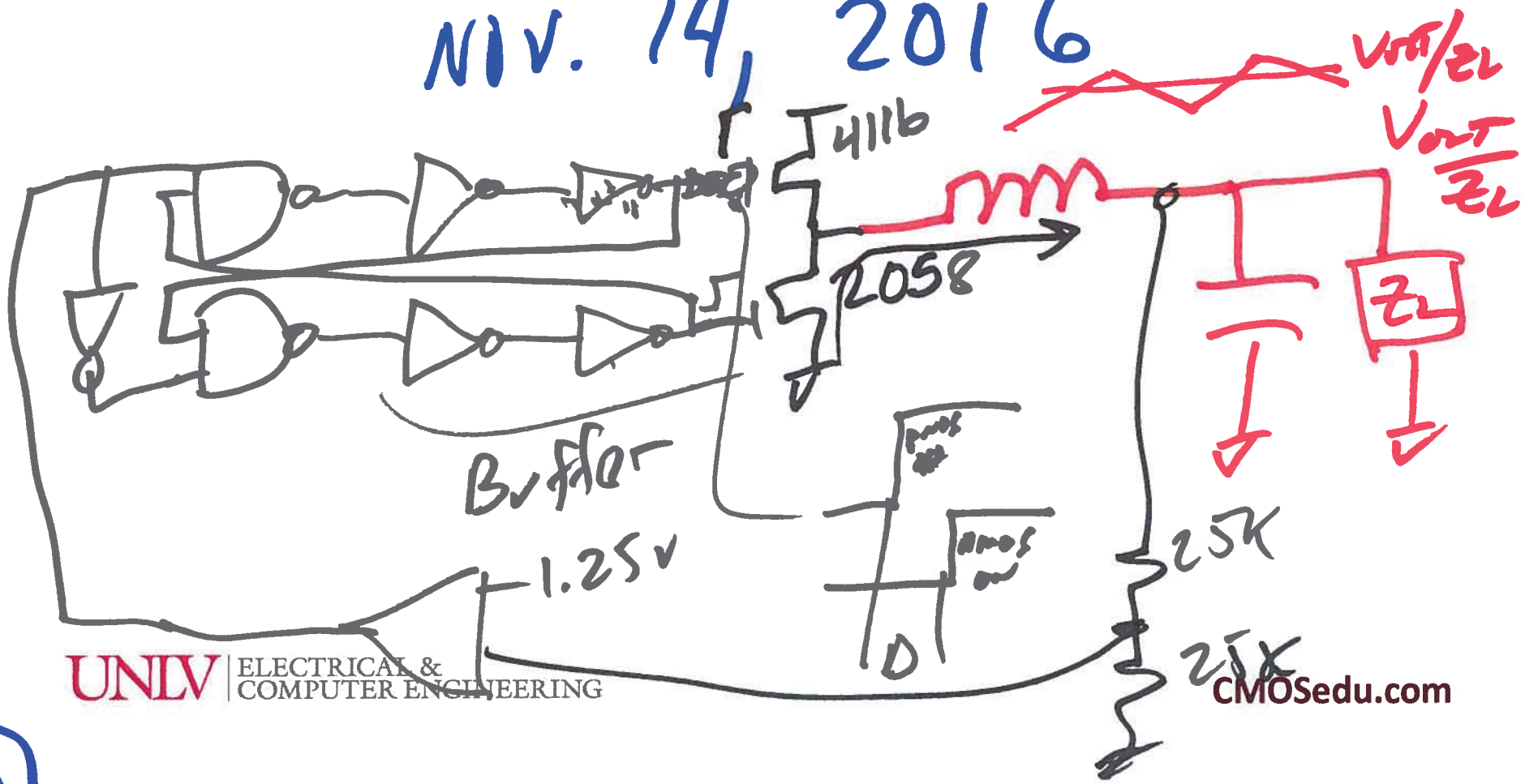
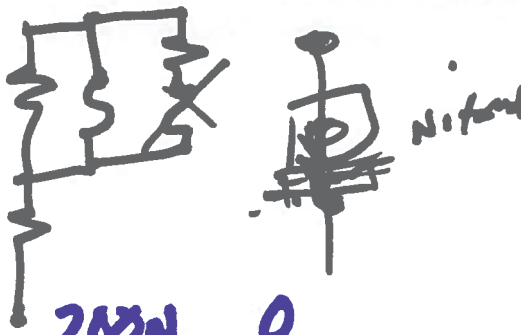
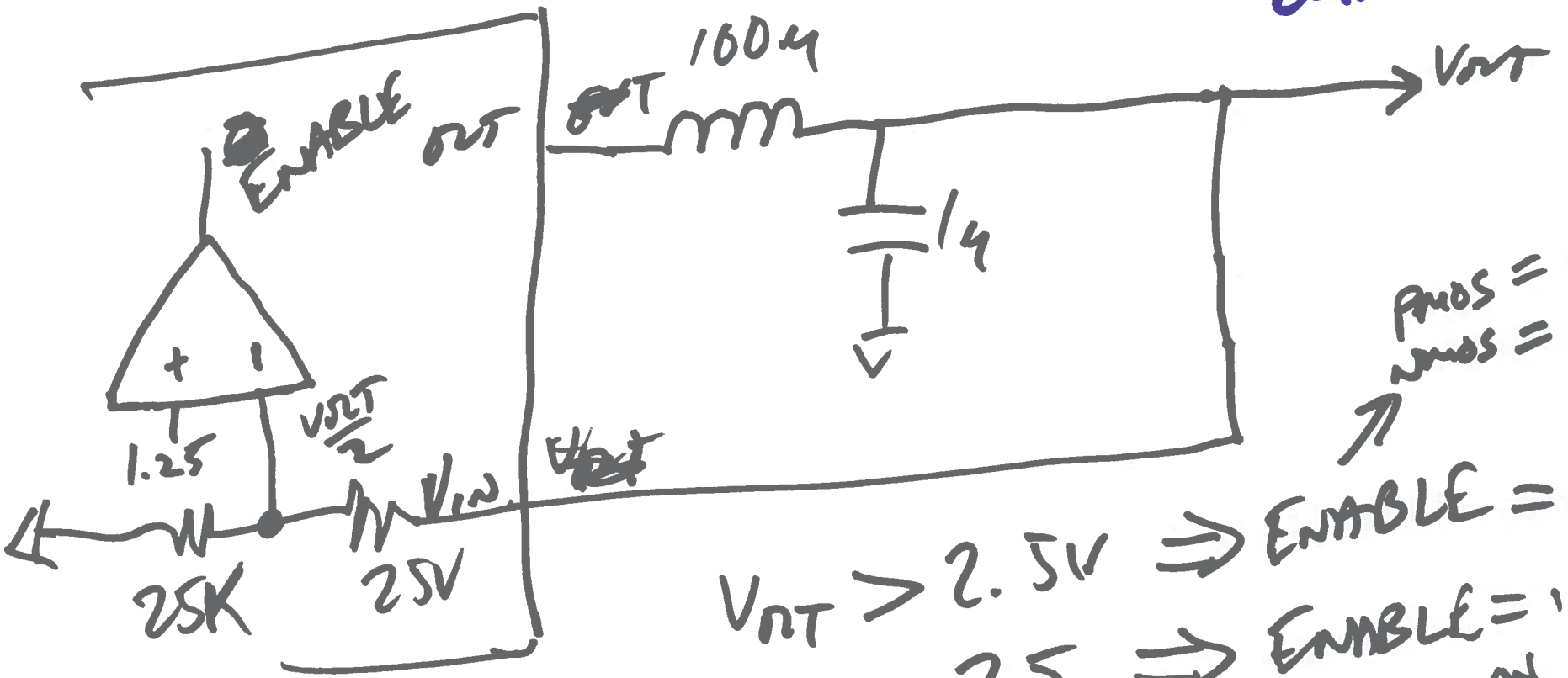
EE 421/621
Digital IC Design
Lecture 19
Nov. 14, 2016





0 5 100NS 5 101NS 0 200N 0

201N 5

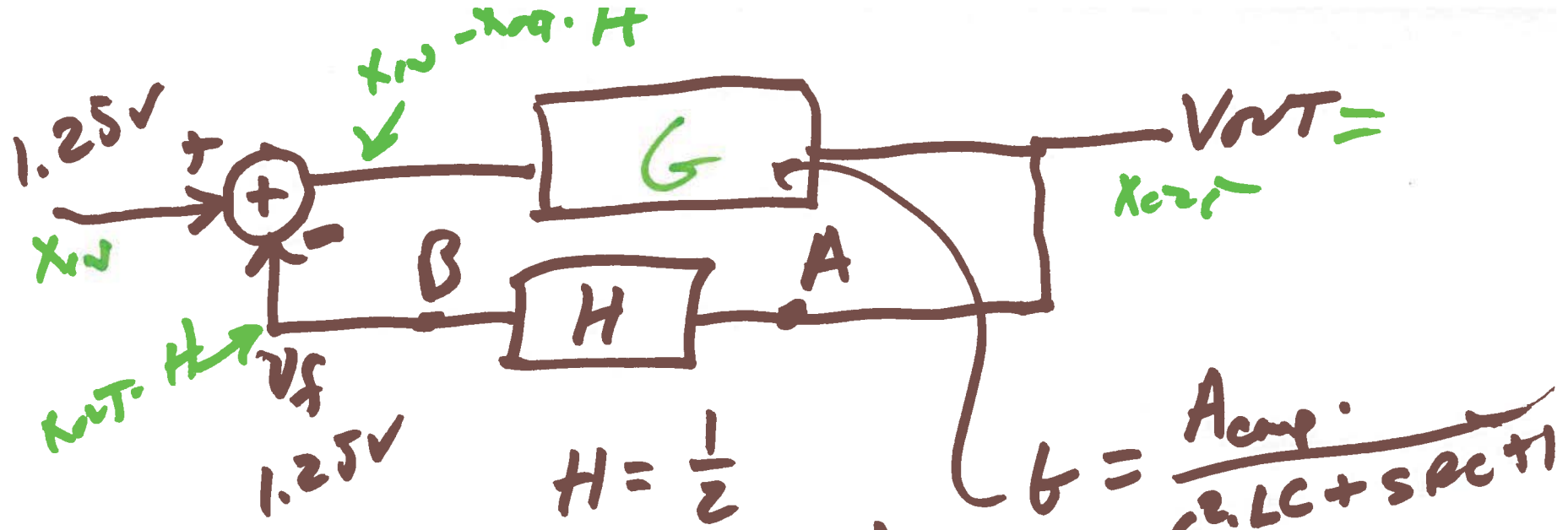


PMOS = off
NMOS = ON

$V_{OUT} > 2.5V \Rightarrow$ ENABLE = 0

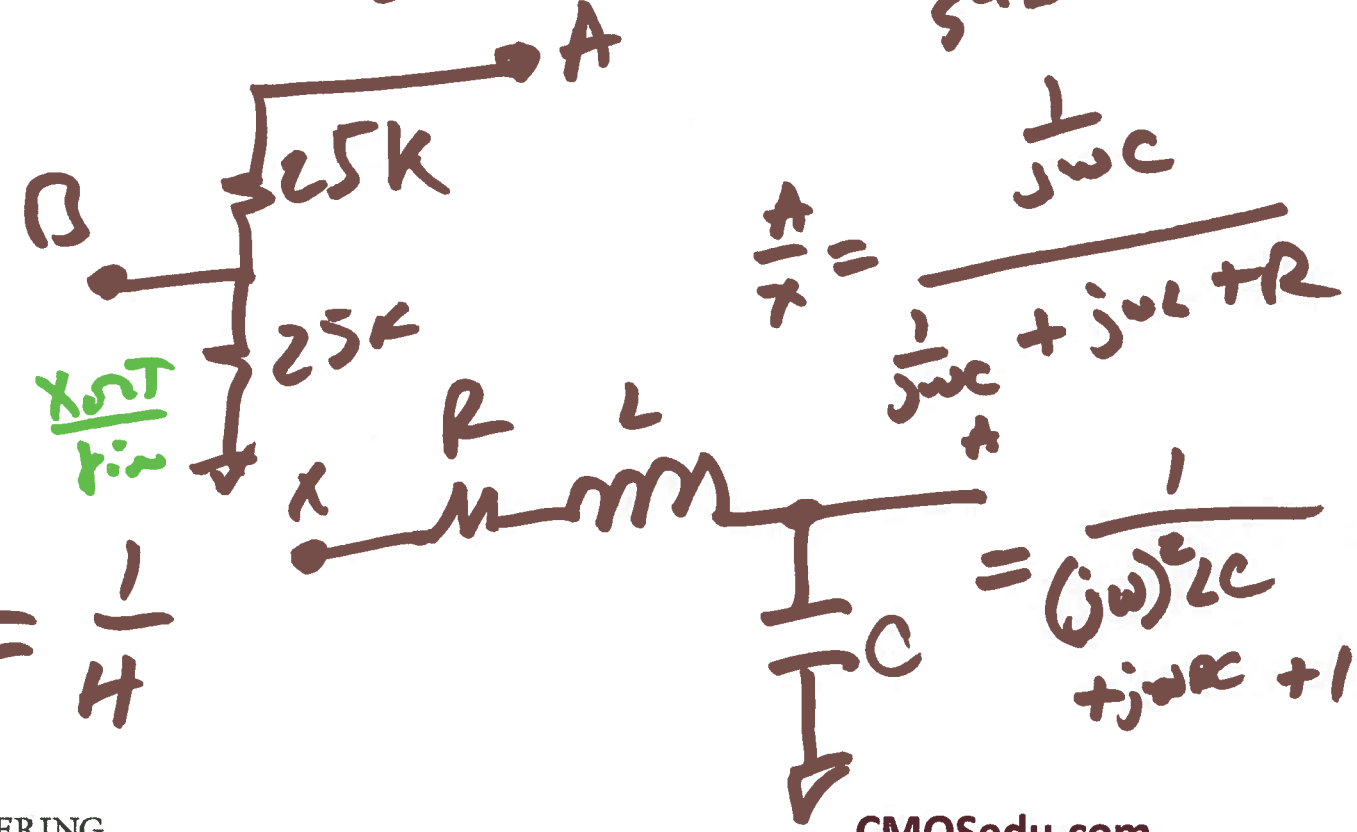
$V_{OUT} < 2.5 \Rightarrow$ ENABLE = 1

PMOS = ON
NMOS = off



$H = \frac{1}{2}$

$G = \frac{A_{amp}}{s^2 LC + sRC + 1}$

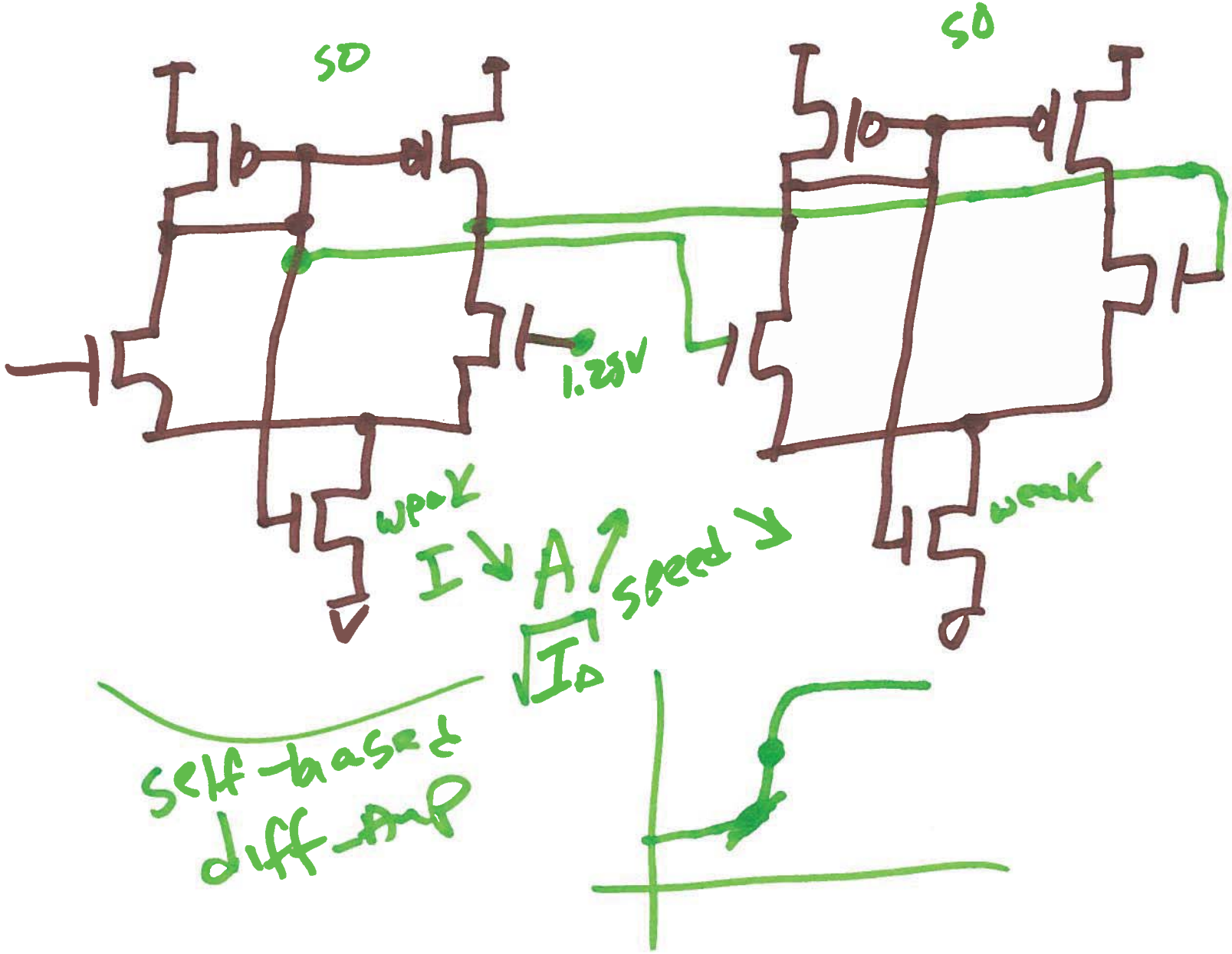


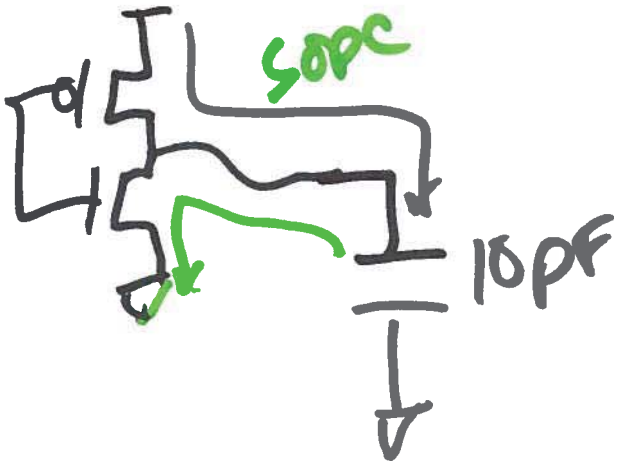
$$\frac{A}{X} = \frac{\frac{1}{j\omega C}}{\frac{1}{j\omega C} + j\omega L + R}$$

$$= \frac{1}{(j\omega)^2 LC + j\omega RC + 1}$$

$$A_{CL} = \frac{G}{1+GH} = \frac{X_{OUT}}{X_{IN}}$$

$$A_{CL} = \frac{1}{\frac{1}{G} + H} = \frac{1}{H}$$

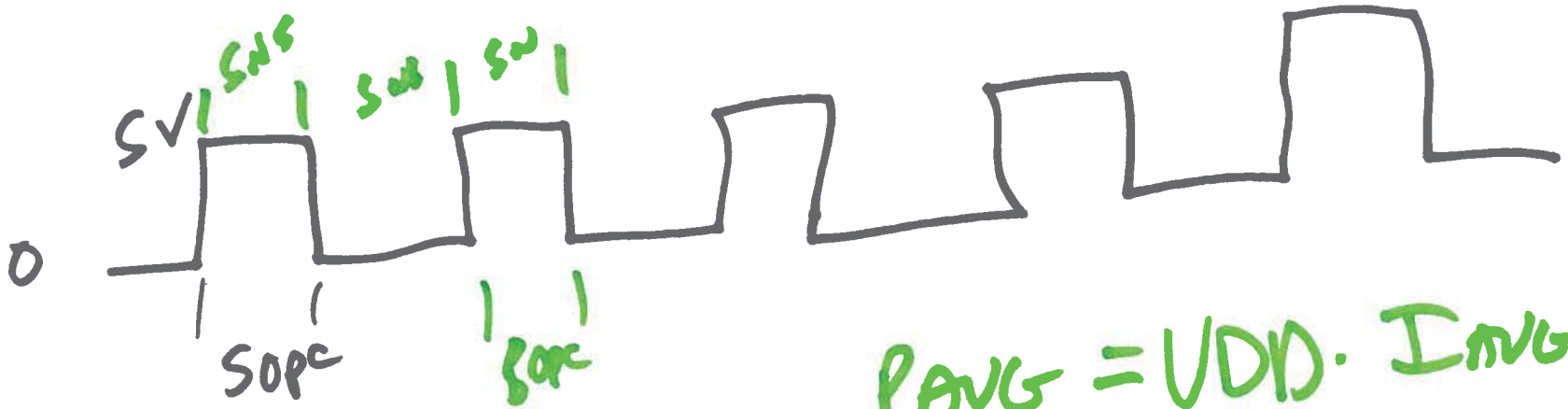

SD
SD
1.25V
weak
weak
I ↘ A ↗ speed ↘
√I_D
self-biased
diff-amp



$$CV = Q = C \cdot VDD$$

$$I_{AVG} = \frac{50pC}{10ns} = 50mA$$

$$= \frac{CVDD}{T} = C \cdot VDD \cdot f$$



$$P_{AVG} = VDD \cdot I_{AVG}$$

$$P_{AVG} = C_L \cdot VDD^2 \cdot f$$