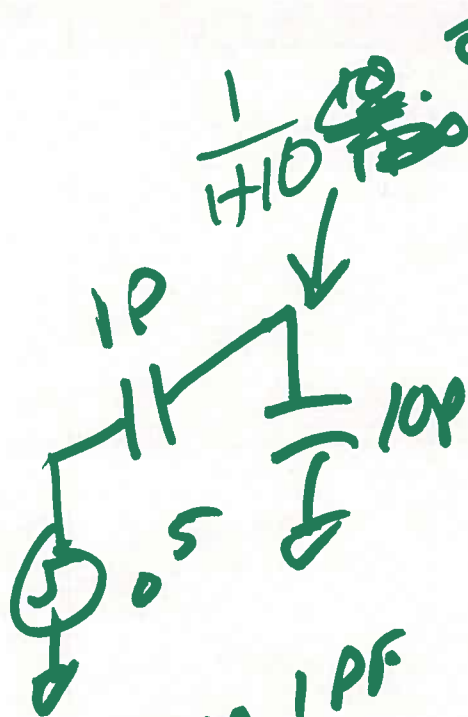


# EE 421 / ECG 621

## Digital IC Design

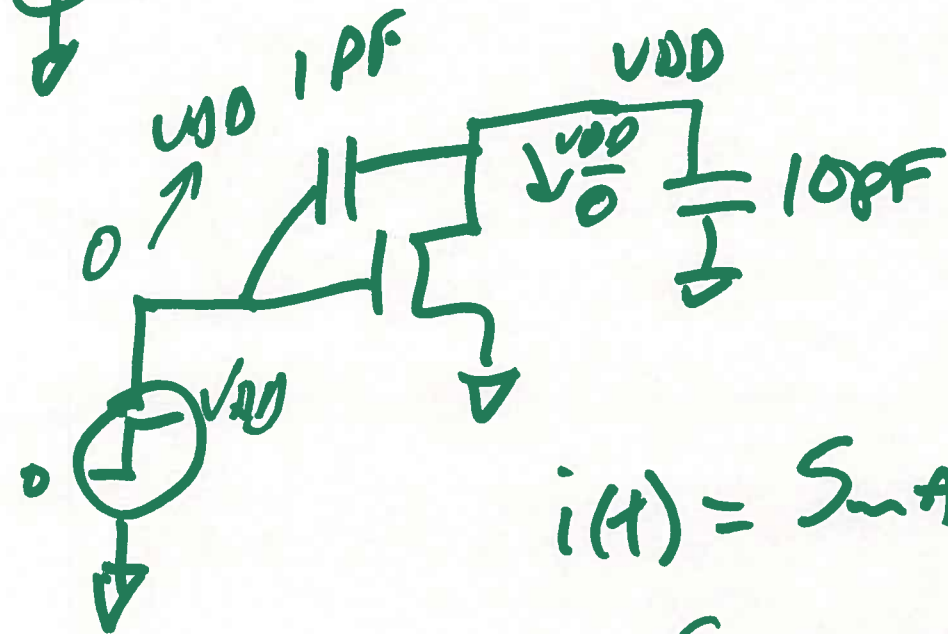
Lecture 16

OCT. 25, 2017



$$Q = 1 \text{ pF} \cdot 2V_{DD}$$

$$V_{DD} = 5V$$



$$i(t) = 5 \text{ mA} \cdot e^{-t/1 \text{ ns}}$$

$$V = -\frac{t}{1 \text{ ns}}$$

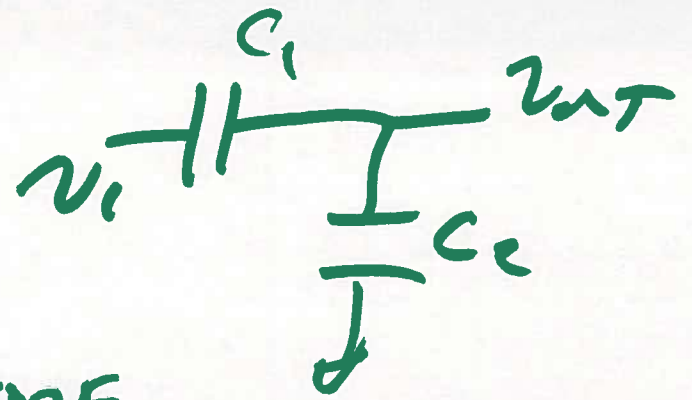
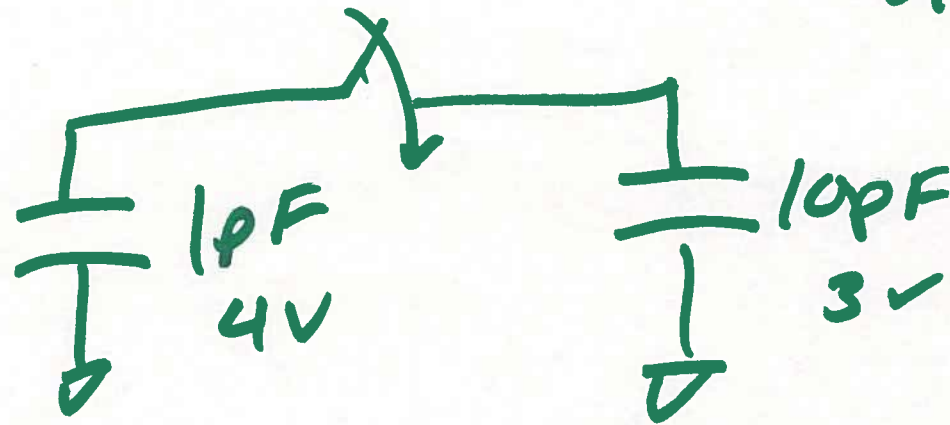
$$du = -\frac{1}{1 \text{ ns}} \cdot dt$$

$$Q_{TOT} = \int i(t) \cdot dt = -5 \text{ mA} \cdot 1 \text{ ns}$$

$$\int e^u \cdot du = 5 \text{ pC}$$

1)

$$CV = Q$$



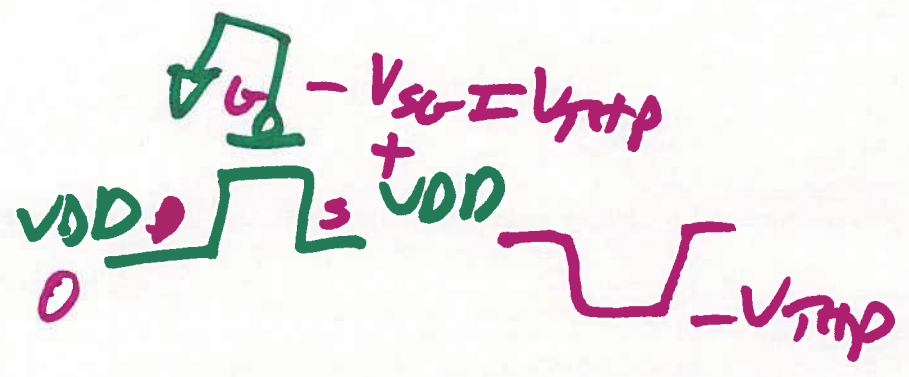
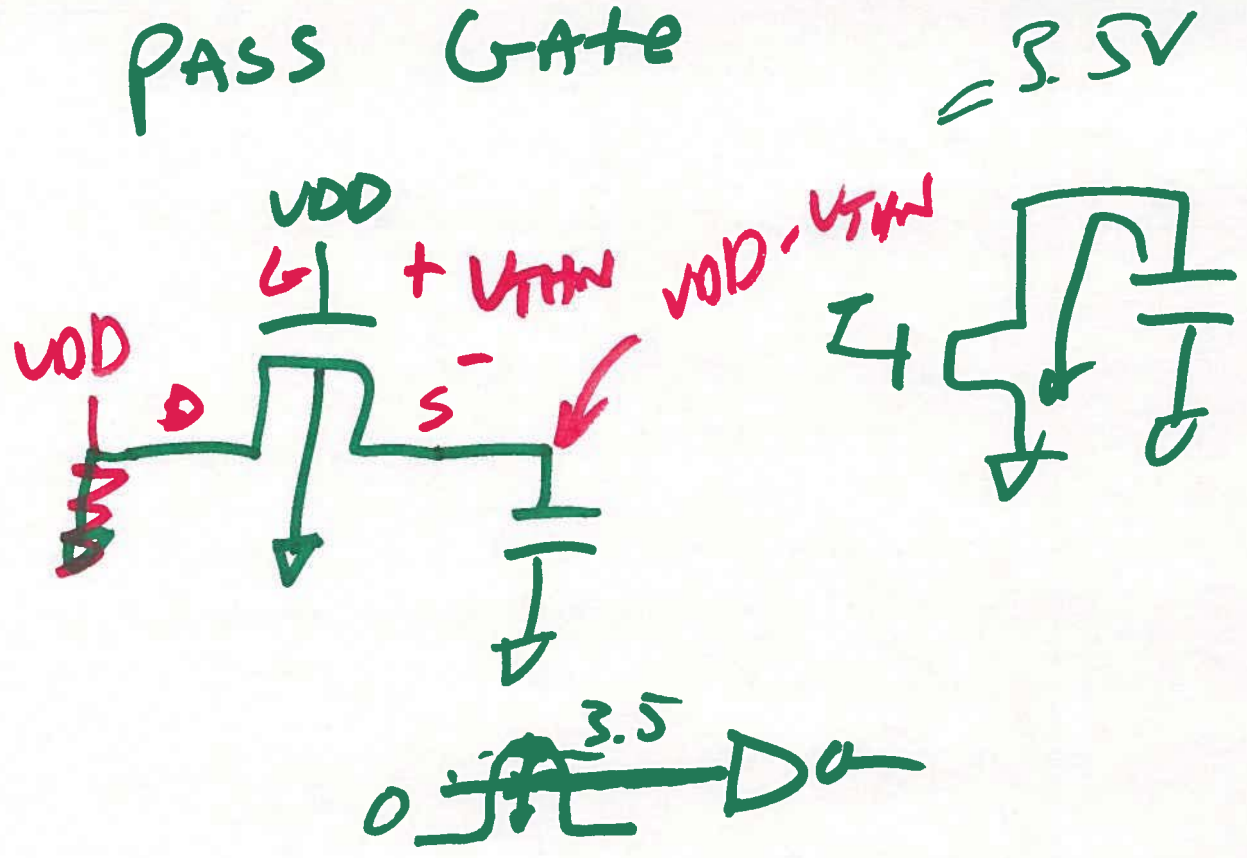
$$4 \cdot 1\text{pF} + 3 \cdot 10\text{pF} = 34\text{pC} = 11\text{pF} \cdot V_F$$

$$V_F = \frac{34\text{pC}}{11\text{pF}} \approx \underline{\underline{3.1\text{V}}}$$

$$v_{out} = v_i \cdot \frac{\frac{1}{j\omega C_2}}{\frac{1}{j\omega C_2} + \frac{1}{j\omega C_1}} = v_i \cdot \frac{C_1}{C_1 + C_2}$$

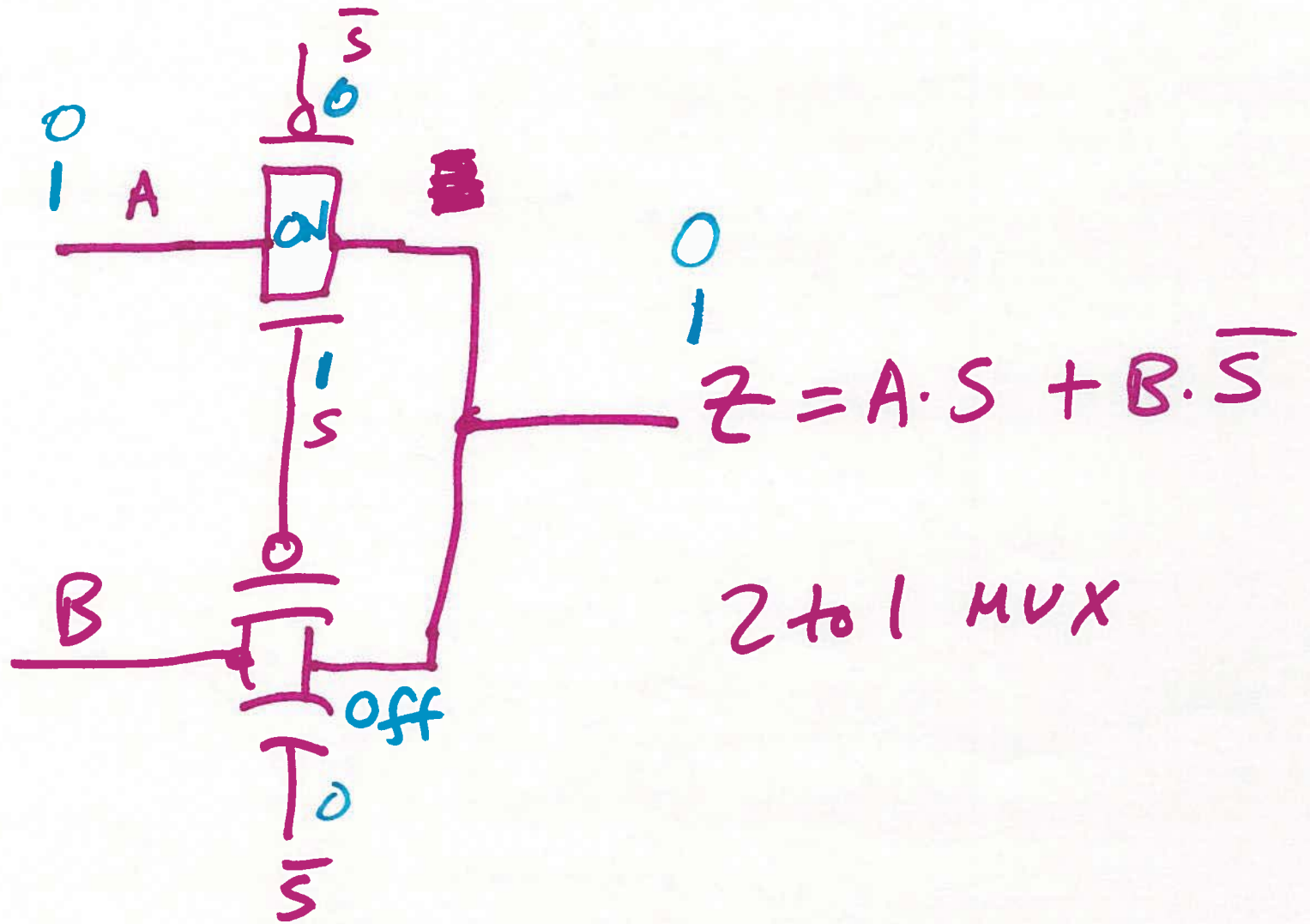
2)

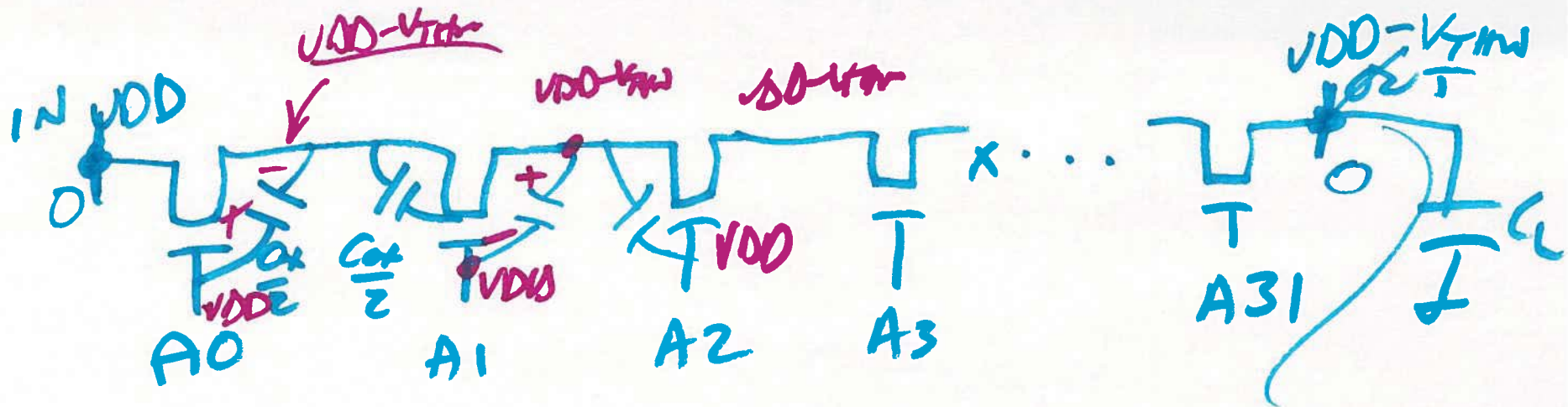
# PASS GATE



3)

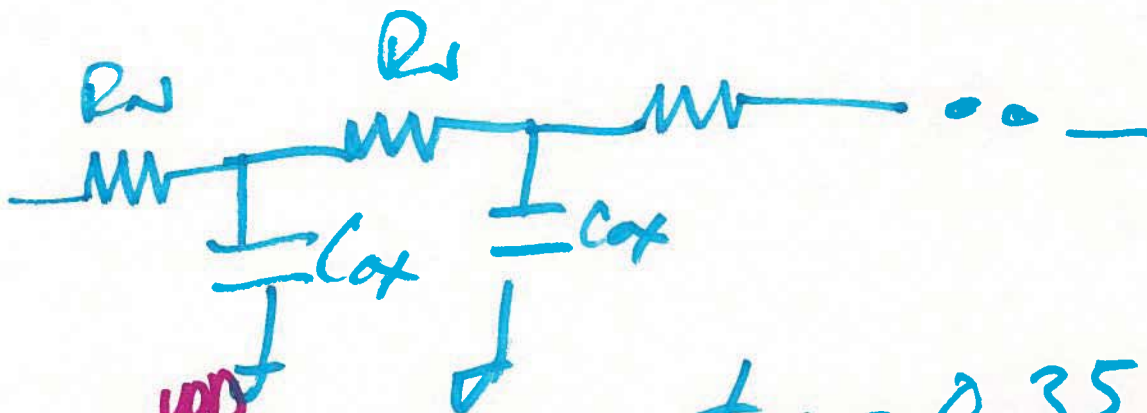
# TRANSMISSION GATE TG





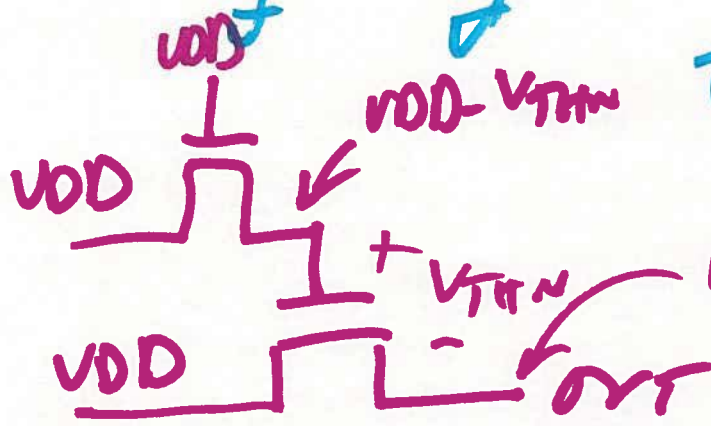
$$t_{p} = 32 R_n \cdot C_L \cdot 2.2$$

HL  
LH



$$t_d = 0.35 \cdot R_n \cdot C_{ox} \cdot 32^2 + 0.7 \cdot 32 R_n \cdot C_L$$

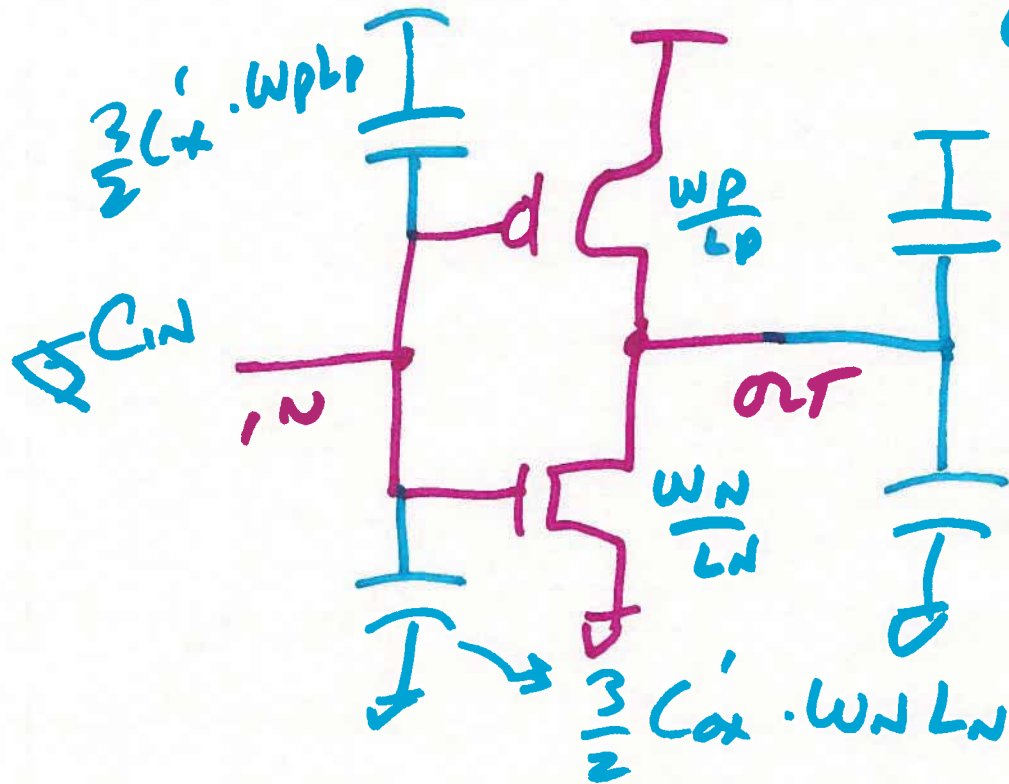
Bad ;)



5)



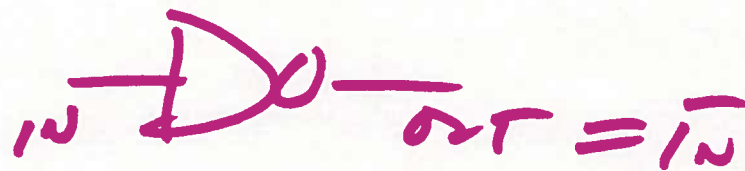
# Inverter

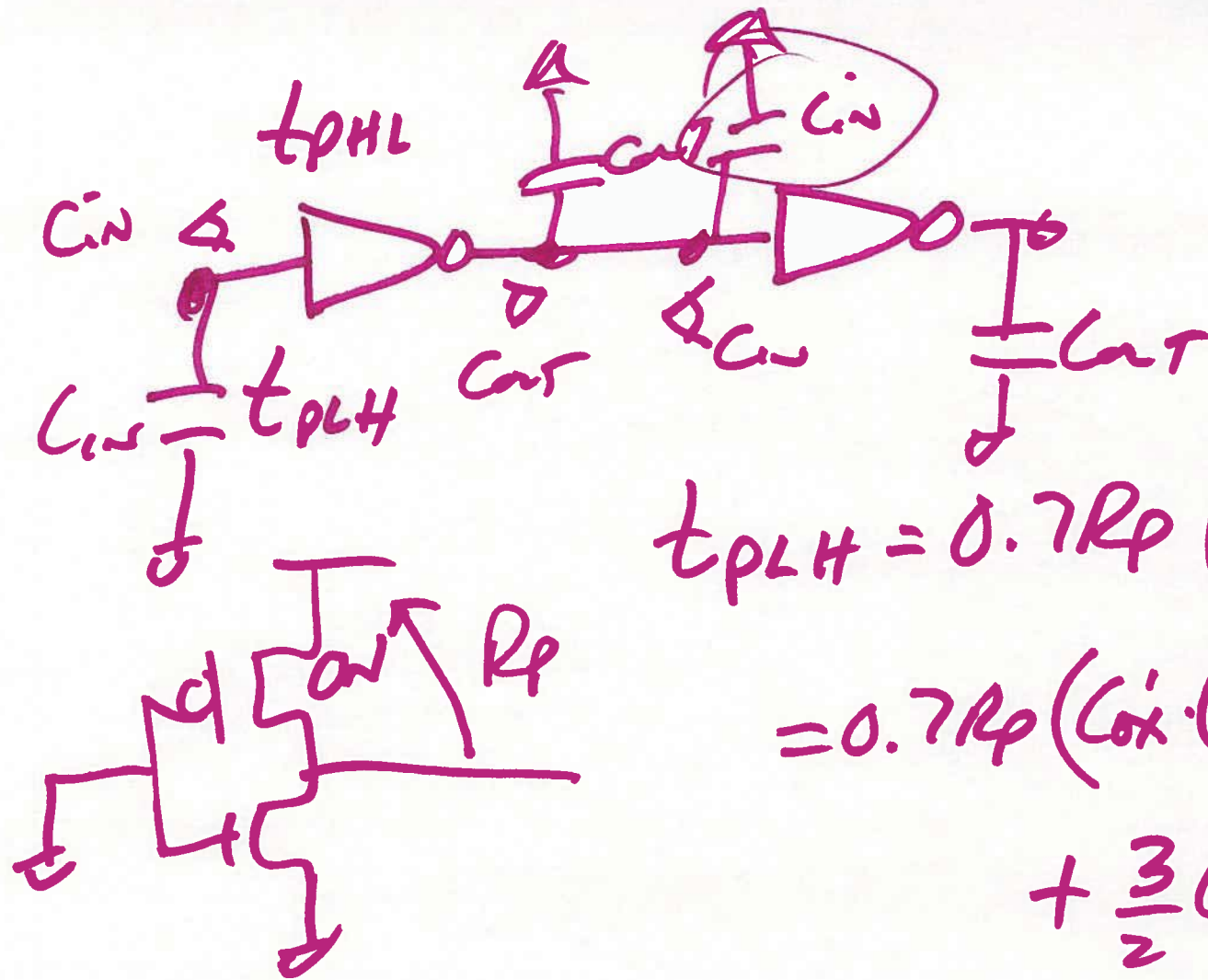


$$C_{IN} = \frac{3}{2} C_{ox}' (w_n L_n + w_p L_p)$$

$$C_{OUT} = C_{ox}' (w_n L_n + w_p L_p)$$

$$C_{IN} = \frac{3}{2} C_{OUT}$$





$$\begin{aligned}
 t_{PHL} &= 0.7 R_p (C_{OUT} + C_{IN}) = \\
 &= 0.7 R_p (C_{ox} \cdot (W_N L_N + W_P L_P) \\
 &\quad + \frac{3}{2} C_{ox} (W_N L_N + W_P L_P))
 \end{aligned}$$