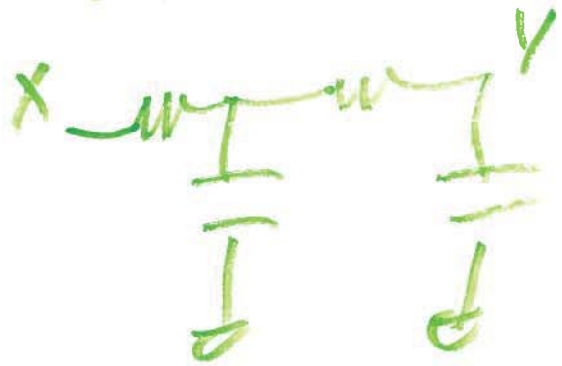
EE421/EC6621
Digital IC Design
Dec. 6, 2017
Lecture 27

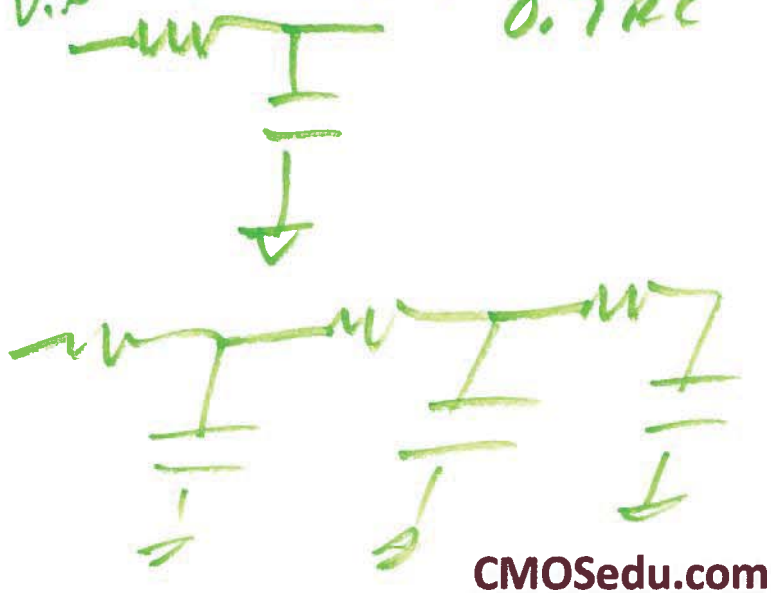
1) LAYOUTS → Read back to Schematic

2) RC delays

0.7RC + 0.7.2RC

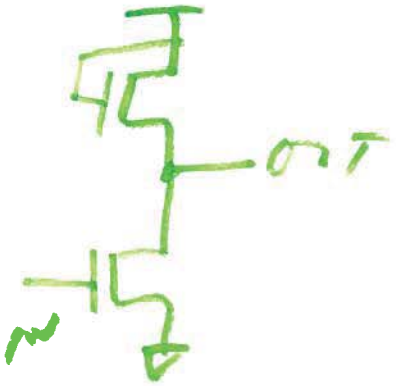


0.7RC



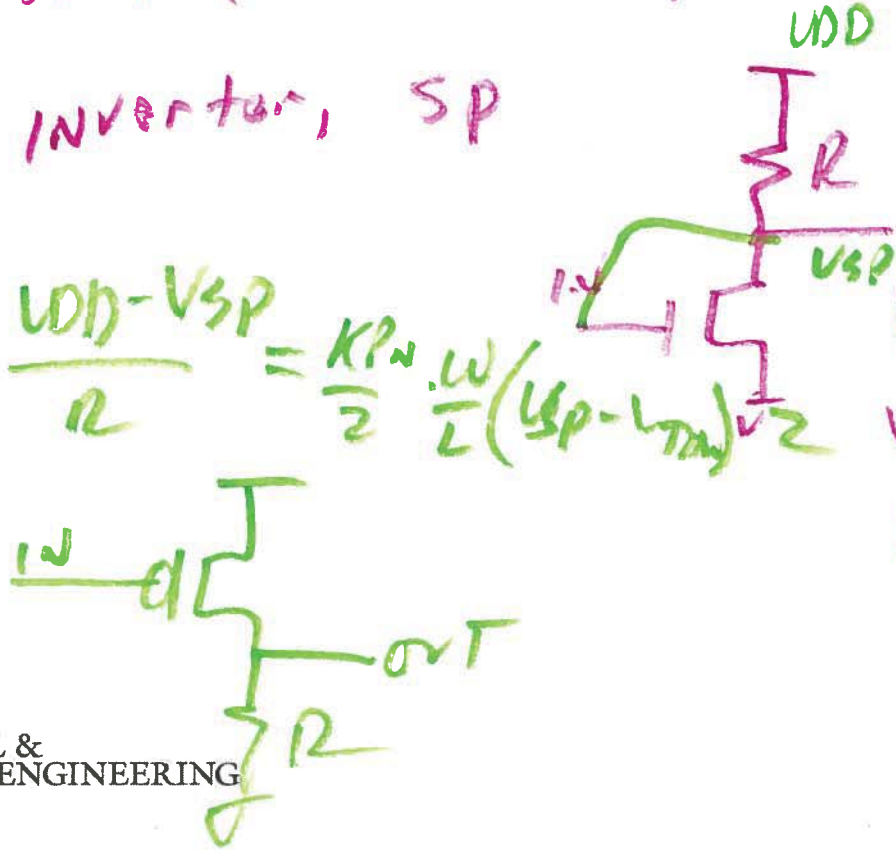
3) Gate delays

inverters
NAND gates
NOR gates
TGs



4) setup & hold times, clocked circuits

5) Inverter, SP

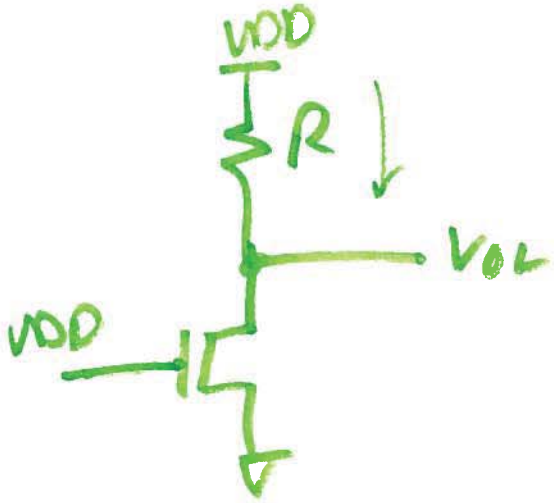


$$\frac{VDD - VSP}{R} = \frac{K'_n}{2}\frac{W}{L}(VSP - V_{TN})^2$$

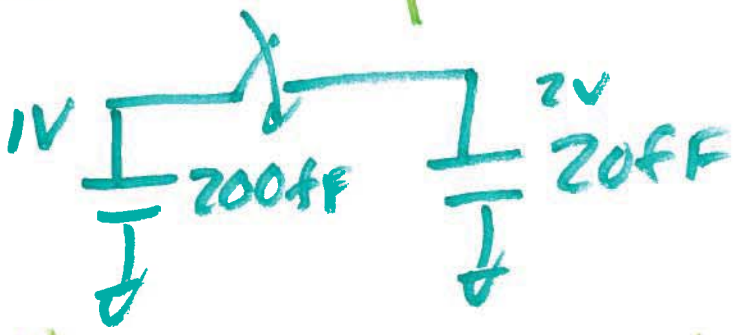
$V_{SP} = ?$

$V_{OL} = ?$

$V_{out} = ?$



$$\frac{VDD - V_{OL}}{R} = K_P \cdot \frac{W}{L}\left((VDD - V_{THN})V_{OL} - \frac{V_{OL}^2}{2}\right.$$



MOSFET operation

Derivation of equations

Body effect

Channel length modulation

ON/off currents

Quizzes

H.W.

Layouts → wide MOSFETS

Long MOSFETS

Depletion C reverse recovery time

Storage C