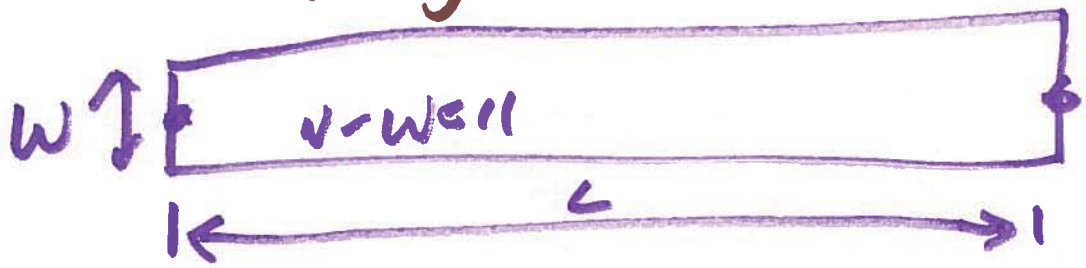
EE 421 / ECG 621

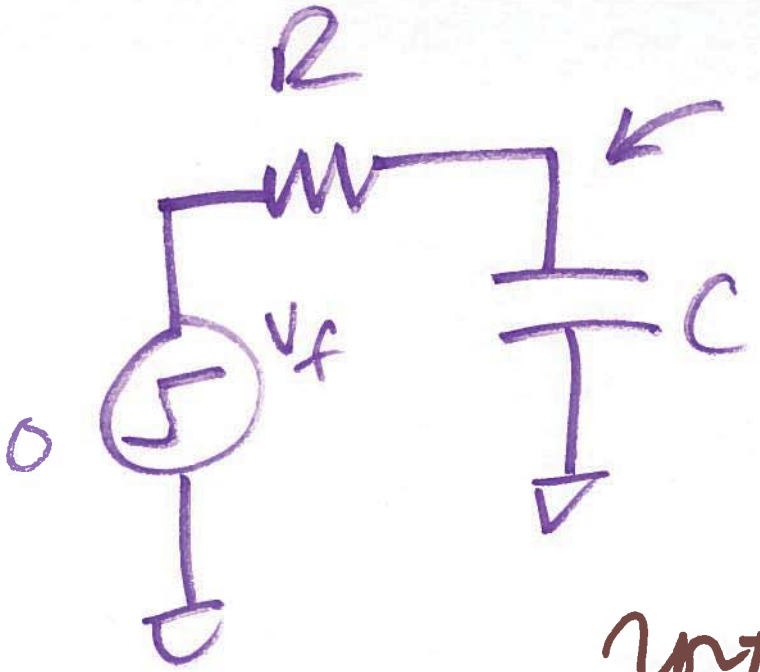
Lecture 3

Sept. 6, 2017

Digital IC Design



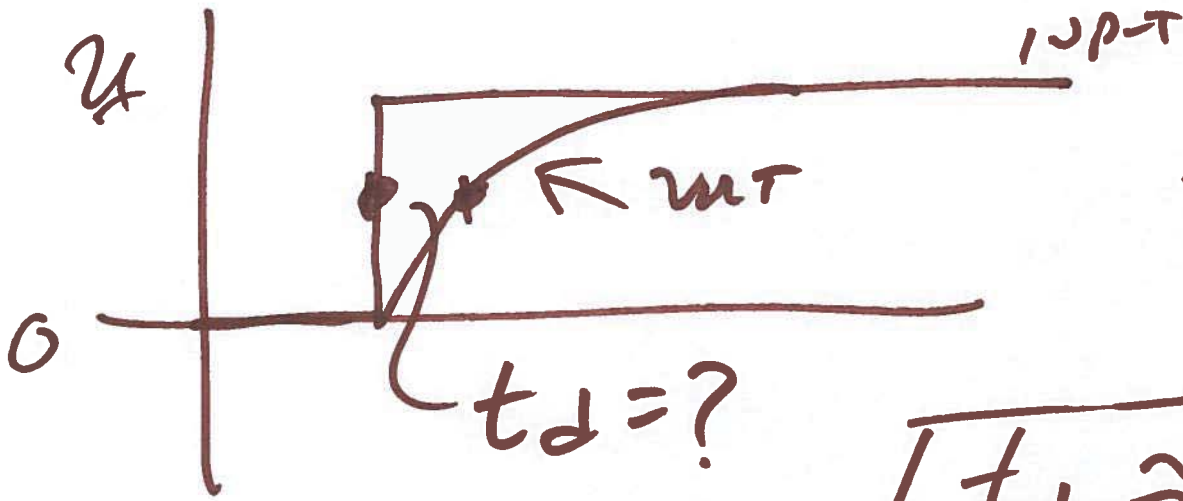
$$R = R_{\square} \cdot \frac{L}{W}$$



$$v_{out} = v_f \pm (v_i + v_f)\, e^{-t/RC}$$

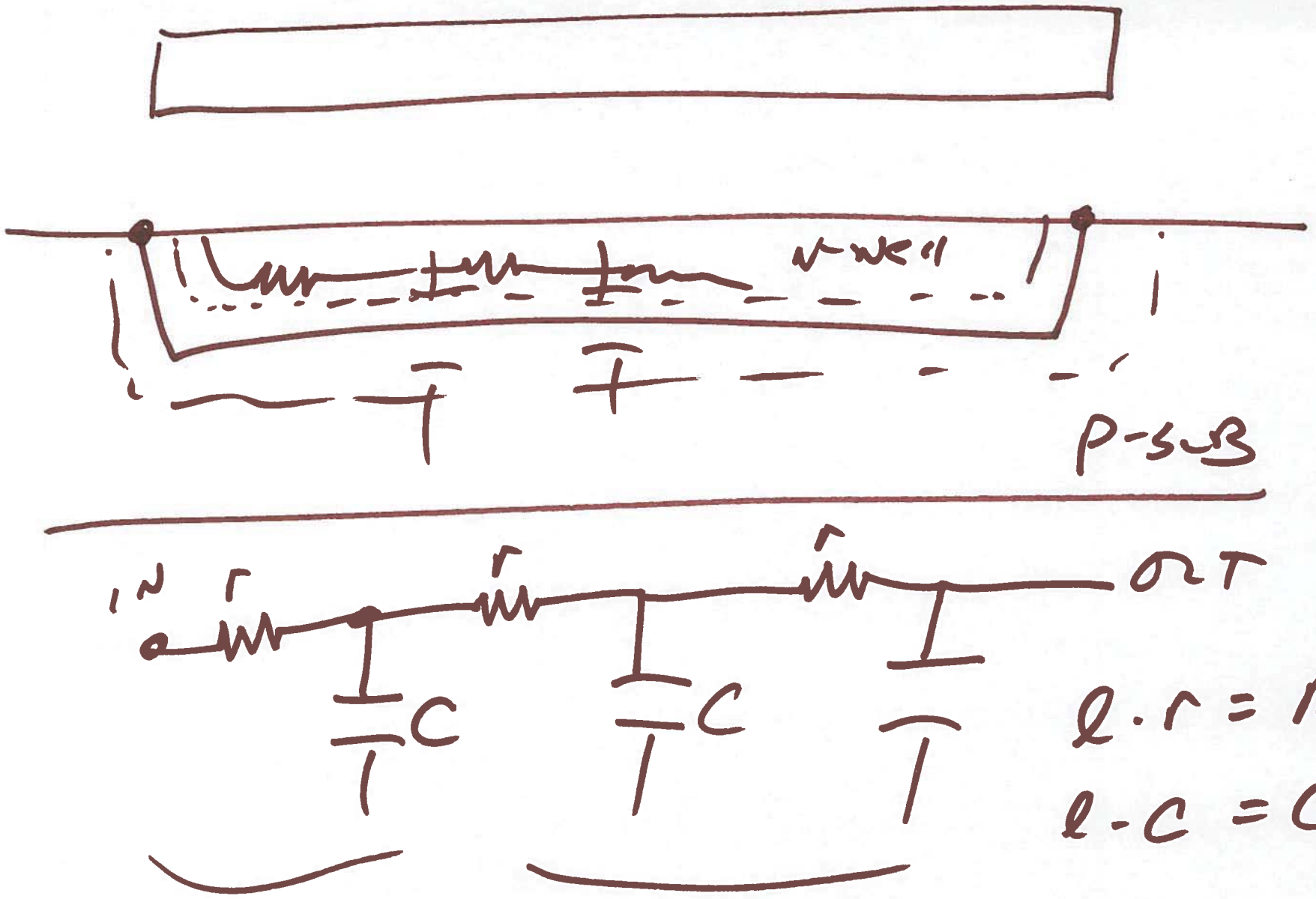
$$= v_f(1 - e^{-t/RC})$$

$$v_{out} \rightarrow \frac{v_f}{2}$$



$$\frac{v_f}{2} = v_f(1 - e^{-t_d/RC})$$

$$\boxed{t_d \simeq RC \cdot 0.7}$$



$\ell \cdot r = R_{TOT}$

$\ell \cdot C = C_{TOT}$

ℓ = sections

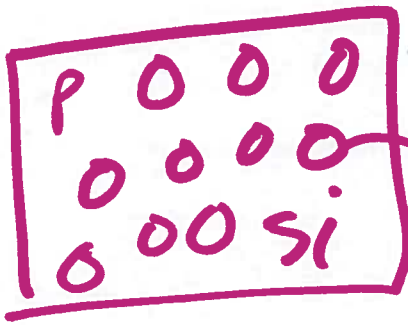
$t_d = 0.7rC + 0.7 \cdot 2rC + 0.7 \cdot 3 \cdot rC + \cdots + 0.7\ell \cdot rC$

Delay through distributed RC

$$t_d = 0.7rc\,\underbrace{(1+2+3+\cdots+\ell)}_{\frac{\ell(\ell+1)}{2}}$$

$$t_d = \frac{0.7}{2} \cdot r \cdot c \cdot \ell(\ell+1)$$

$$\boxed{t_d \simeq 0.35 \cdot r \cdot c \cdot \ell^2}$$



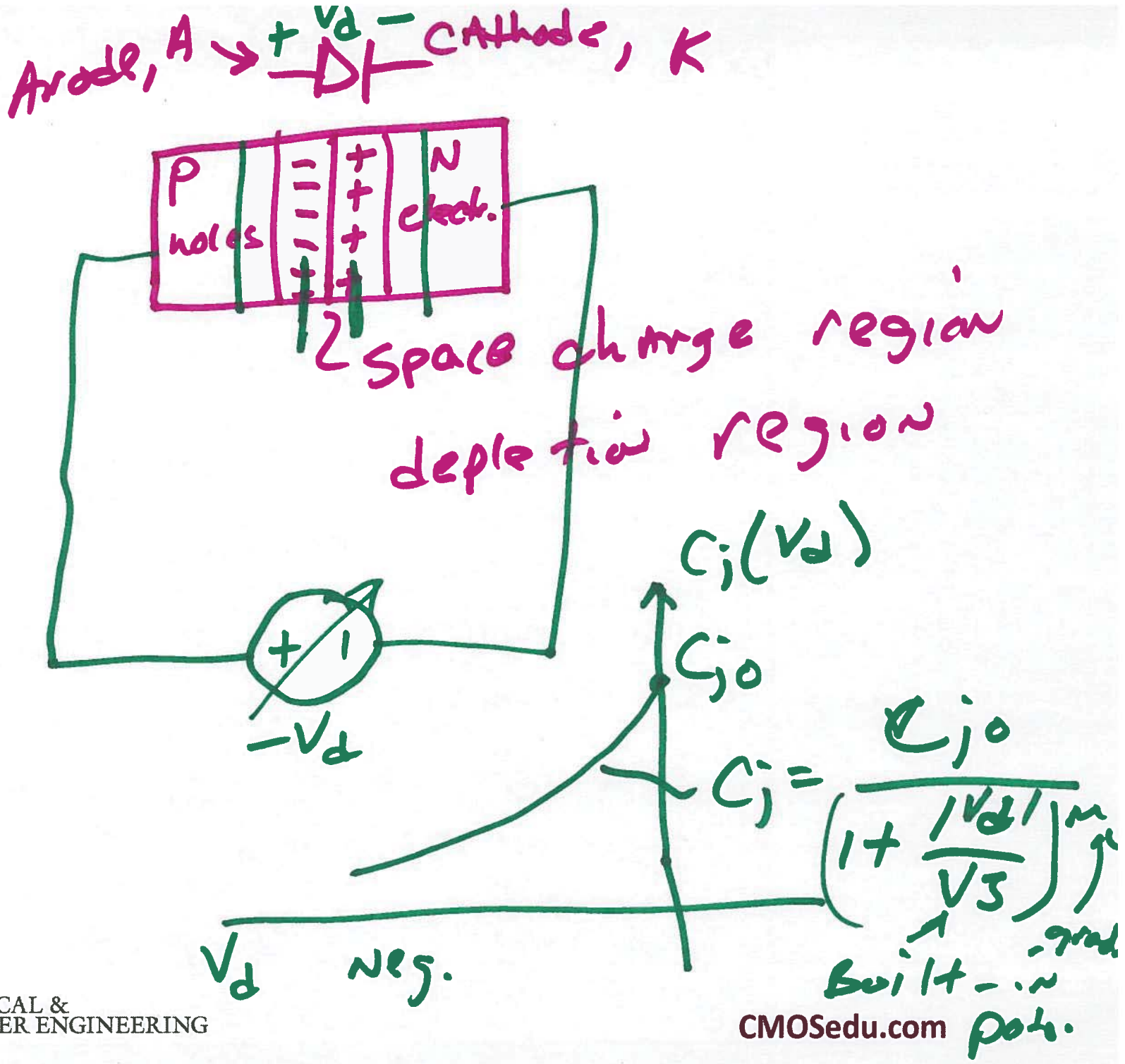
Valence - 4 in Si

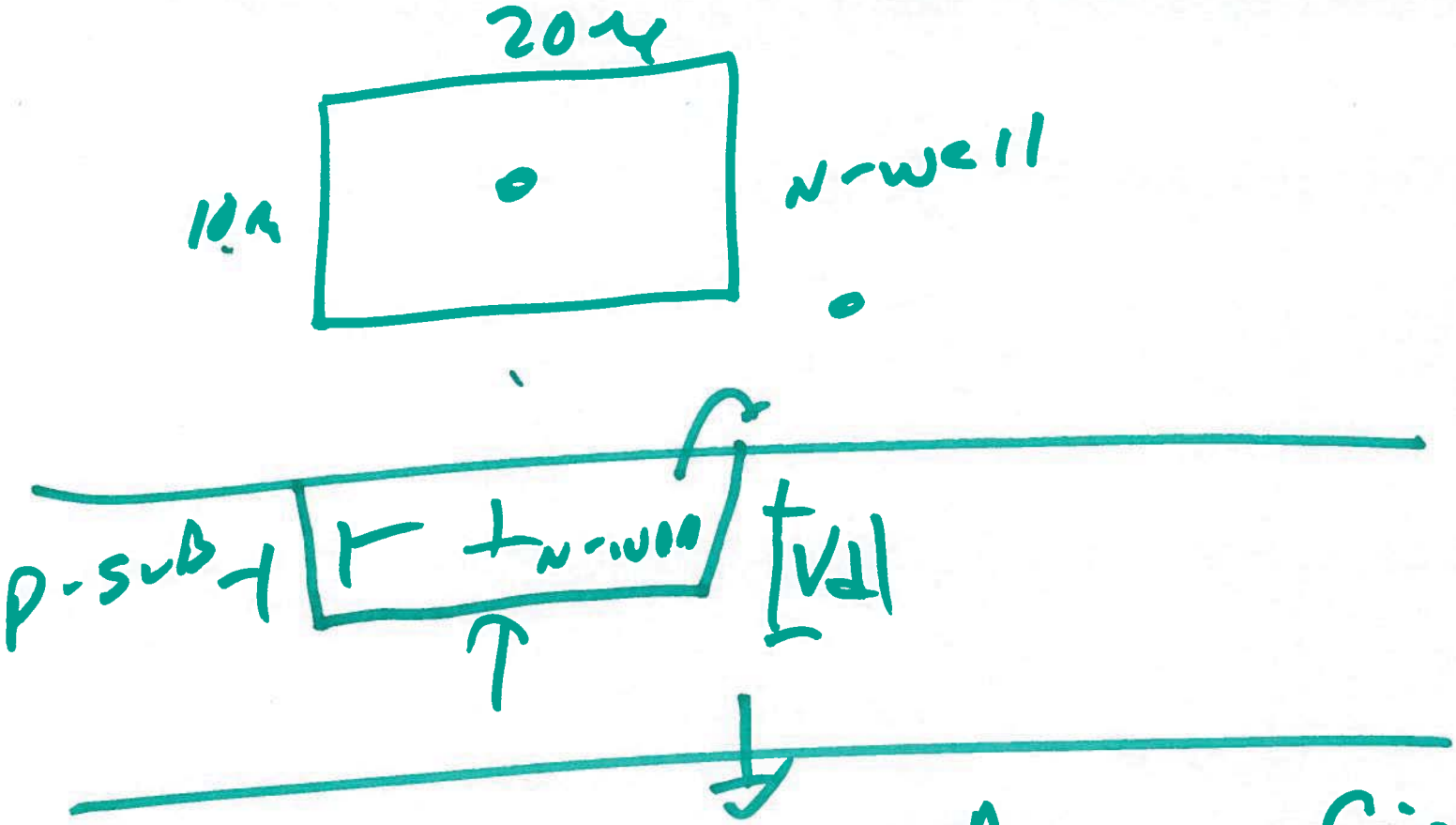
add Boron → Valence = 3

$N_{Si} \simeq 10^{22}$ Atom/cm^3

$N_{A|_{Boron}} = 10^{16}$

5)

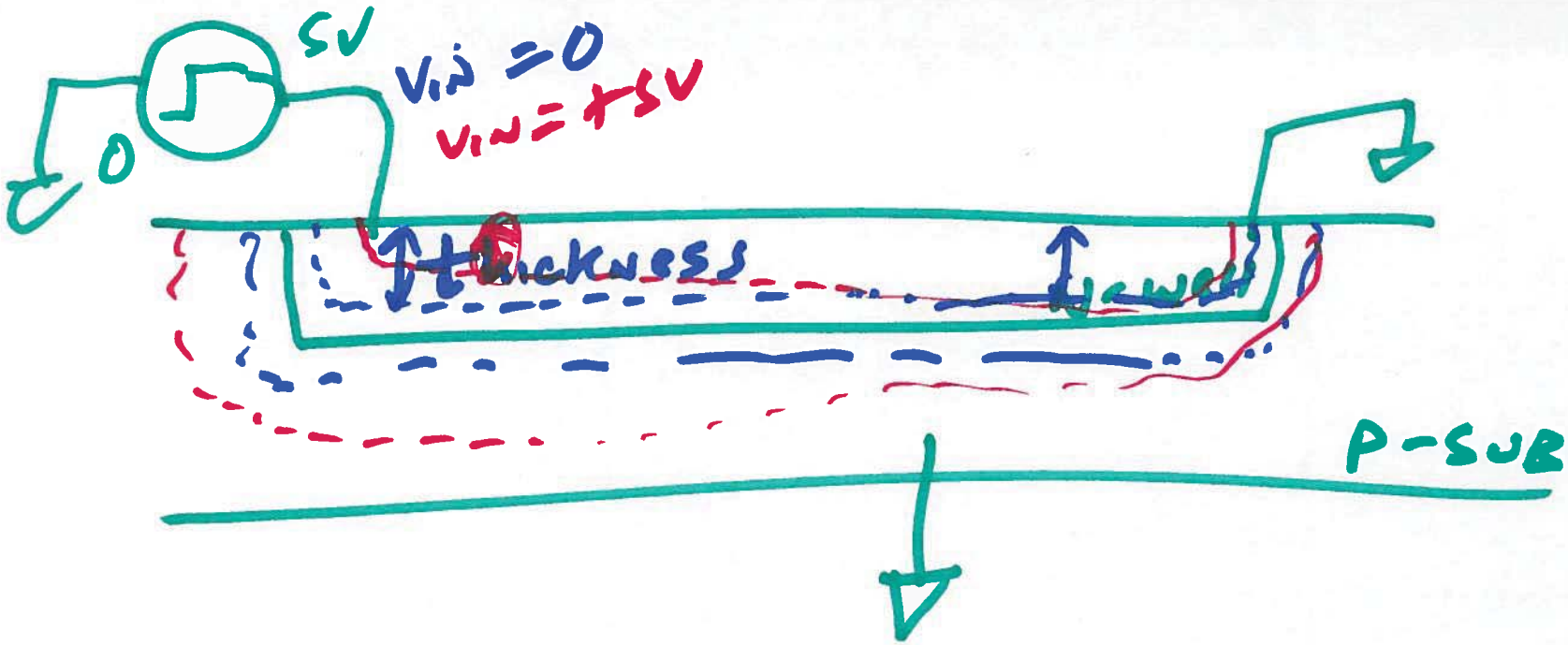

Anode, A
+ v_d −
Cathode, K
P
holes
N
elect.
2
space charge region
depletion region
+
1
$-V_d$
$C_j(V_d)$
C_{j0}
$C_j = \frac{C_{j0}}{\left(1 + \frac{|V_d|}{V_3}\right)^m}$
V_d neg.
Built-in pot.



$$\text{CAP between n well p sub} = \frac{C_{jon} \cdot A}{\left(1 + \frac{V_d}{pbd}\right)^{MJ}} + \frac{C_{jsw} \cdot P}{\left(1 + \frac{V_d}{pbsw}\right)^{MJSW}}$$

built-in pot

grading


5V
0
$V_{in} = 0$
$V_{in} = +5V$
thickness
P-SUB