

EE 421 / ECG 621

Digital IC Design

$t_d =$

0.35 · 100k · 60fF Lecture 4

$t_d = 2.1 \mu s$ Sept. 11, 2017 $t_d = 0.35 r_{eq}^2$

plate cap 100 aF / μm^2 $r_{eq} = \text{tot. Res.}$
sidewall 50 aF / μm $C_{eq} = \text{tot. Cap}$

$$C_{TOT} = C_{side} \quad 24 \times 200 \mu m$$

$$+ (plate \ R = 1k \cdot \frac{200}{2} = 100k \Omega)$$

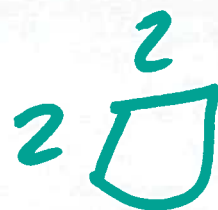
$$C_{sidewall} = 404 \mu m \cdot \frac{50 \text{ aF}}{\mu m}$$

$$C_{plate} = \frac{100 \text{ aF}}{\mu m^2} \cdot 24 \cdot 200 \mu m$$

$$R = 100k$$

$$l = 100\mu$$

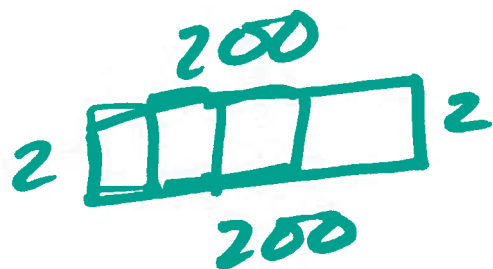
$$r = 1k$$



$$C = \frac{100f}{\cancel{2\mu m^2}}$$

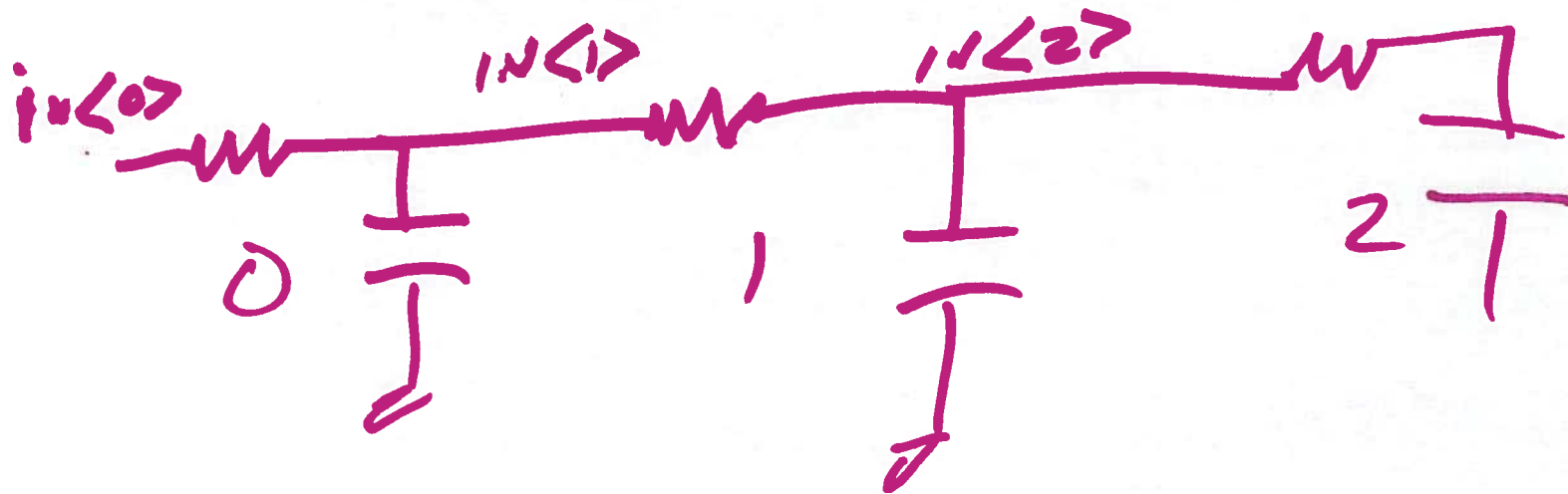
$$\frac{400\cancel{\mu m^2}}{2} = 40,000af$$
$$40fF$$

$$\frac{50af}{\cancel{2\mu m}} \cdot 40\cancel{\mu m} = 20,020af$$
$$20fF$$

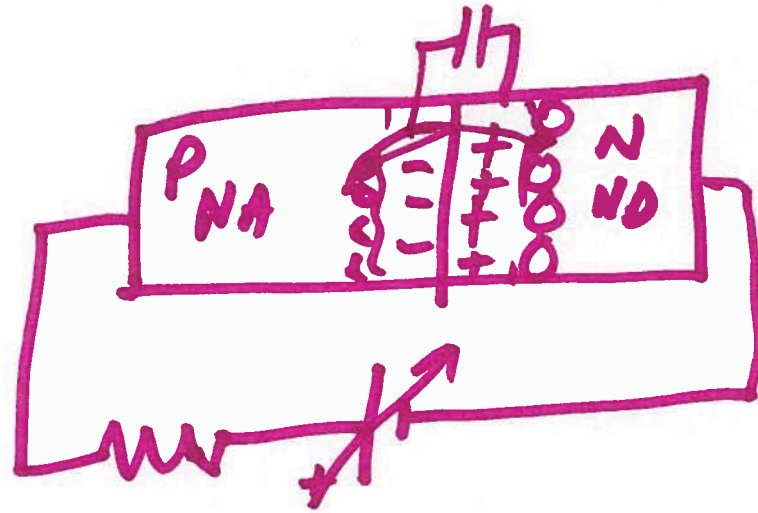


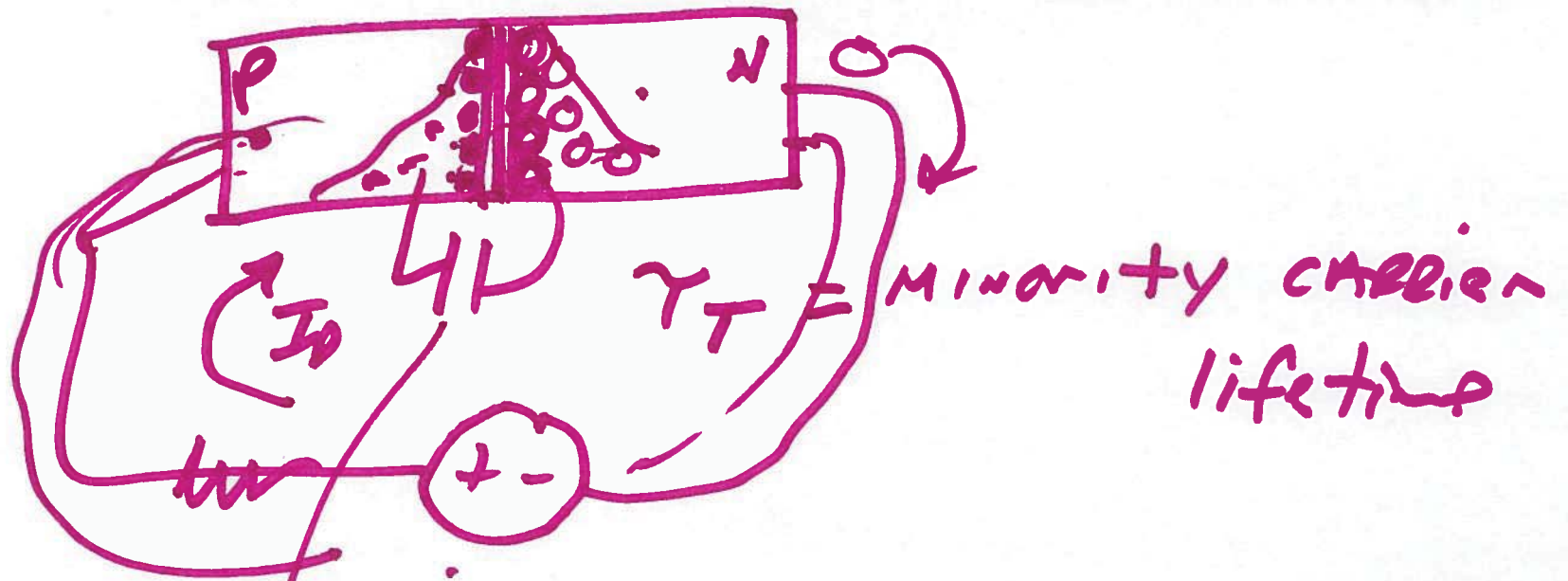
$$C_{TOT} = \underline{\underline{60fF}}$$

$$C = \frac{60fF}{100} = \underline{\underline{0.6fF/\square}}$$



diffusion capacitance storage CAP.





$$C_{diff} = \tau_T \cdot \frac{I_D}{V_T}$$

$V_T \cdot n \rightarrow \text{emission}$

$\downarrow \quad \quad \quad \approx 1$

thermal

voltage

$$\frac{kT}{q} \Rightarrow 26 \text{ mV}$$

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