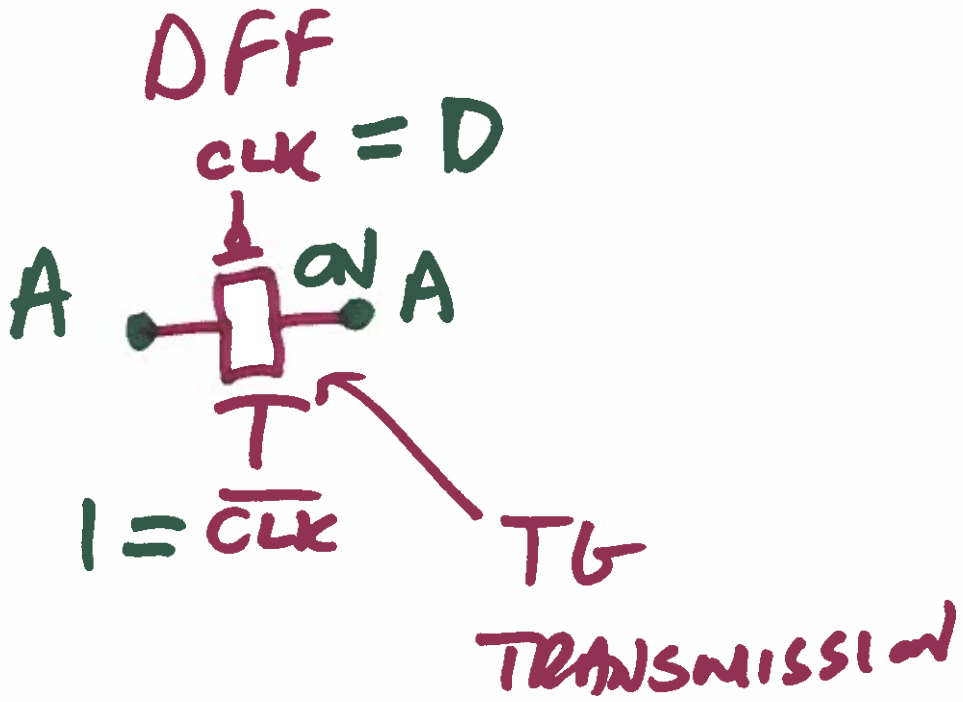
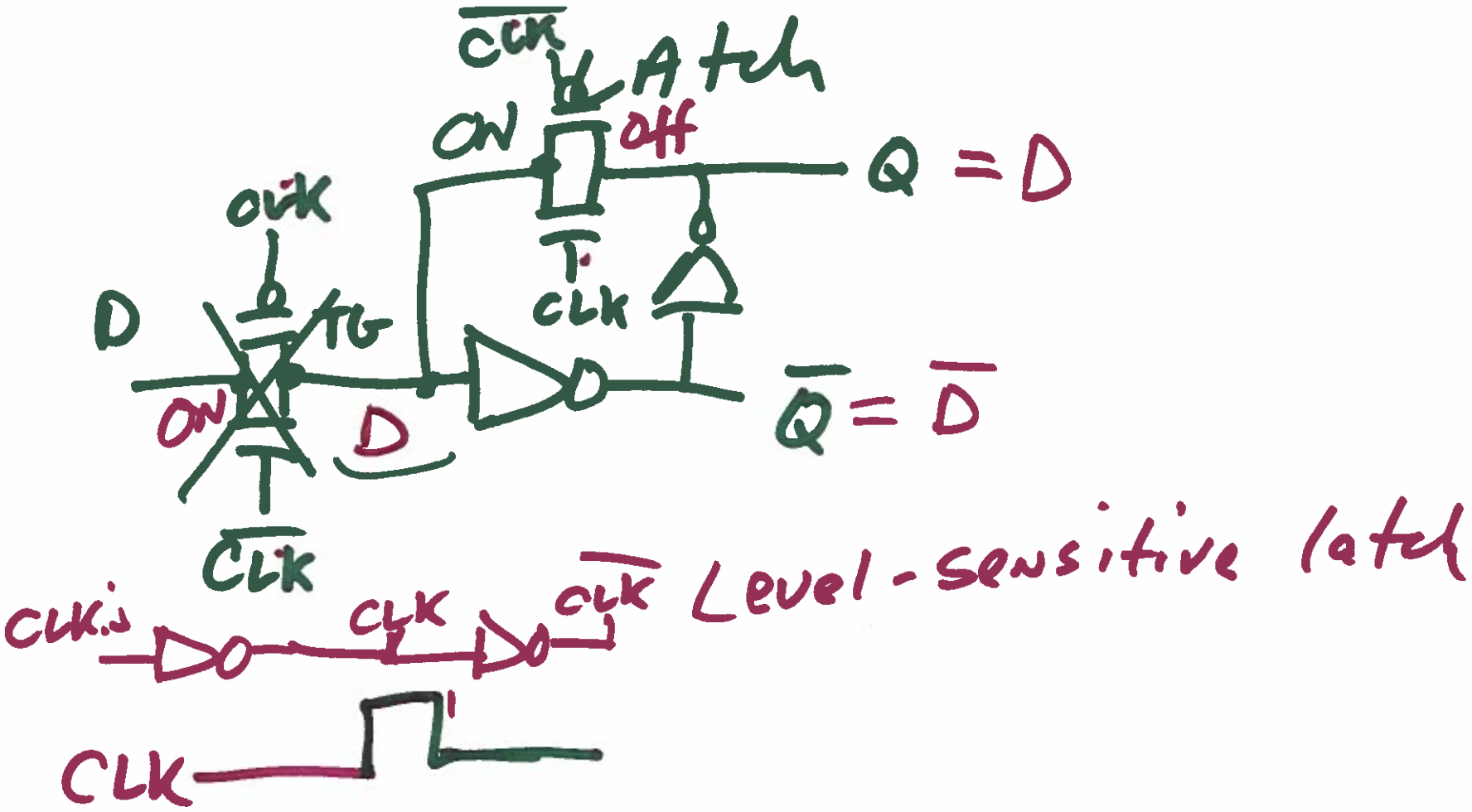
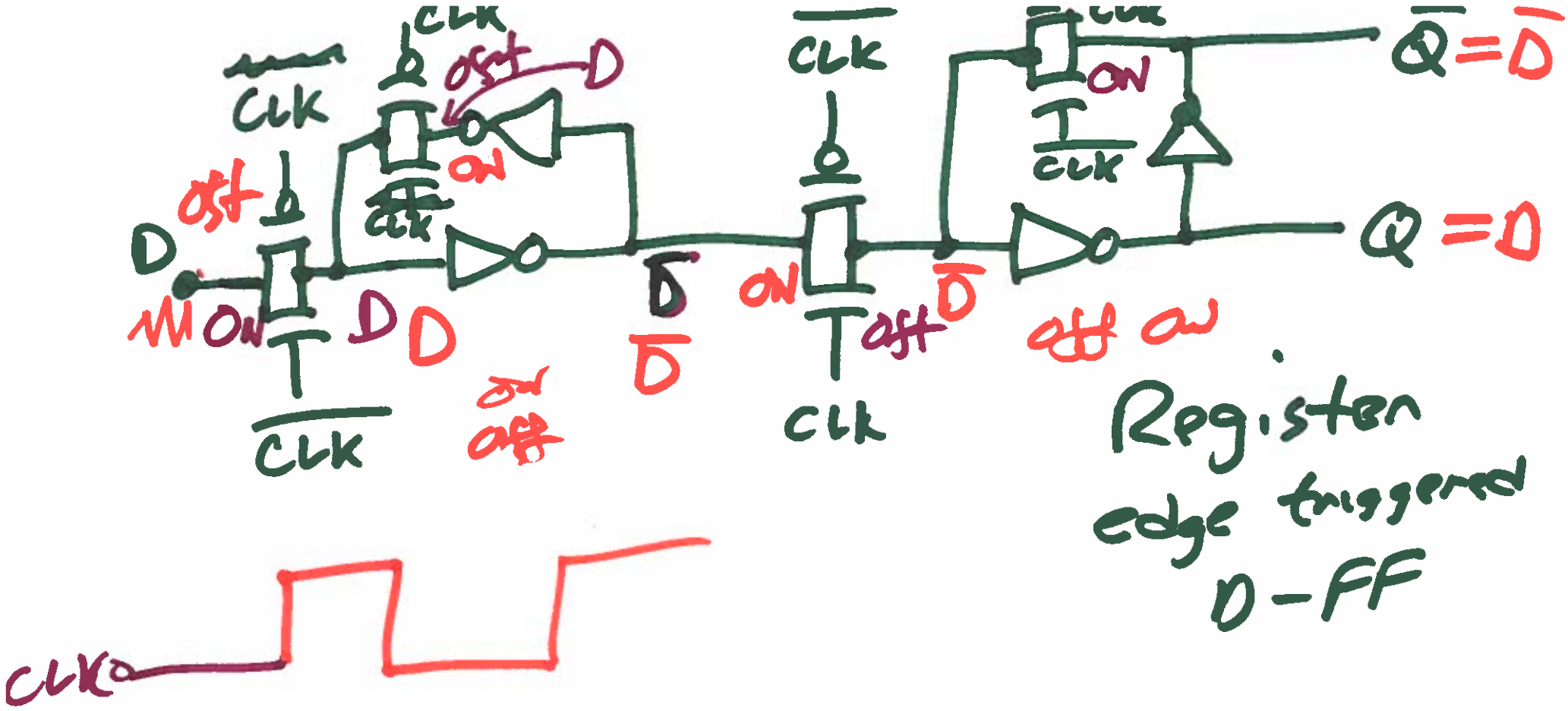
EE 421 / EGG 621
Digital IC Design

NOV. 13, 2019

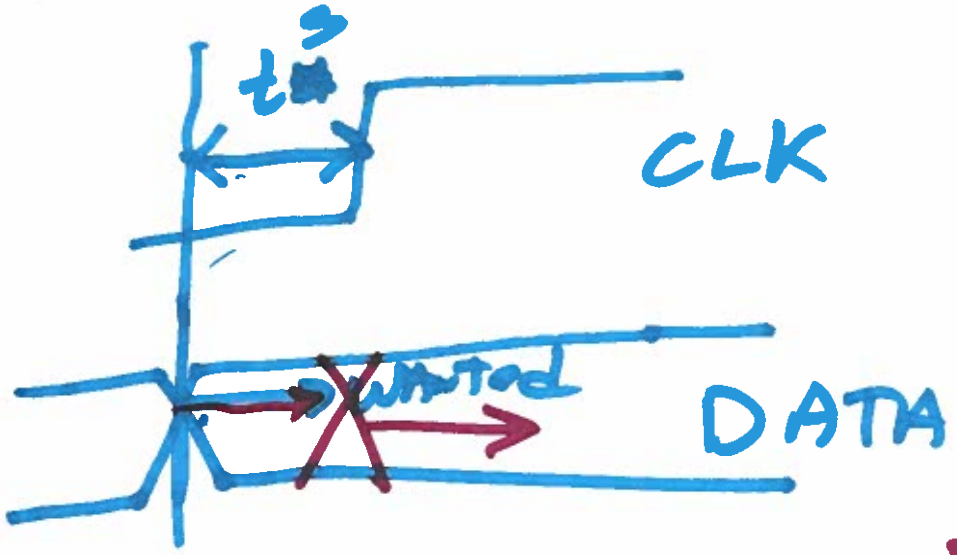
Lecture 21

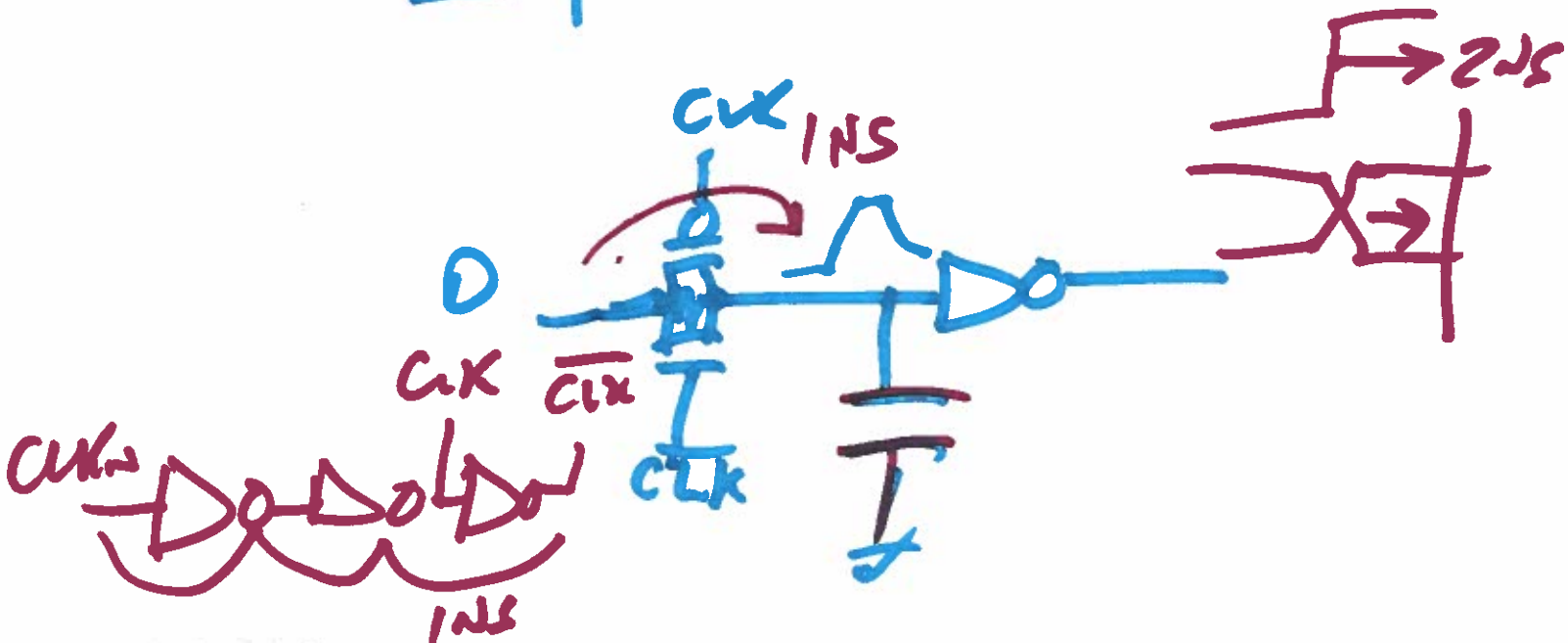


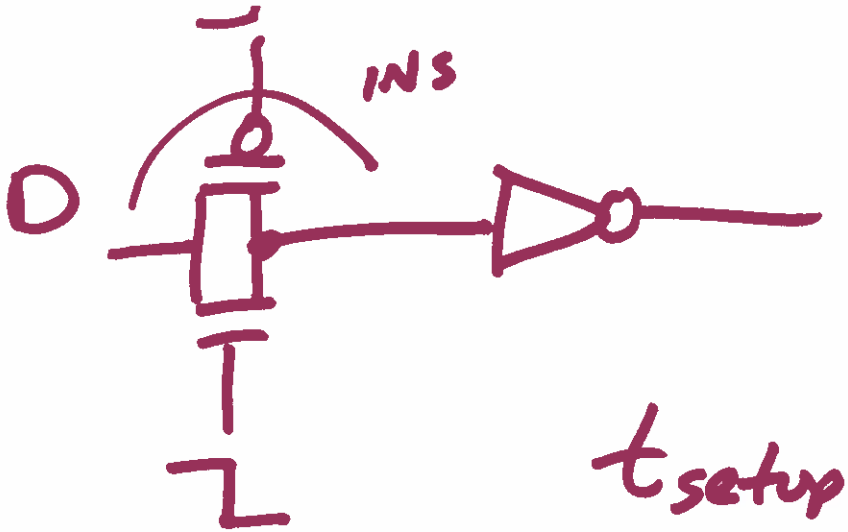

CLK
Latch
ON
off
Q = D
CLK
D
TG
CLK
ON
D
$\overline{Q} = \overline{D}$
CLK
Level-sensitive latch
CLK
CLK
CLK
CLK


CLK
D
ON
OFF
Q=D
Q=D
Register
edge triggered
D-FF
CLK

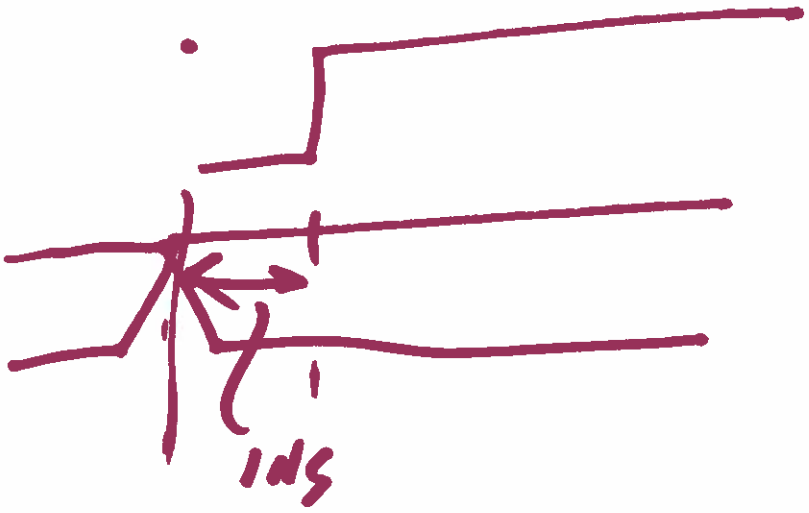
setup time

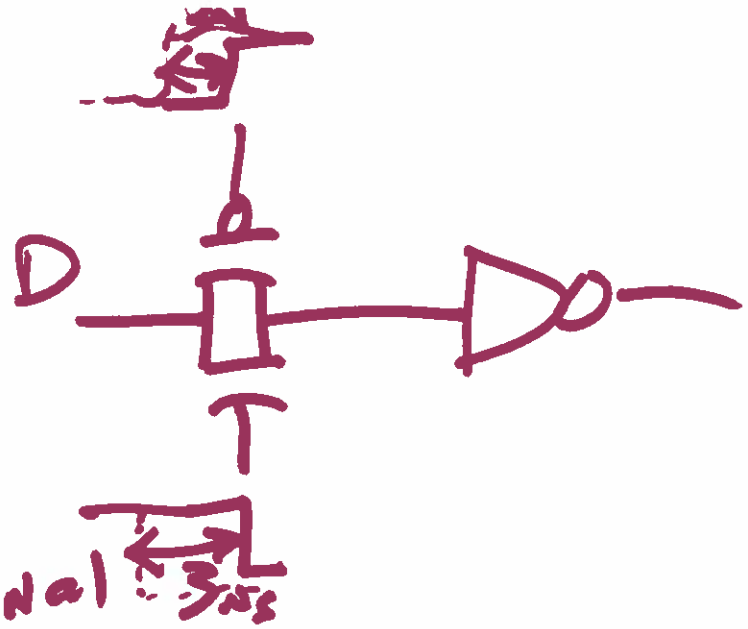




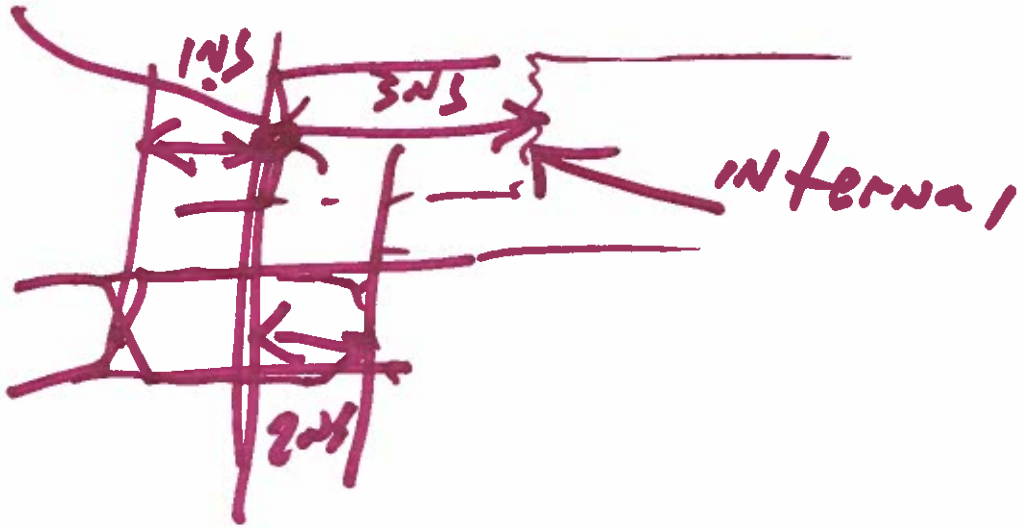


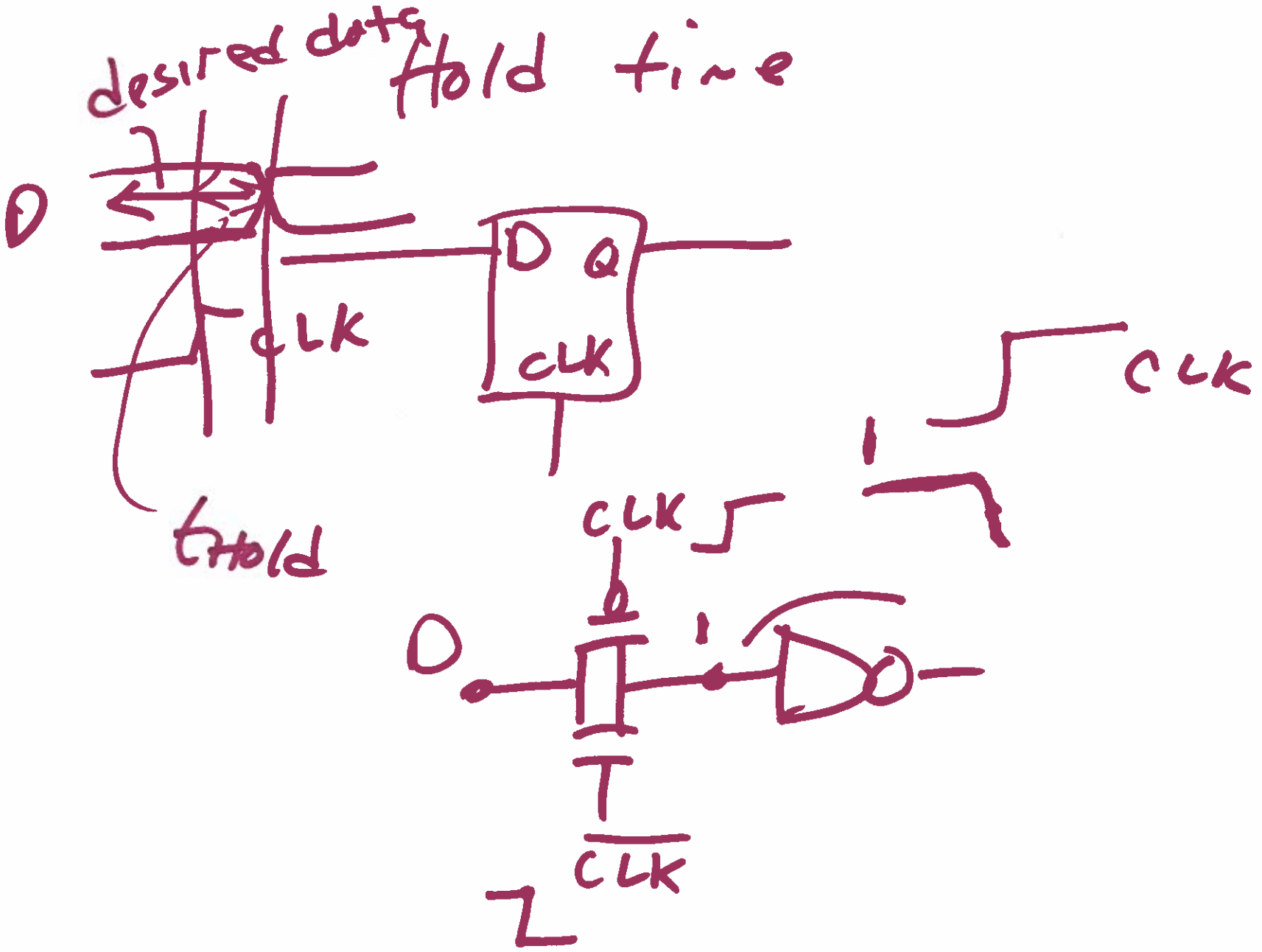
$t_{setup} = 1ns$



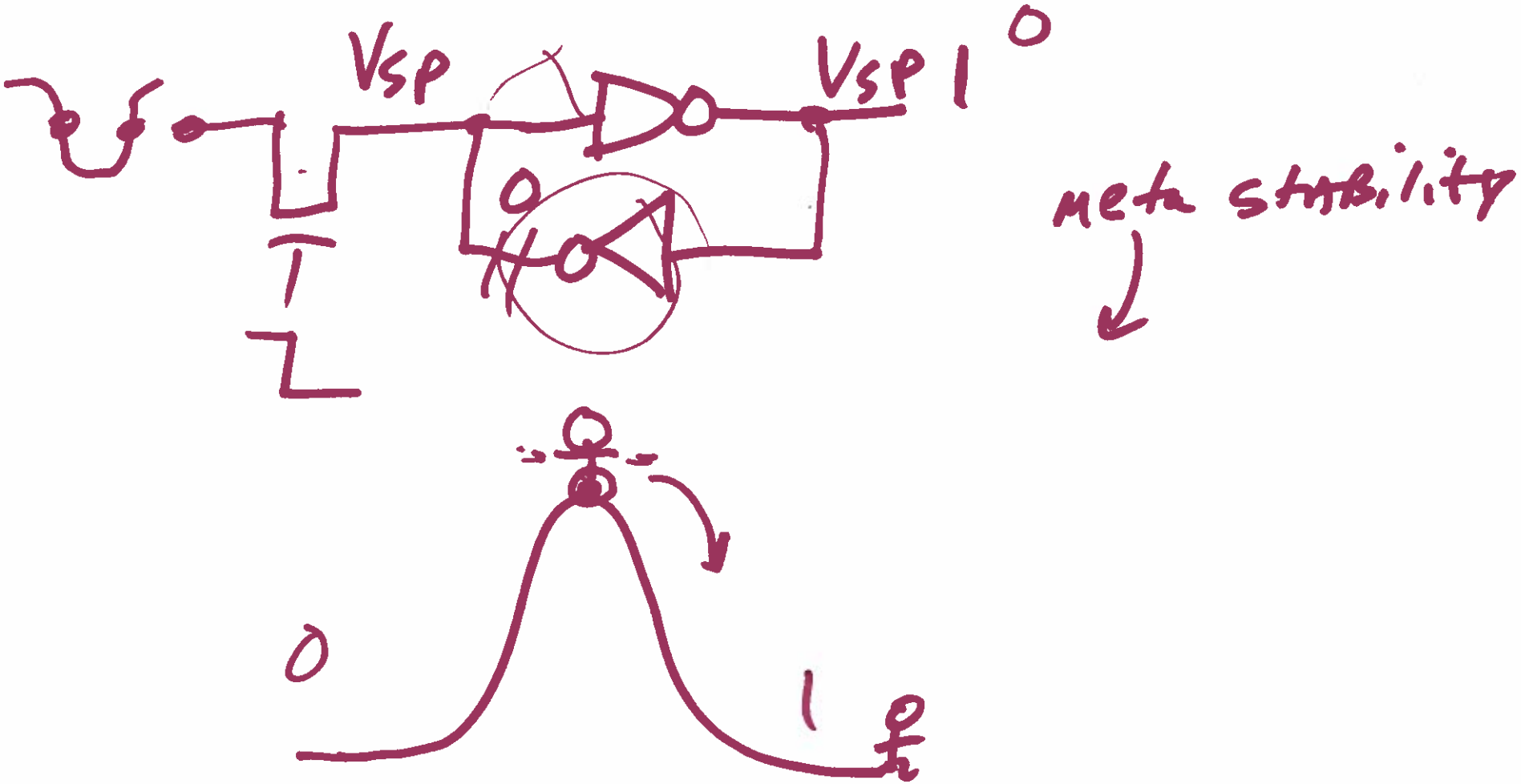


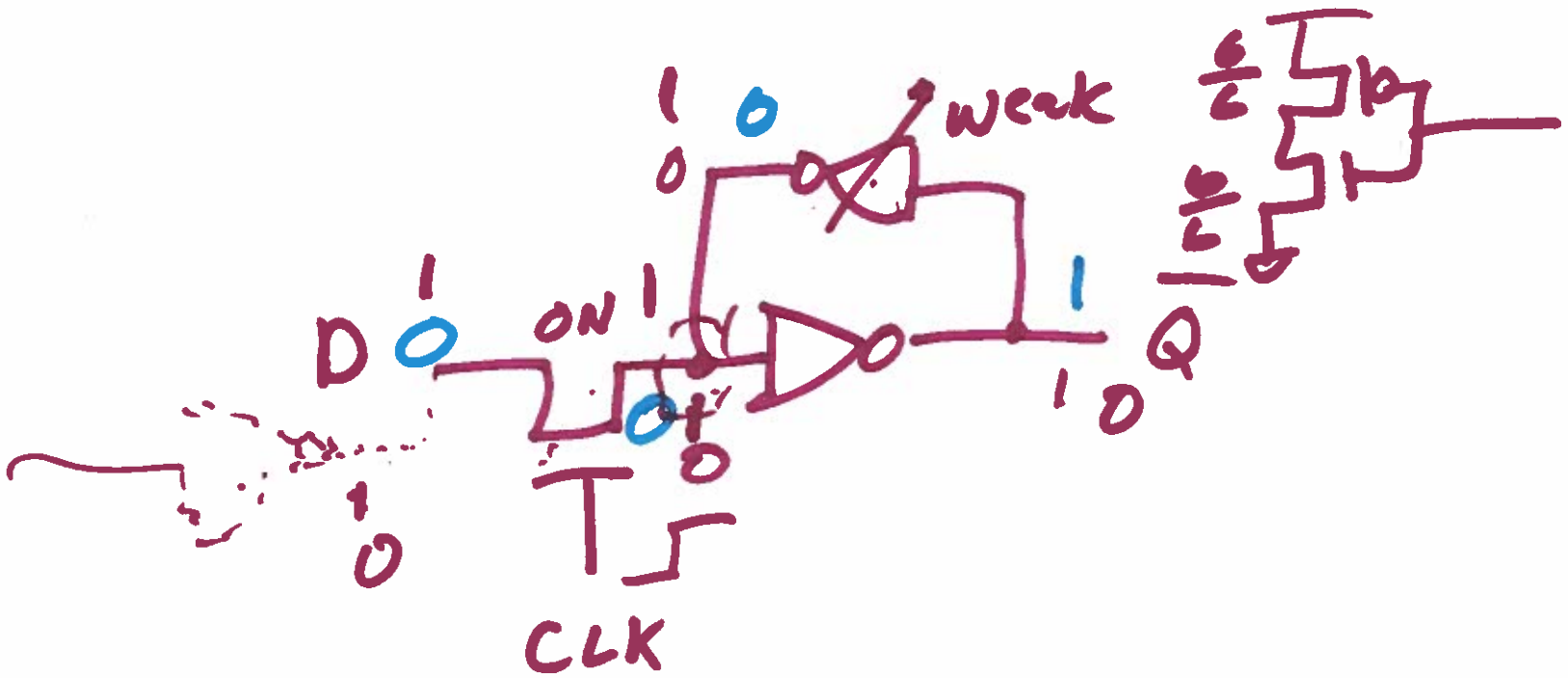
$t_{setup} = -2ns$




desired data
Hold time
D
CLK
D Q
CLK
t_{Hold}
CLK
CLK
D
T
$\overline{CLK}$

Latch




1
0
weak
D
1
0
ON
1
1
0
Q
1
0
1
0
CLK