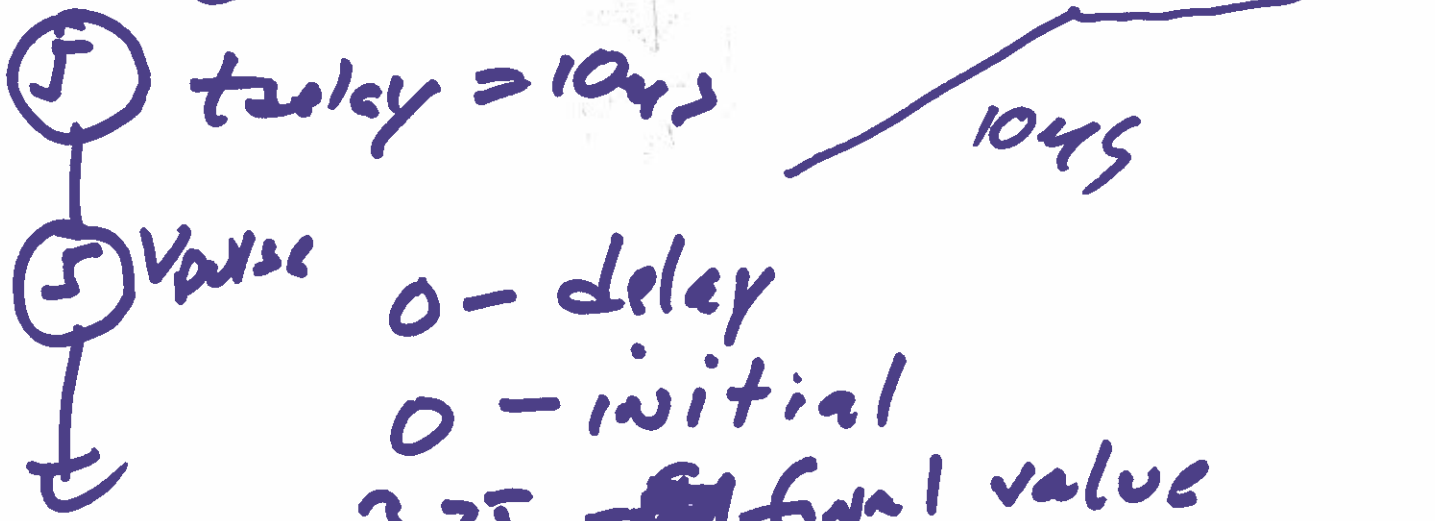
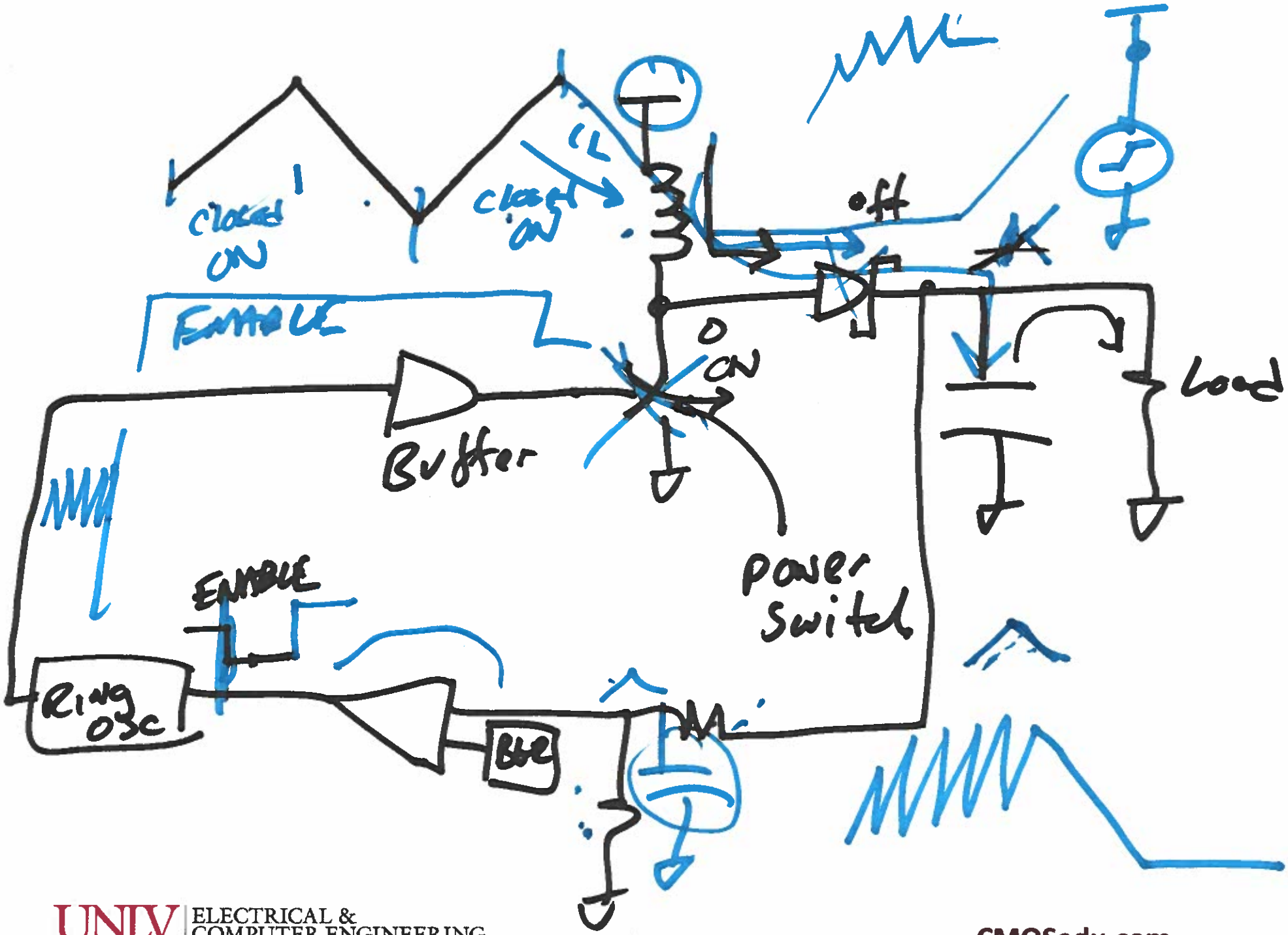
EE421/ECG621
Digital IC Design
November 18, 2019
Lecture 22

0 → 1.75

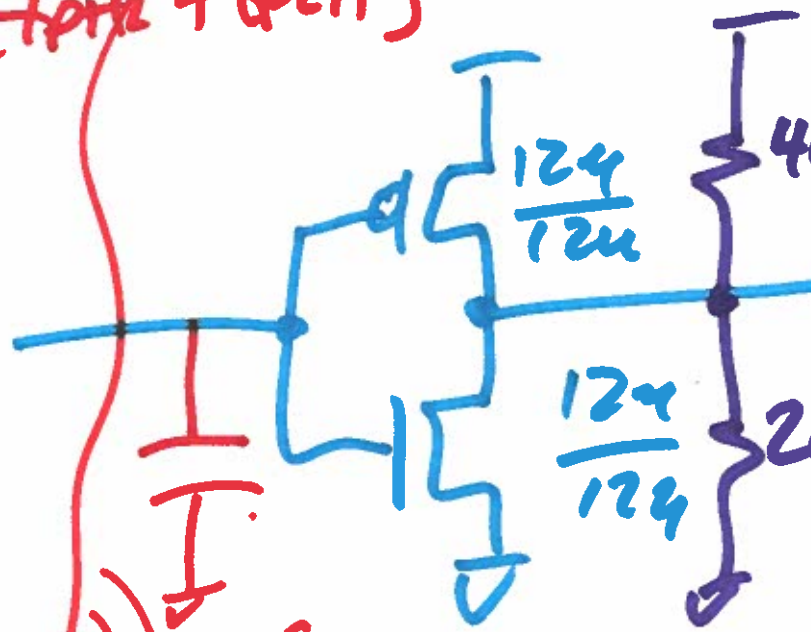



clocked ON
clock ON
ENABLE
off
ON
Buffer
Load
power switch
ENABLE
Ring Osc

Long L

Why?

$$f_{OSC} = \frac{1}{N(t_{pHL} + t_{pLH})}$$



$C_{OUT} + \frac{3}{2}C_{OUT} = \frac{5}{2}C_{OUT}$

$C_{OUT} = 2.5(12.12 + 12.12)$

$\frac{3}{2}(2.5fF/\square)(12.12 + 12.12) = C_{INV}$

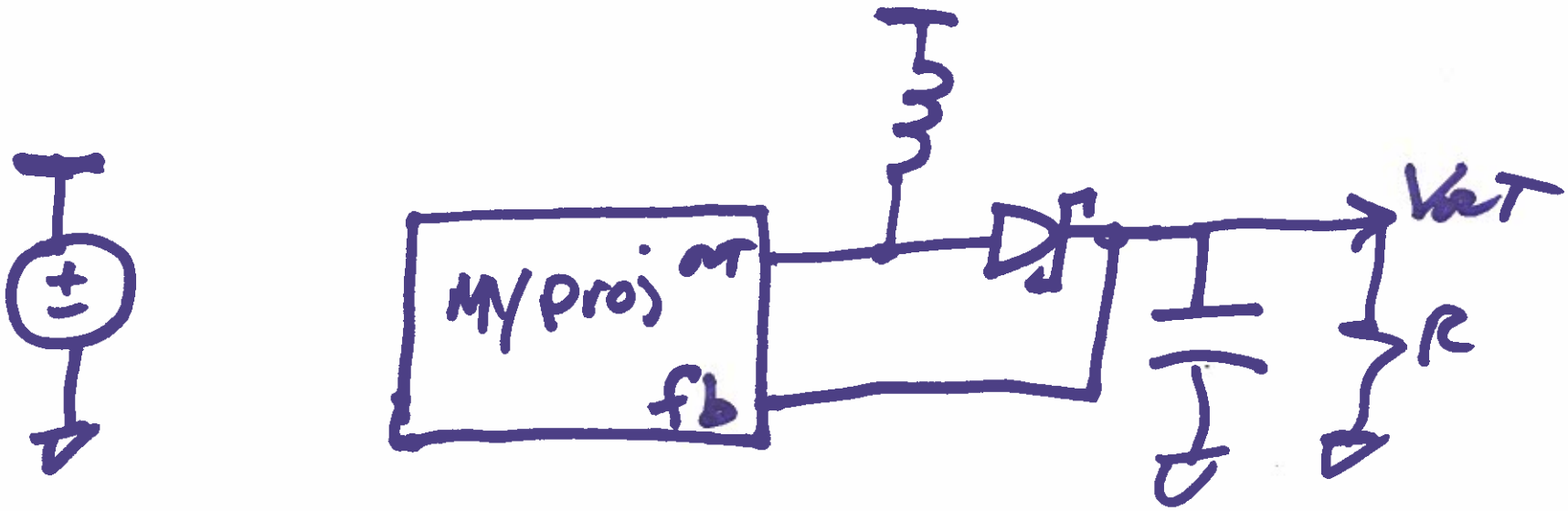
$\frac{2}{3}C_{IN}$

$\frac{3}{2}C_{OUT} = C_{IN}$

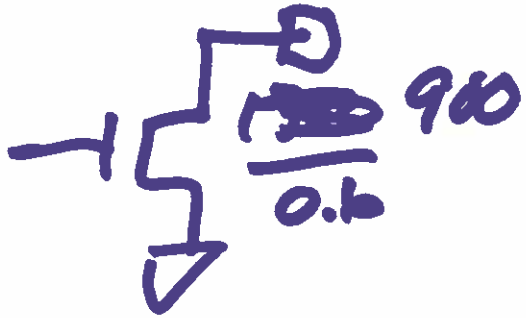
$C_{TOT} = \frac{5}{2} \cdot 2.5 \cdot 2 \cdot (12.12)$

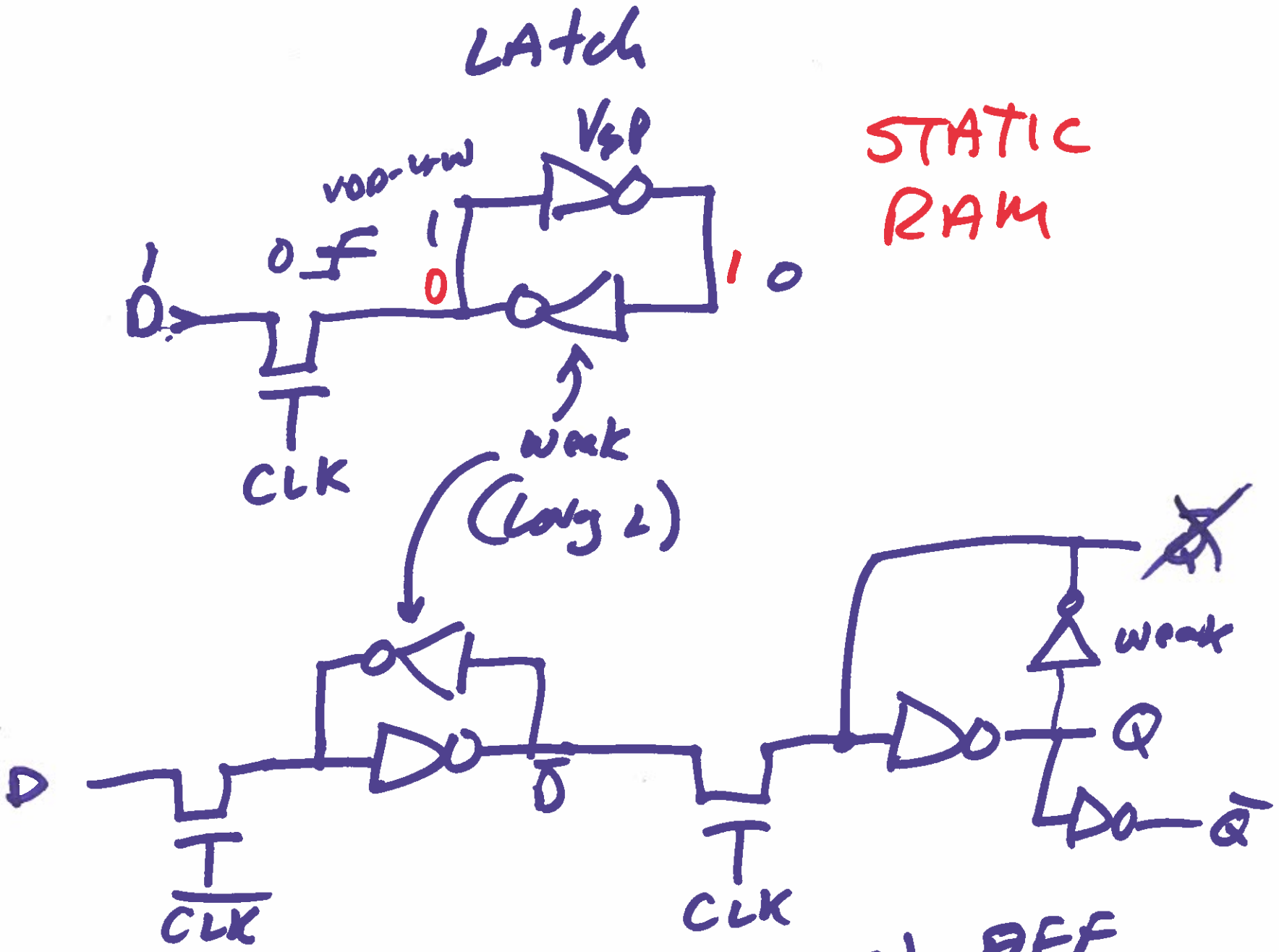
$t_{pHL} = 0.7 \cdot 20K \cdot C_{TOT}$

$t_{pLH} = 0.7\,40K \cdot C_{TOT}$ $2 \cdot t_{pHL}$



POWER MANAGEMENT IC




Latch
STATIC
RAM
VDD-Vtn
Vtp
1
0
1
0
1
0
D
CLK
Weak
(Long L)
D
CLK
CLK
Weak
Q
Q̄
Edge triggered DFF