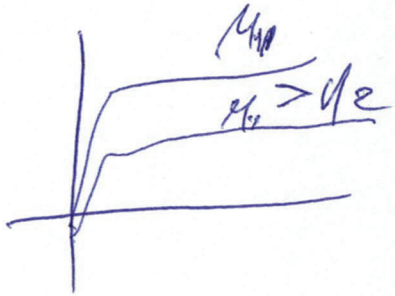
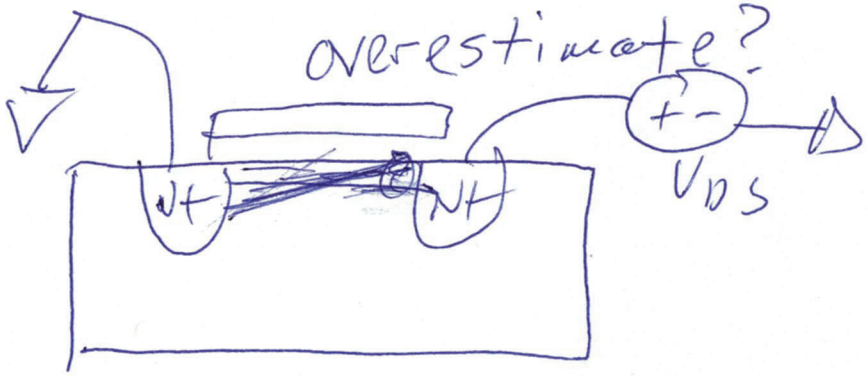
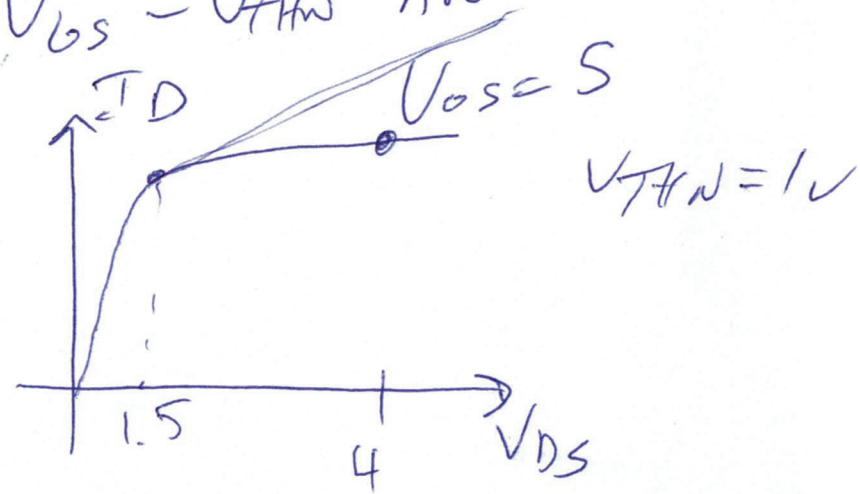
EE 421/ECG 621
Digital IC Design
Lecture 13



OCT. 7, 2020

Why is $V_{DS,SAT} = V_{GS} - V_{THN}$ AN overestimate?

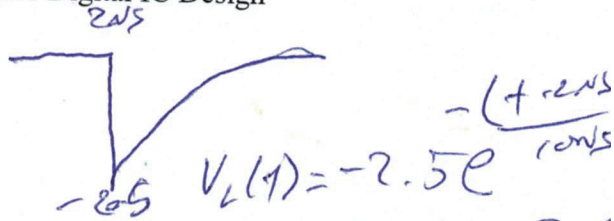




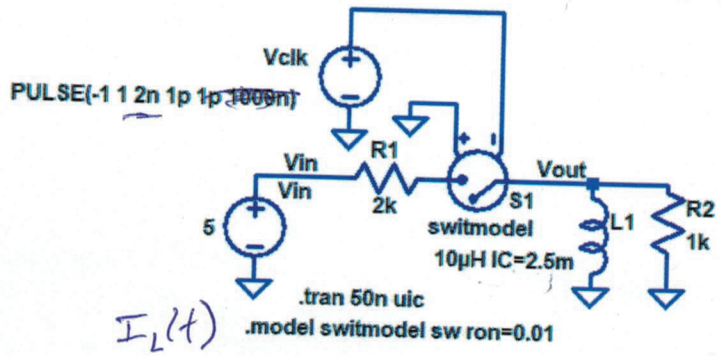
Practice Midterm Exam – EE 421 Digital Electronics and ECG 621 Digital IC Design
Fall – University of Nevada, Las Vegas

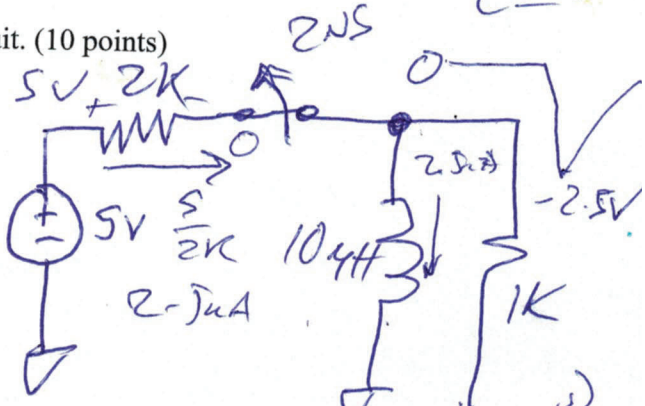
NAME: _____

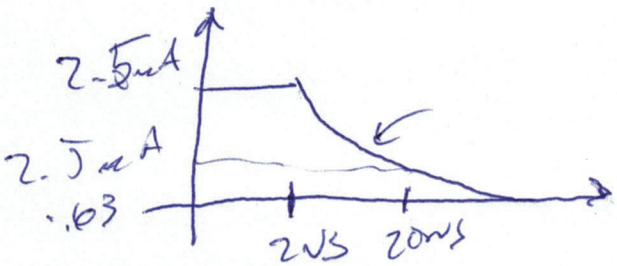
Open book, closed notes.
Show your work for credit. When possible place boxes around your answers.



1. Plot the current through the inductor in the following circuit. (10 points)







$\tau = \frac{L}{R} = \frac{10\mu}{1K} = 10NS$

$I_L(t) = 2.5mA\, e^{-(t-2NS)/10NS}$

$t \geq 2NS$

2. What key binding is used to descend and edit a cell in Cadence? (5 points)

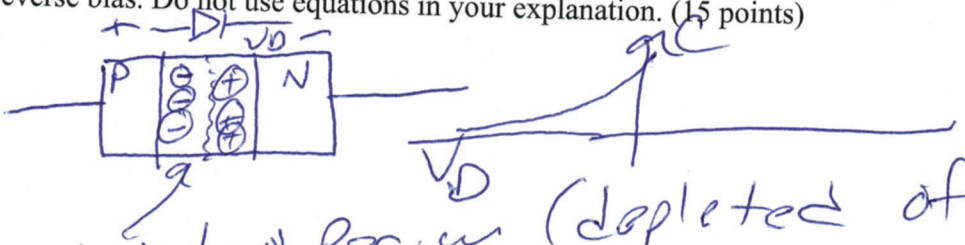
shift - X

3. Estimate the delay through an n-well resistor having a sheet resistance of 1kohm/square and a zero-bias depletion capacitance of 100 fF/um^2. Assume the resistor is 100 um long and 2 um wide. (5 points)

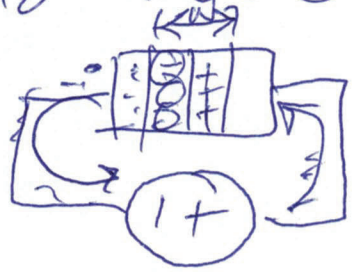
$t_d = 0.35 \cdot \underbrace{1K \cdot \frac{100}{2}}_{R_{TOT}} \cdot \underbrace{\frac{100fF}{um^2} \cdot (100um \times 2um)}_{C_{TOT}}$

2)

4. Explain **in your own words** why depletion capacitance of a pn junction decreases with increasing reverse bias. Use a cross-sectional view of a pn junction showing the depletion region's width in your explanation. Also show a plot of the depletion capacitance against reverse bias. Do not use equations in your explanation. (15 points)



depletion Region (depleted of free carriers. holes move to N leaving behind ⊖ charge causing N-side to have ⊕ charge

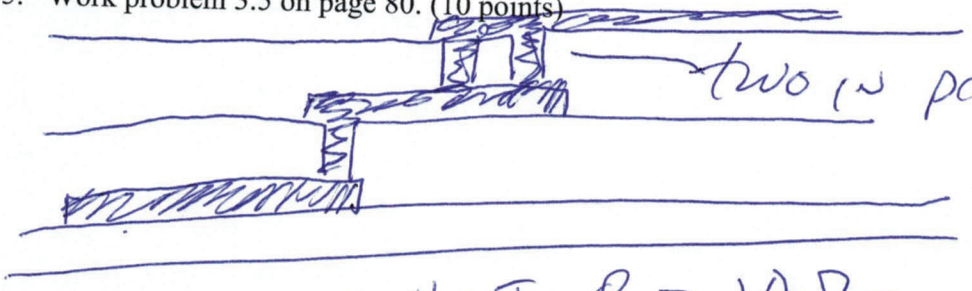


Attract electrons, which in direction shown

which cause W ↗

C ↘

5. Work problem 3.5 on page 80. (10 points)



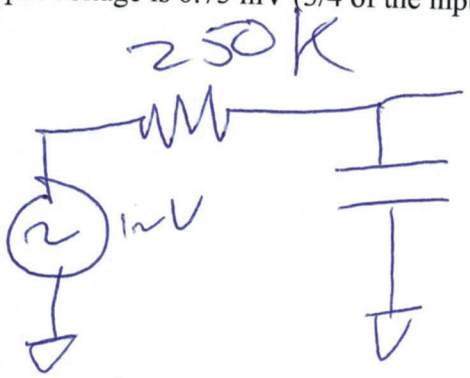
two in parallel

CONTACT R = 10Ω

contact resistance = 5Ω

3)

6. For problem 6.1 on page 162 determine the frequency when the AC component of the output voltage is 0.75 mV (3/4 of the input AC voltage). (20 points)



$54.54 - 225\,fF$

$625\,fF$ / μm^2

$$0.75 = 1 \cdot \frac{\frac{1}{j \cdot 2\pi f \cdot 625f}}{\frac{1}{j \cdot 2\pi f \cdot 625f} + 250k}$$

$$0.75 = \frac{1}{1 + j \cdot 2\pi f \cdot 625f \cdot 250k}$$

$$0.75 = \frac{1}{\sqrt{1 + (f \cdot 981n)^2}}$$

$$.5625 = \frac{1}{1 + (f \cdot 981n)^2}$$

$$.5625(f \cdot 981n)^2 = 0.4375$$

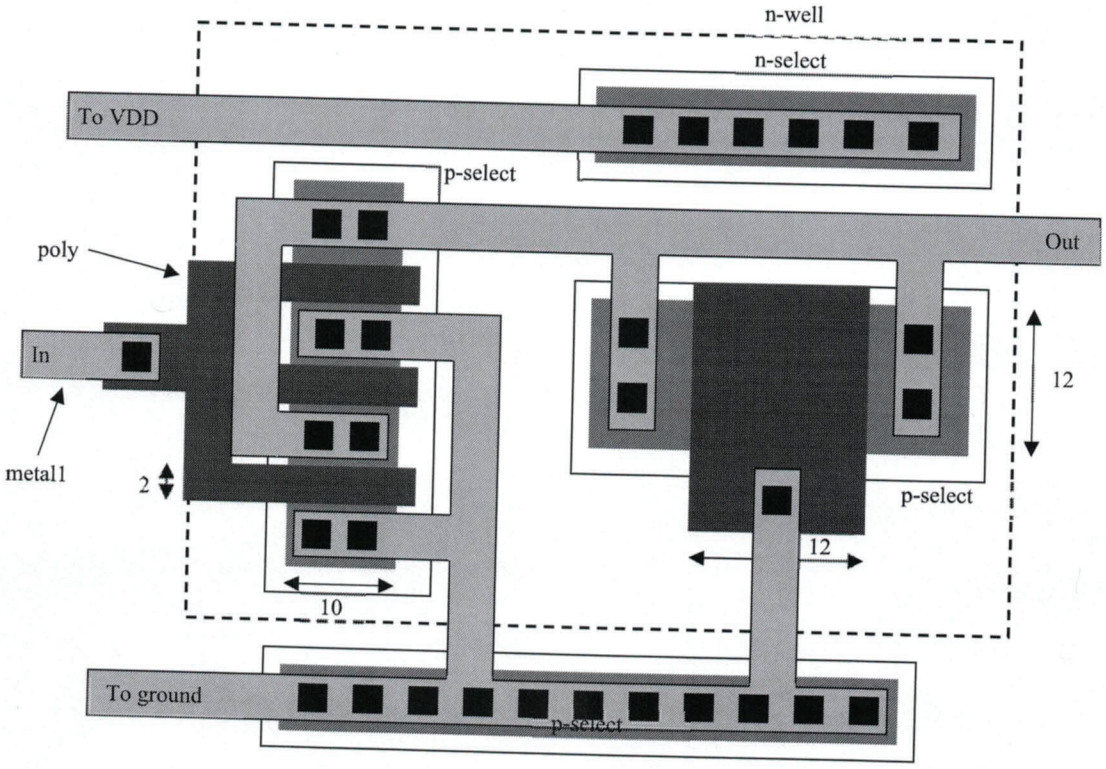
$$f^2(981n)^2 = 0.777$$

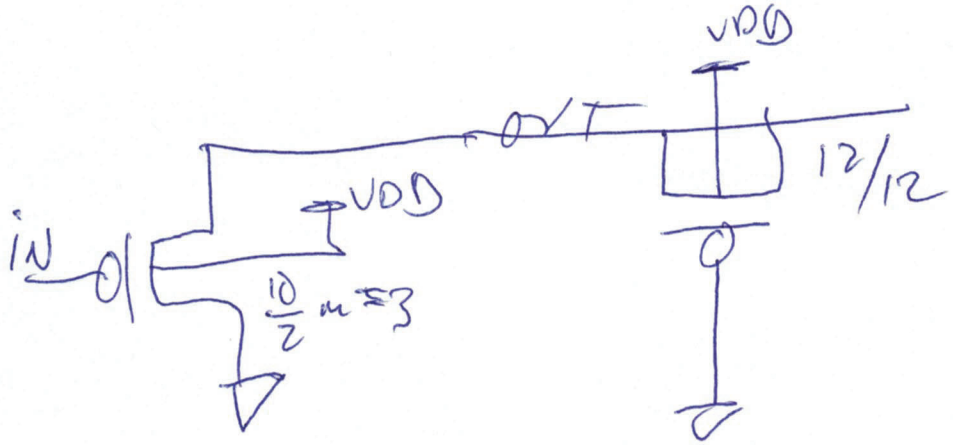
$$f \cdot 981n = .88$$

$f = 899\,MHz$

4)

7. Sketch the corresponding schematic for the following layout. Make sure the body connections of the MOSFETs are clearly seen in your schematic. (15 points)

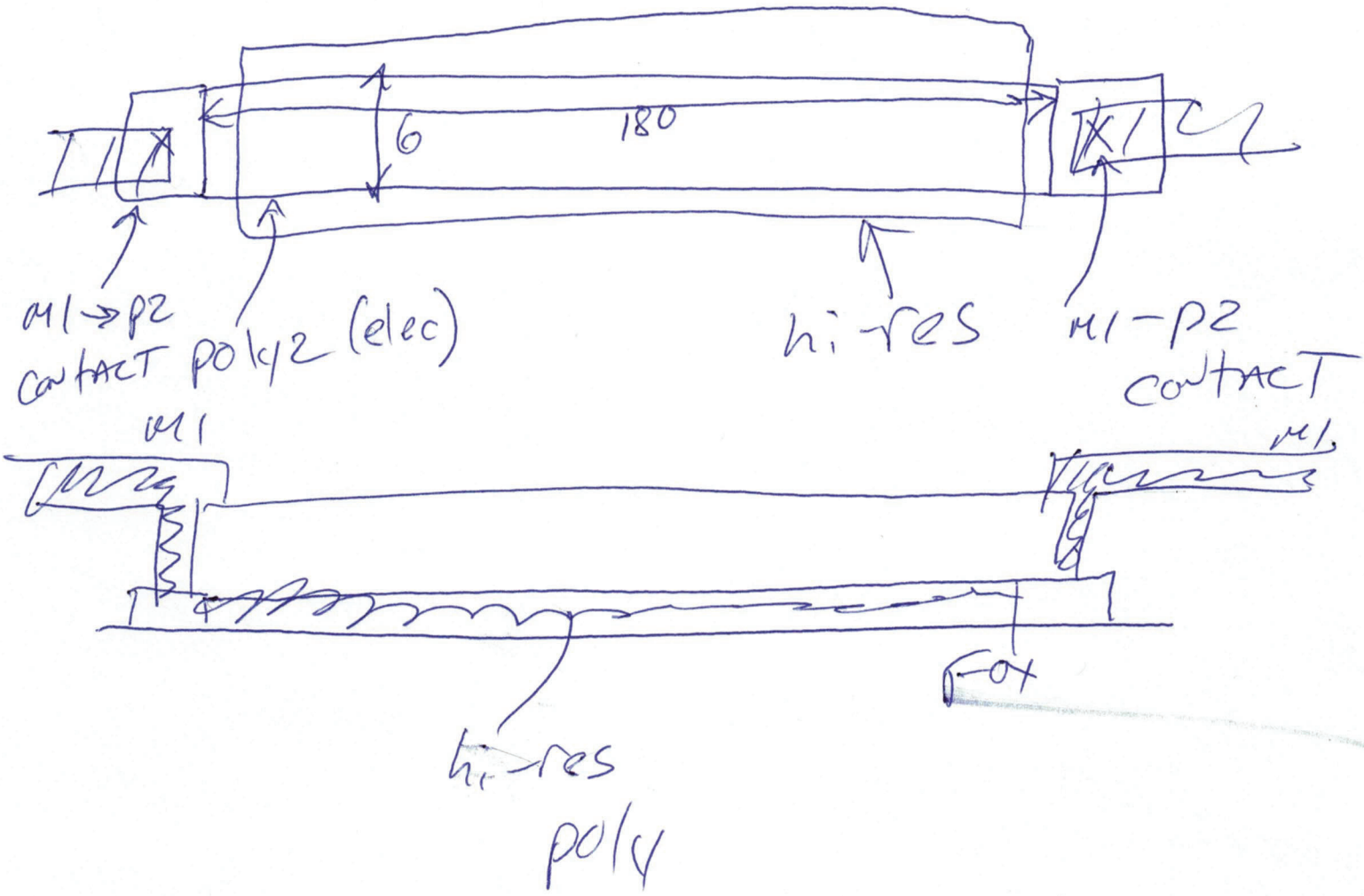




5)

8. Sketch the layout of a 30k poly2 resistor in the C5 process using the hires layer assuming the sheet resistance is 1k/square. Make sure to label each of the layers in your layout. Sketch the cross-sectional view of your layout. Explain what the hires layer does during the fabrication process. (20 points)

hi-res blocks poly2 from being doped



6)