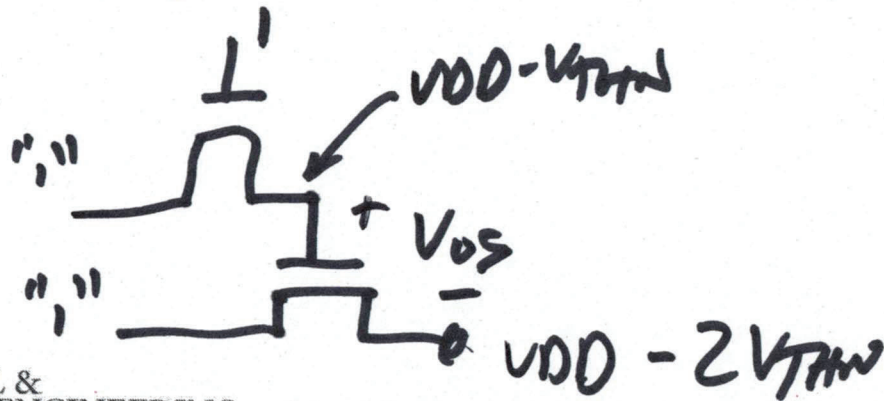
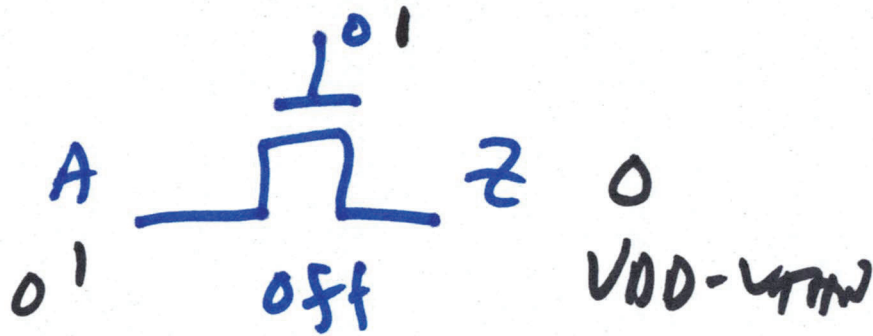


EE 421 / ECG 621

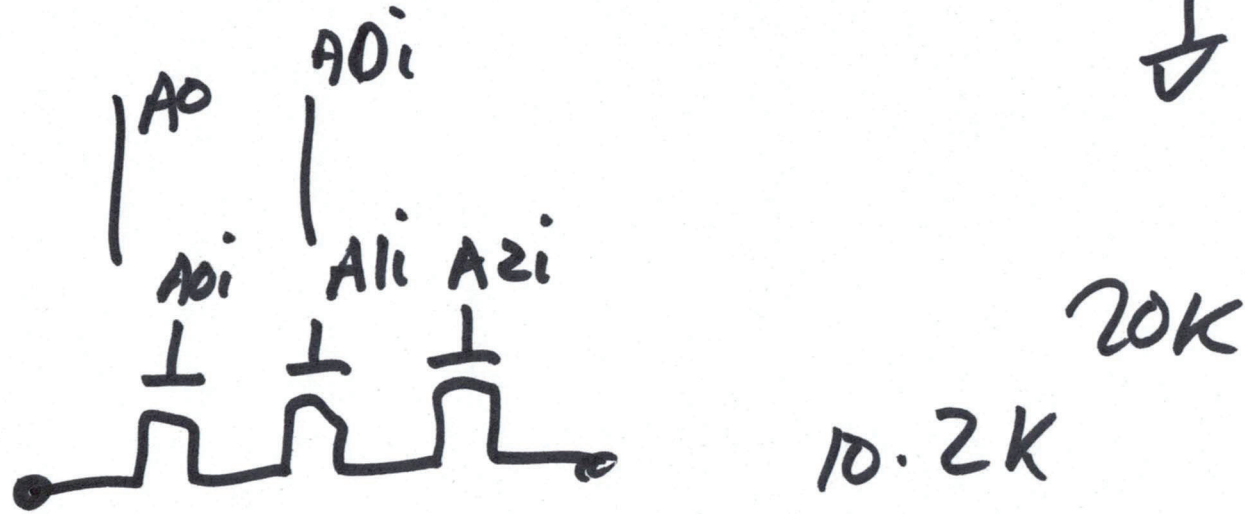
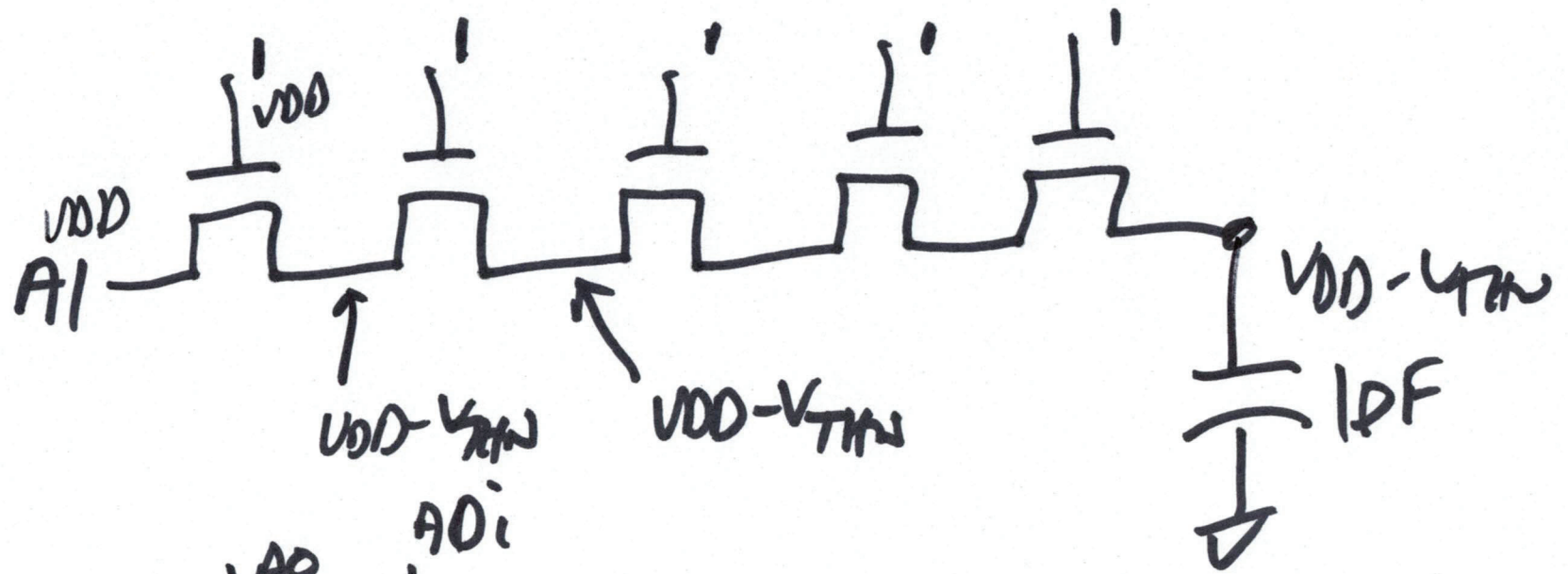
Digital IC Design

OCT. 21, 2020

Lecture 16



1)

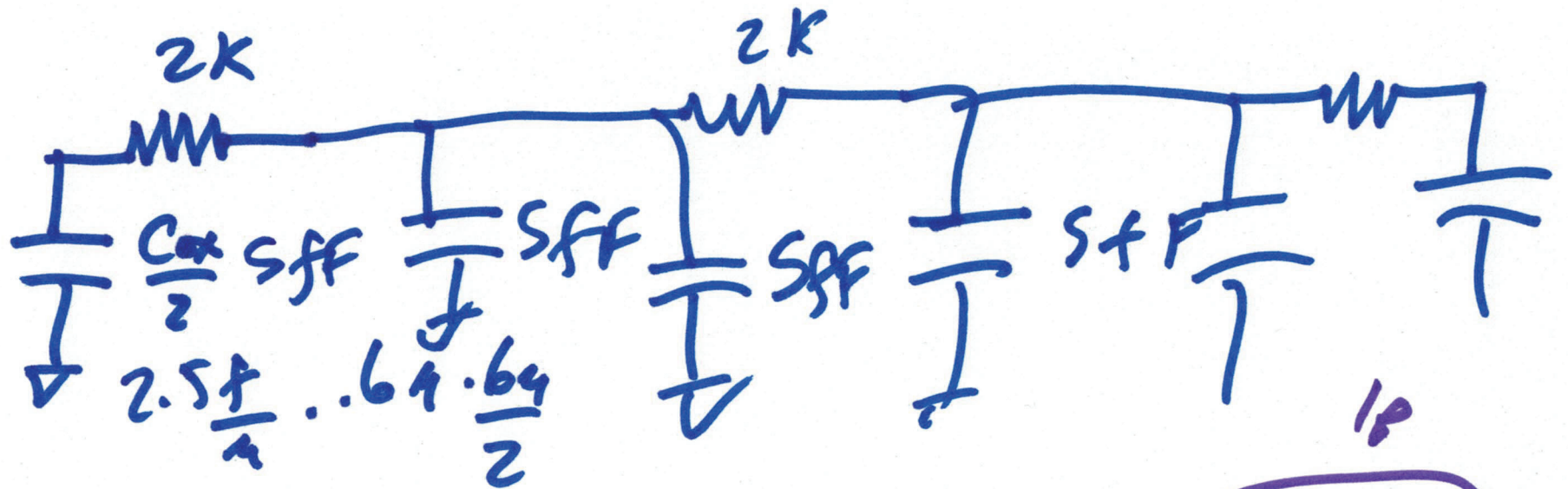


$$20 \cdot \frac{6}{6} = 20$$

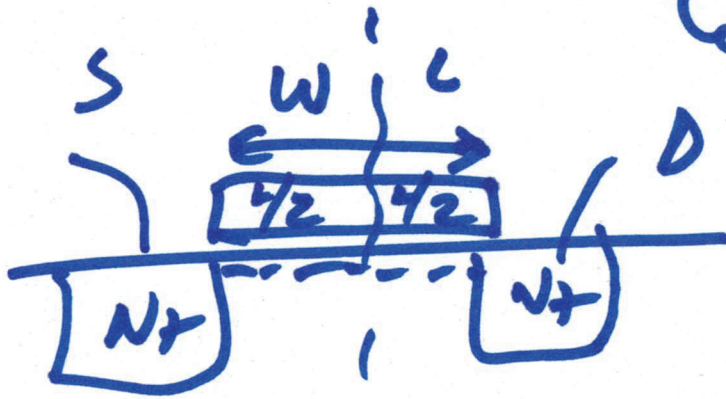
$$t_d = 0.7 \cdot 20k \cdot 1pF = 14ns$$

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2)



$$2(2+1)$$



$$t_d = 0.35 \cdot 10f \cdot 2k \cdot 10^2 + 10 \cdot 2k \cdot C_L$$

700p

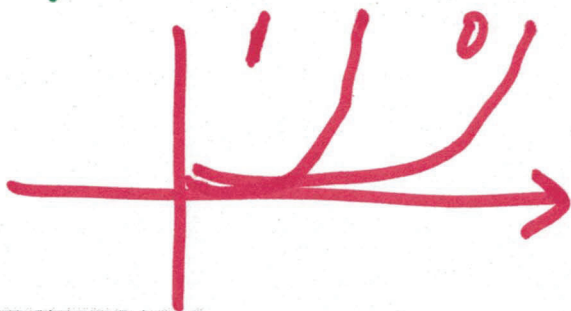
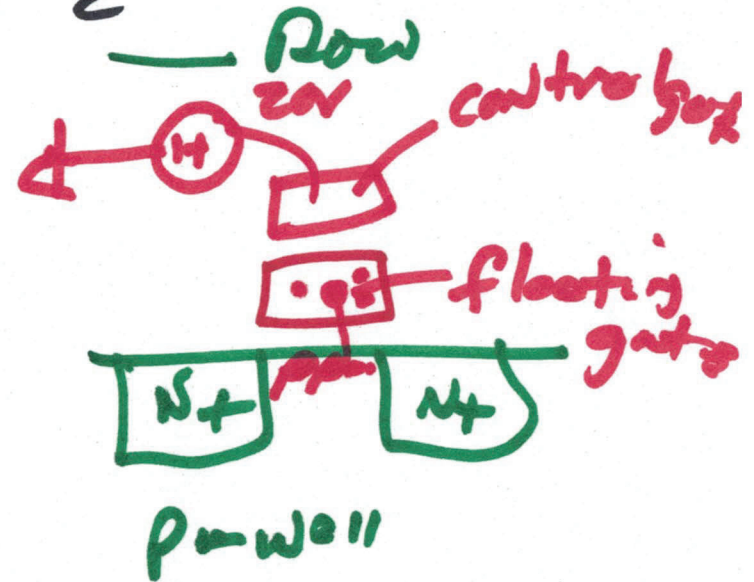
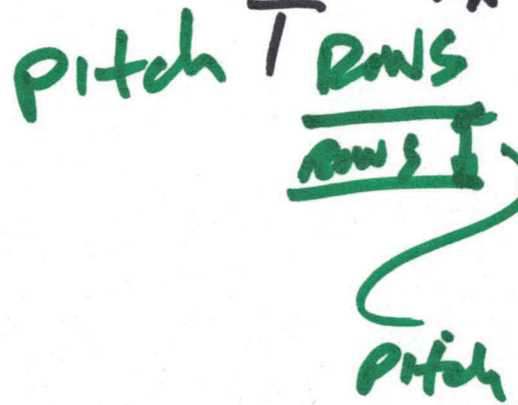
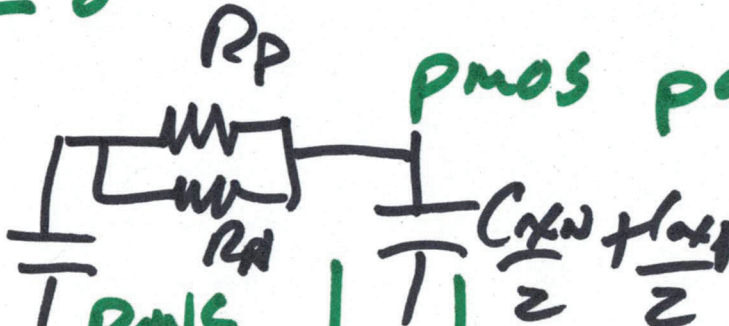
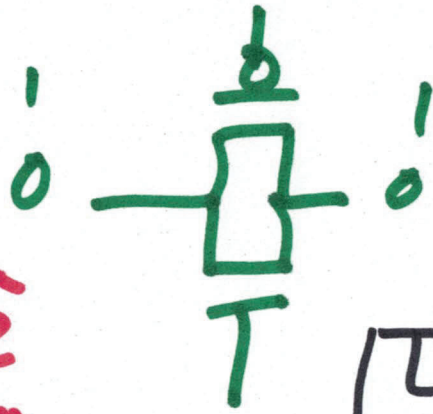
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \cdot w \cdot \frac{L}{2}$$

3)

# Transmission Gate

NMOS passes a "0" well

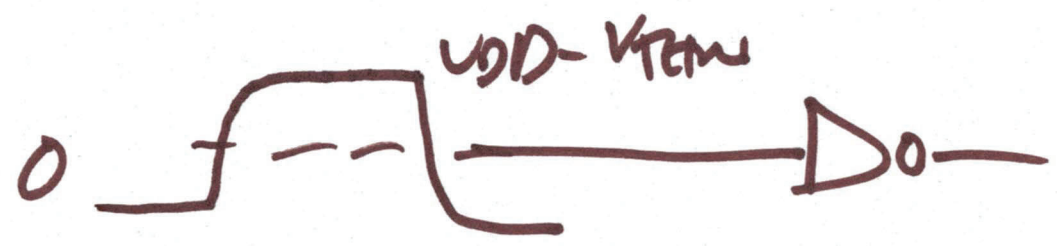
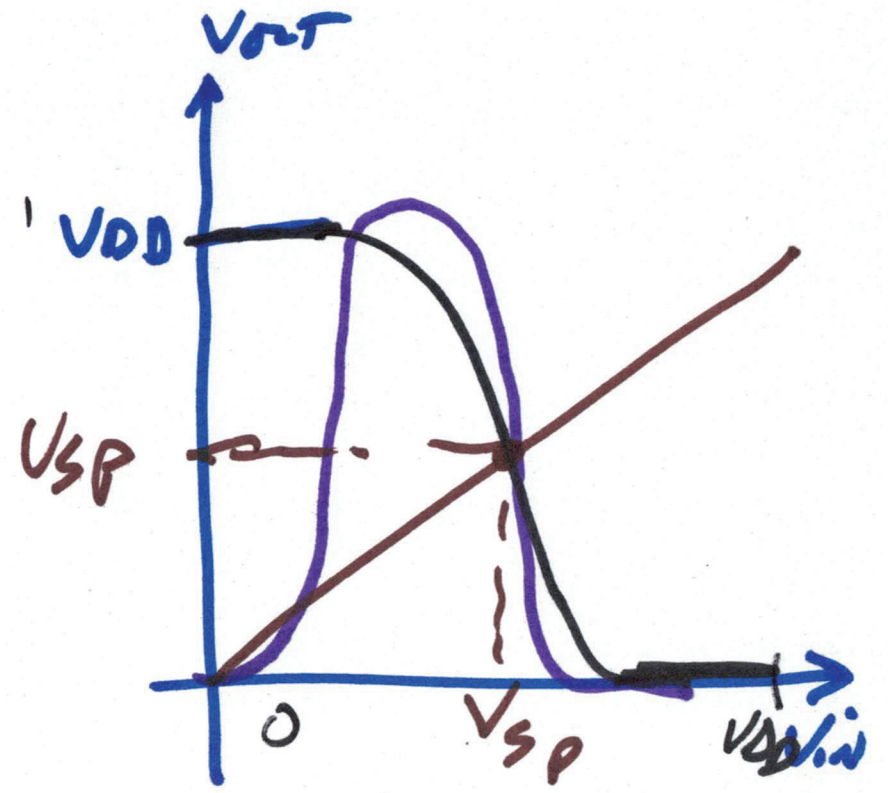
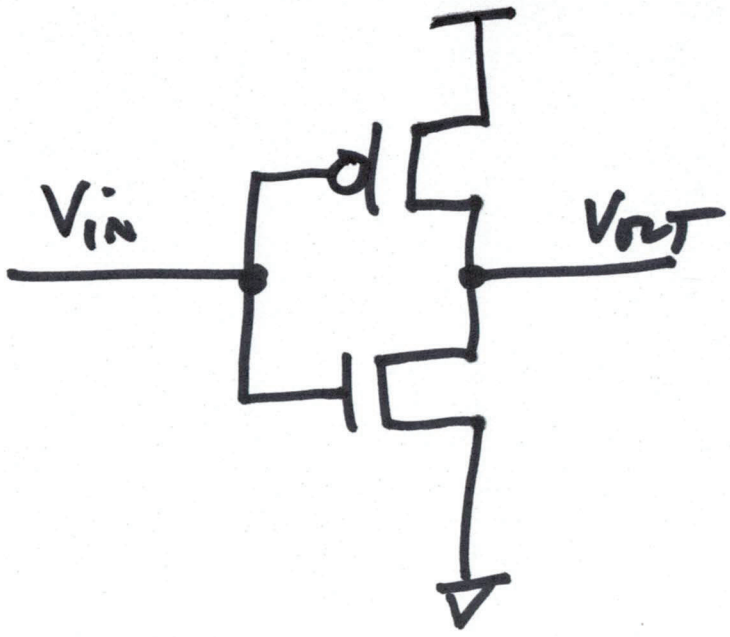
PMOS passes a "1" well



EEPROM  
erasable  
programmable  
cellular  
array

4)

# The inverter



5)