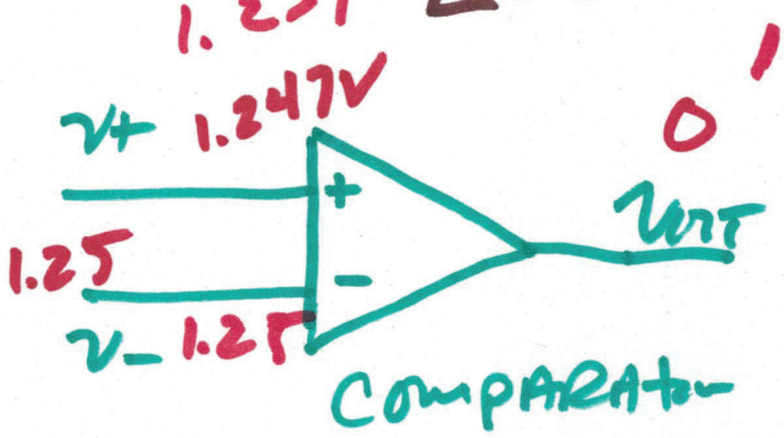
EE 421/ECE 621

Digital IC Design

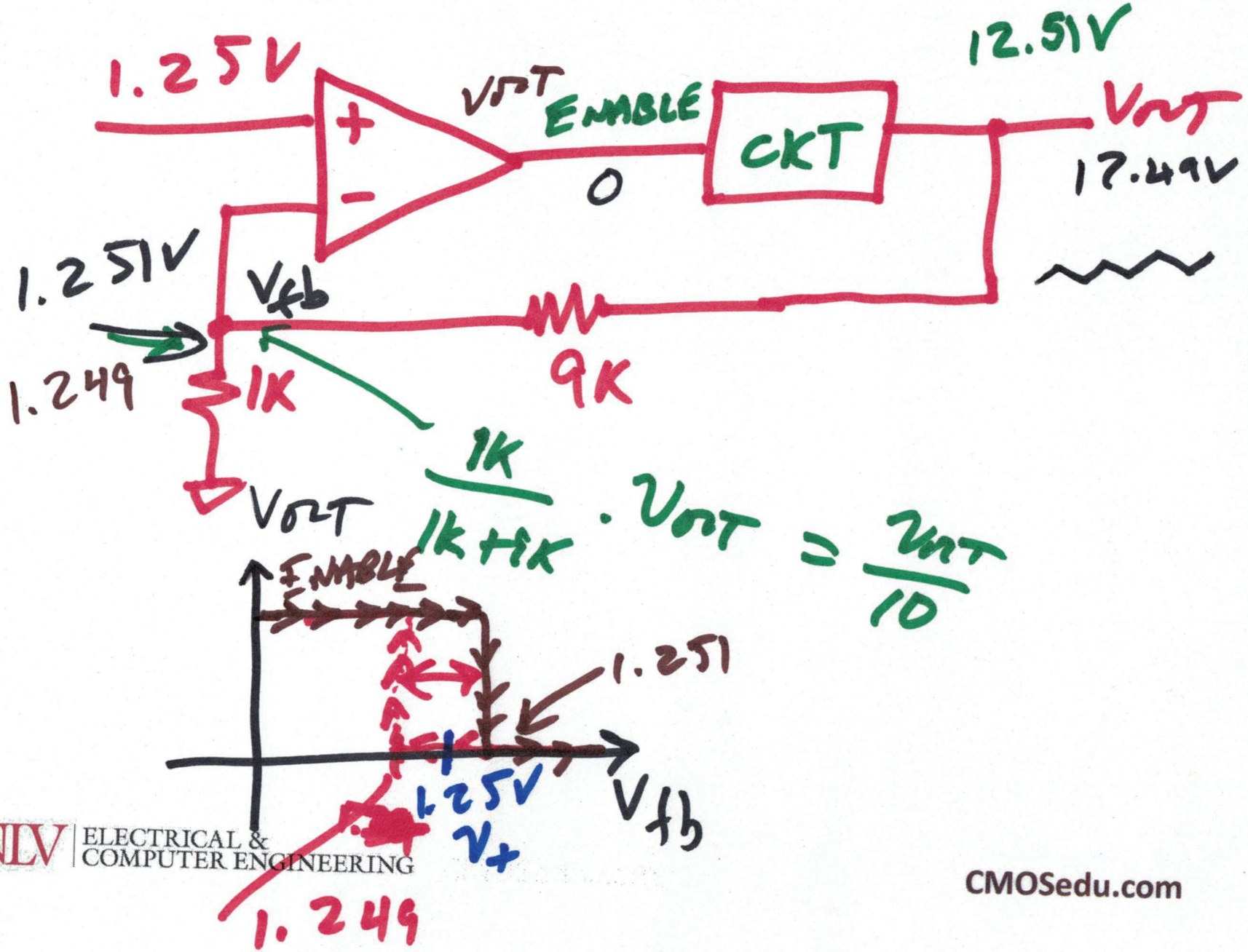
November 2, 2020

Lecture 19



$V_+ > V_-$ $V_{OUT} = 1$

$V_+ < V_-$ $V_{OUT} = 0$



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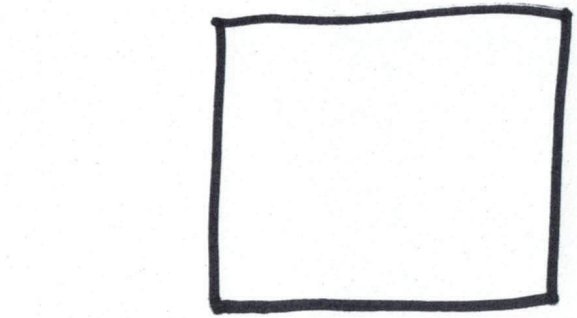
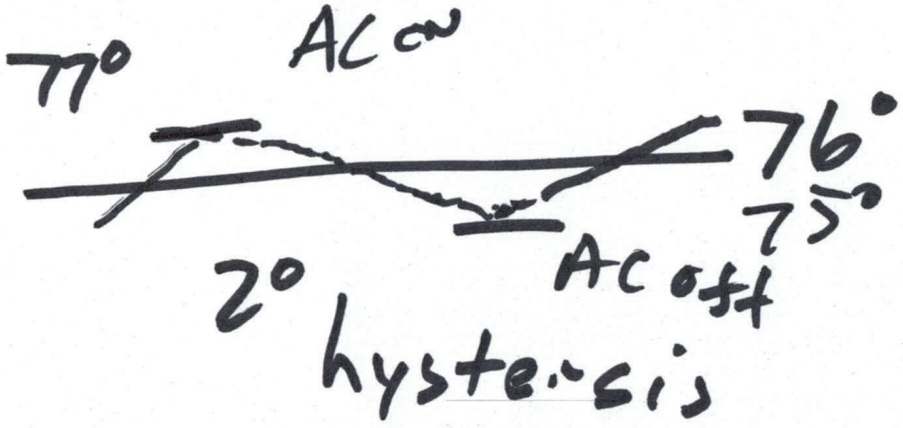
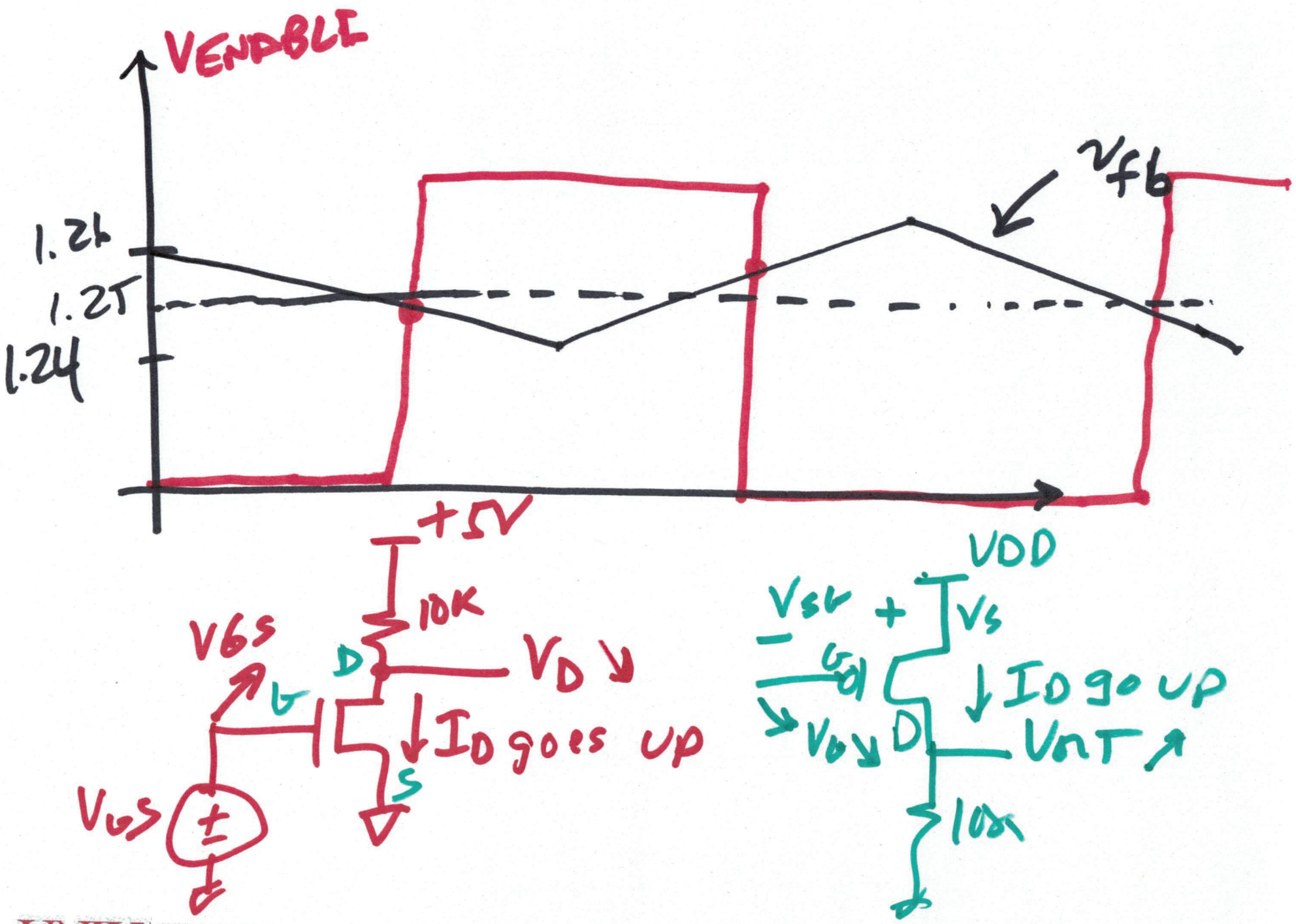
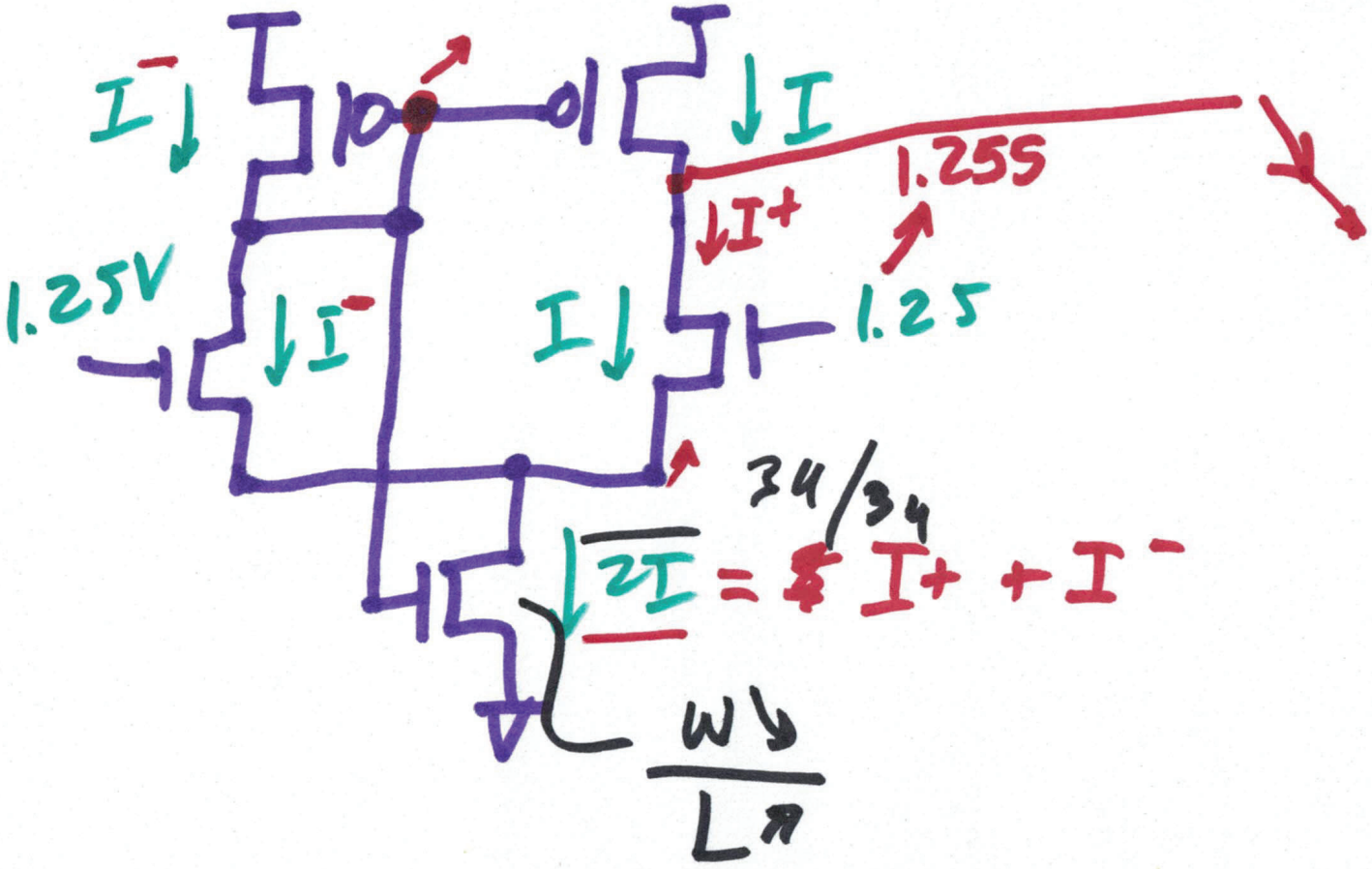


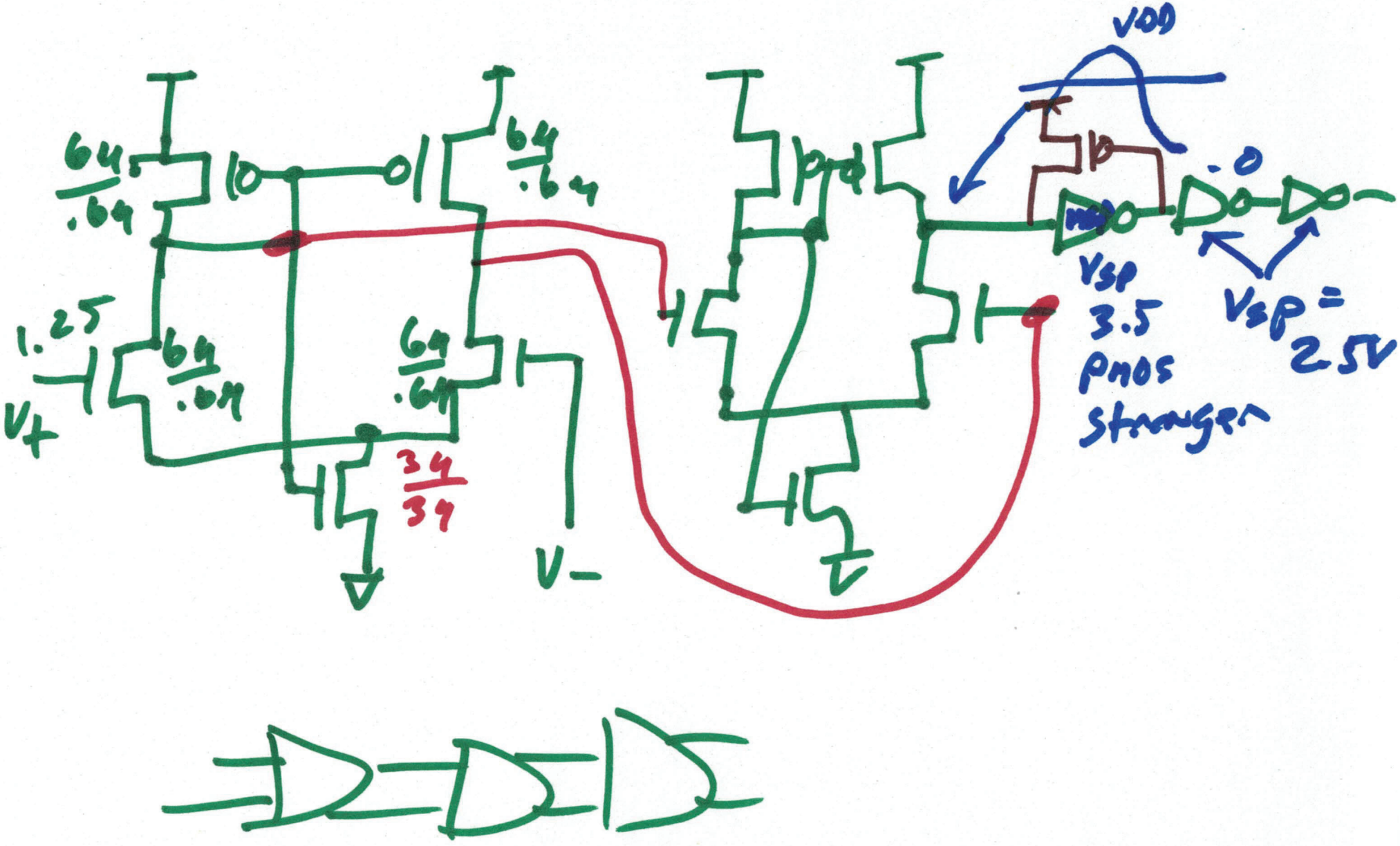

77°
AC on
76°
75°
AC off
2°
hysteresis

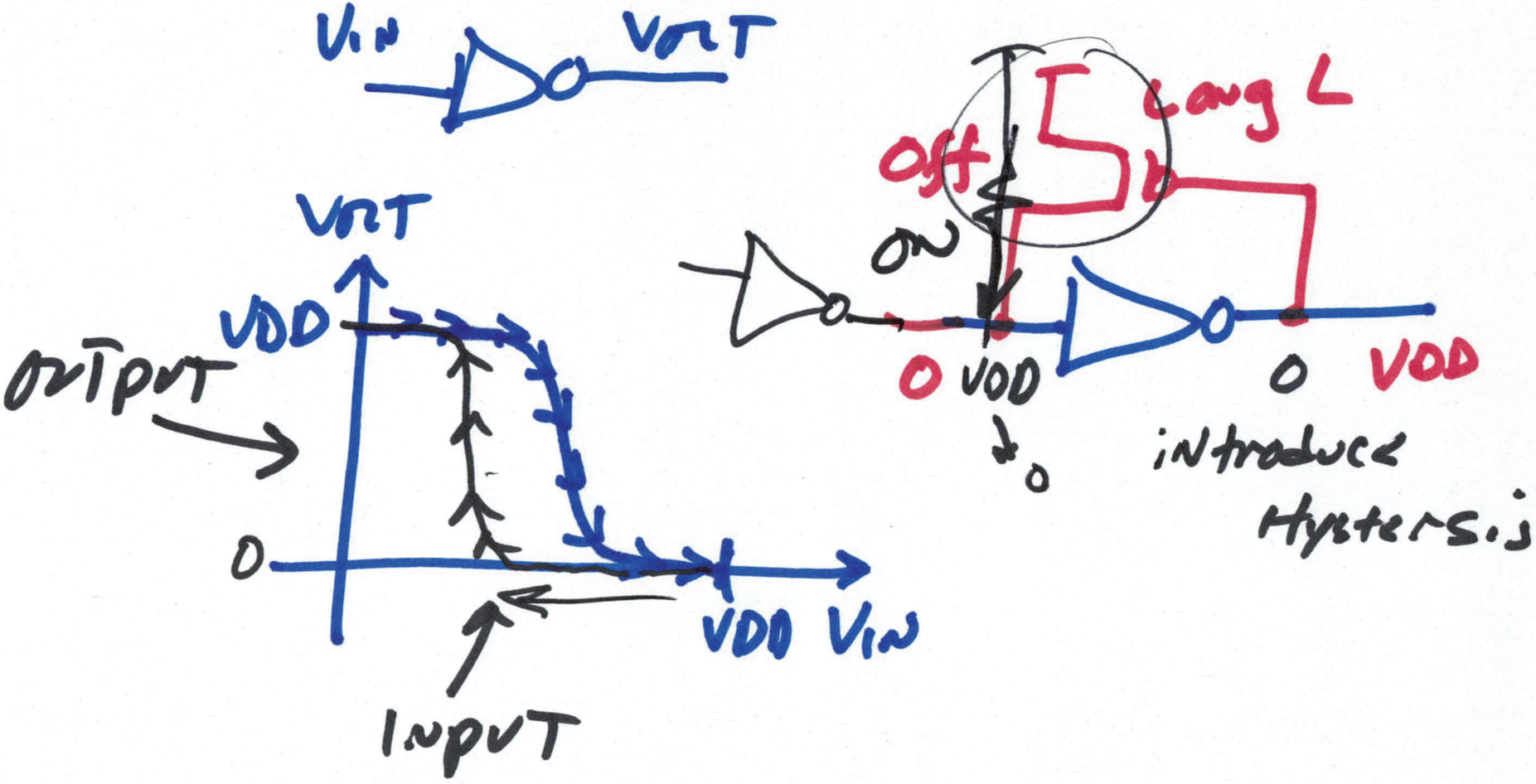

VENDBLI
1.26
1.25
1.24
Vfb
+5V
10K
VGS
D
VD ↘
G
S
ID goes up
VDS
VDD
VSG
+
VS
G
ID go up
VSG ↘
D
VDT ↗
10K

Comparator Design

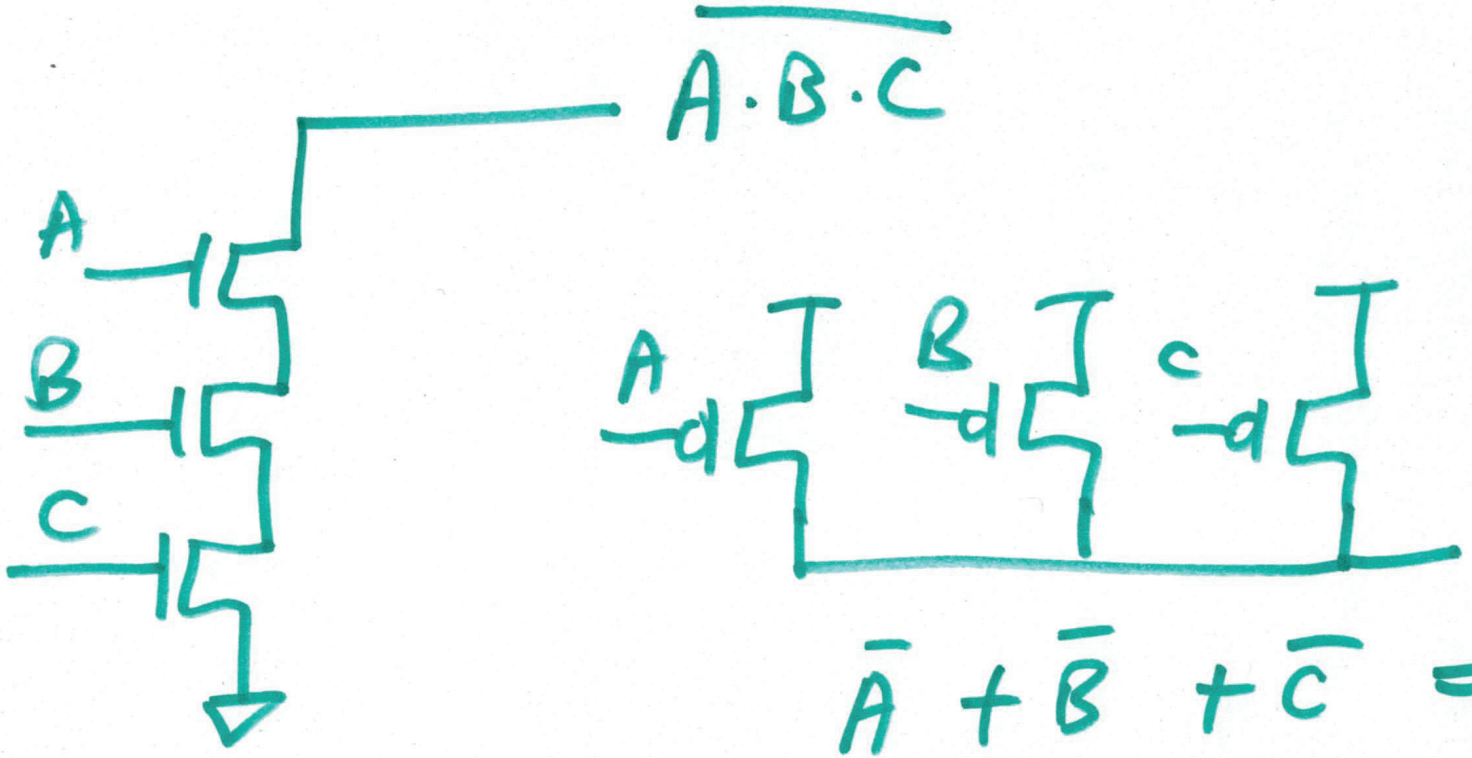
self-biased diff-Amp




VDD
64/.64
64/.64
1.25
64/.64
64/.64
34/34
V+
V-
VSP
3.5
PMOS
Stronger
VSP =
2.5V


VIN
VOUT
VOUT
VDD
OUTPUT
0
VDD VIN
INPUT
Long L
off
ON
0 VDD
0 VDD
Introduce
Hysteresis

CMOS Complex logic



$$\bar{A} + \bar{B} + \bar{C} =$$

$$\overline{\bar{A} + \bar{B} + \bar{C}} = \overline{A \cdot B \cdot C}$$