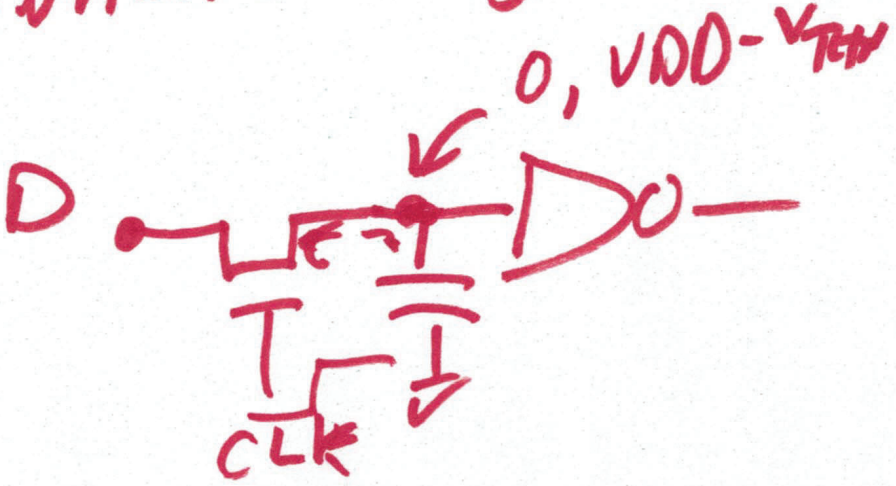
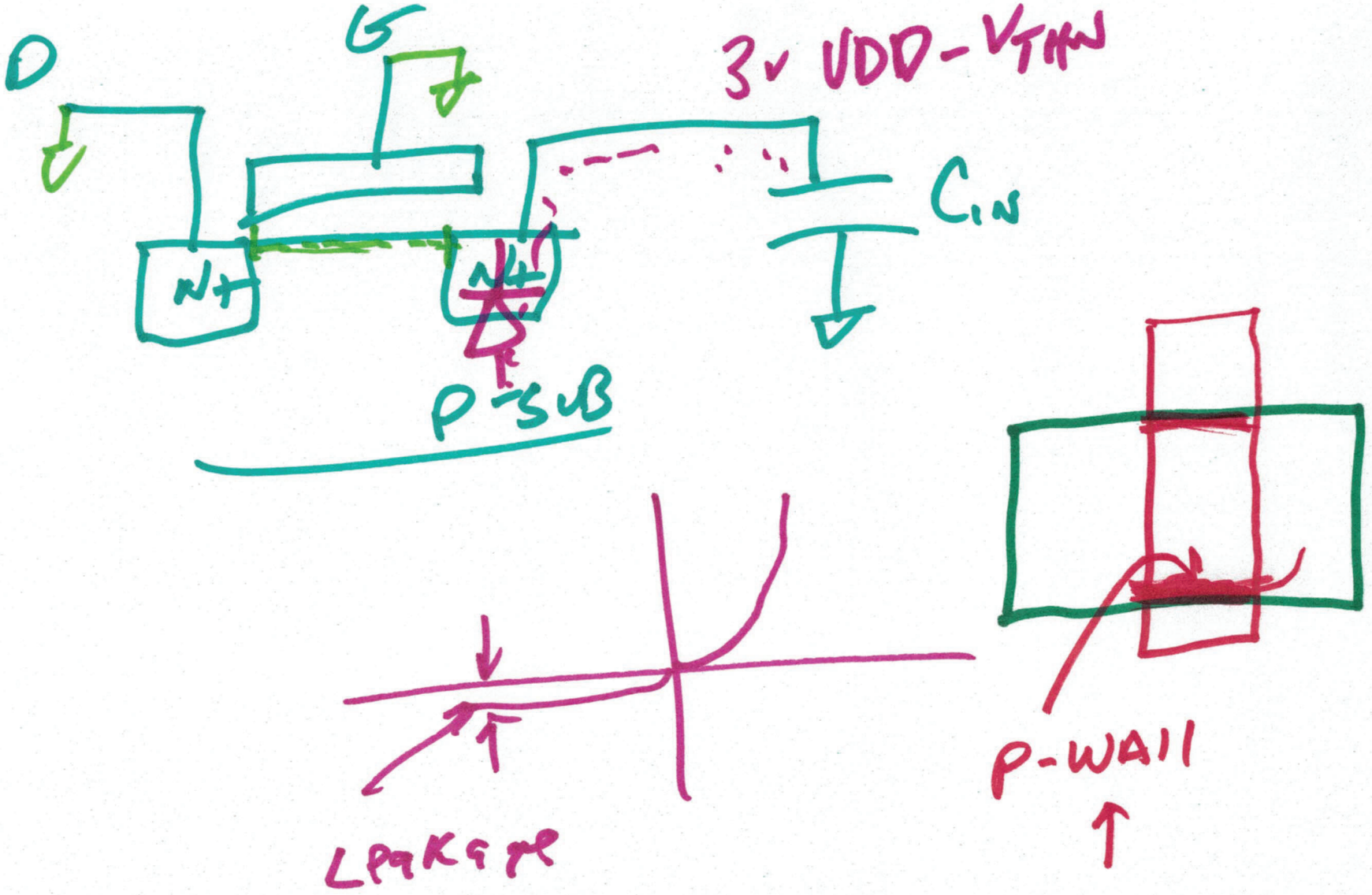
EE 421/ECG 621
Digital IC Design
Lecture 24,
NOV. 23, 2020

Dynamic Logic



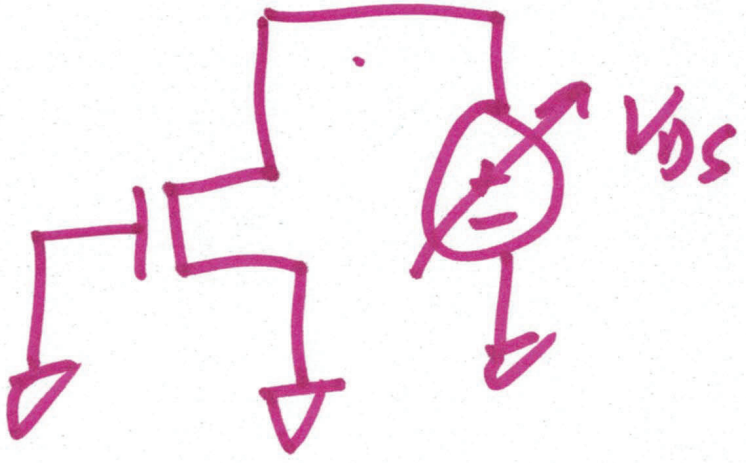


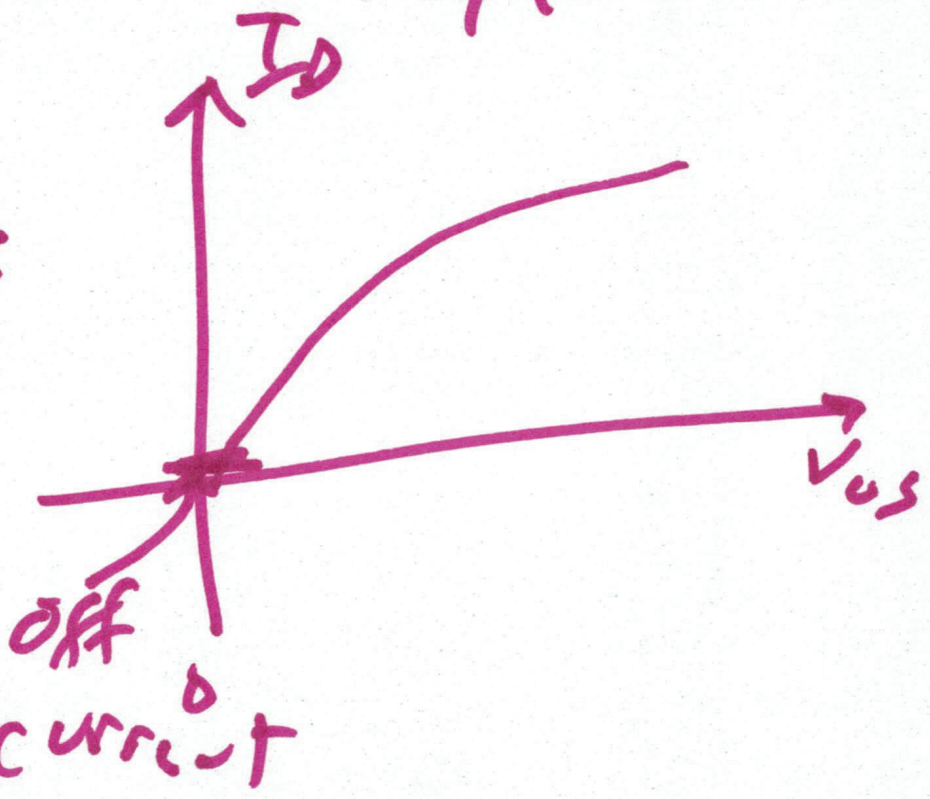
2)

off current

NA/μm

NANO Amps / μ (micron)

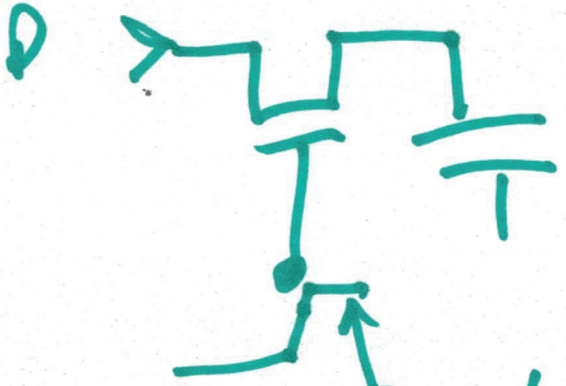


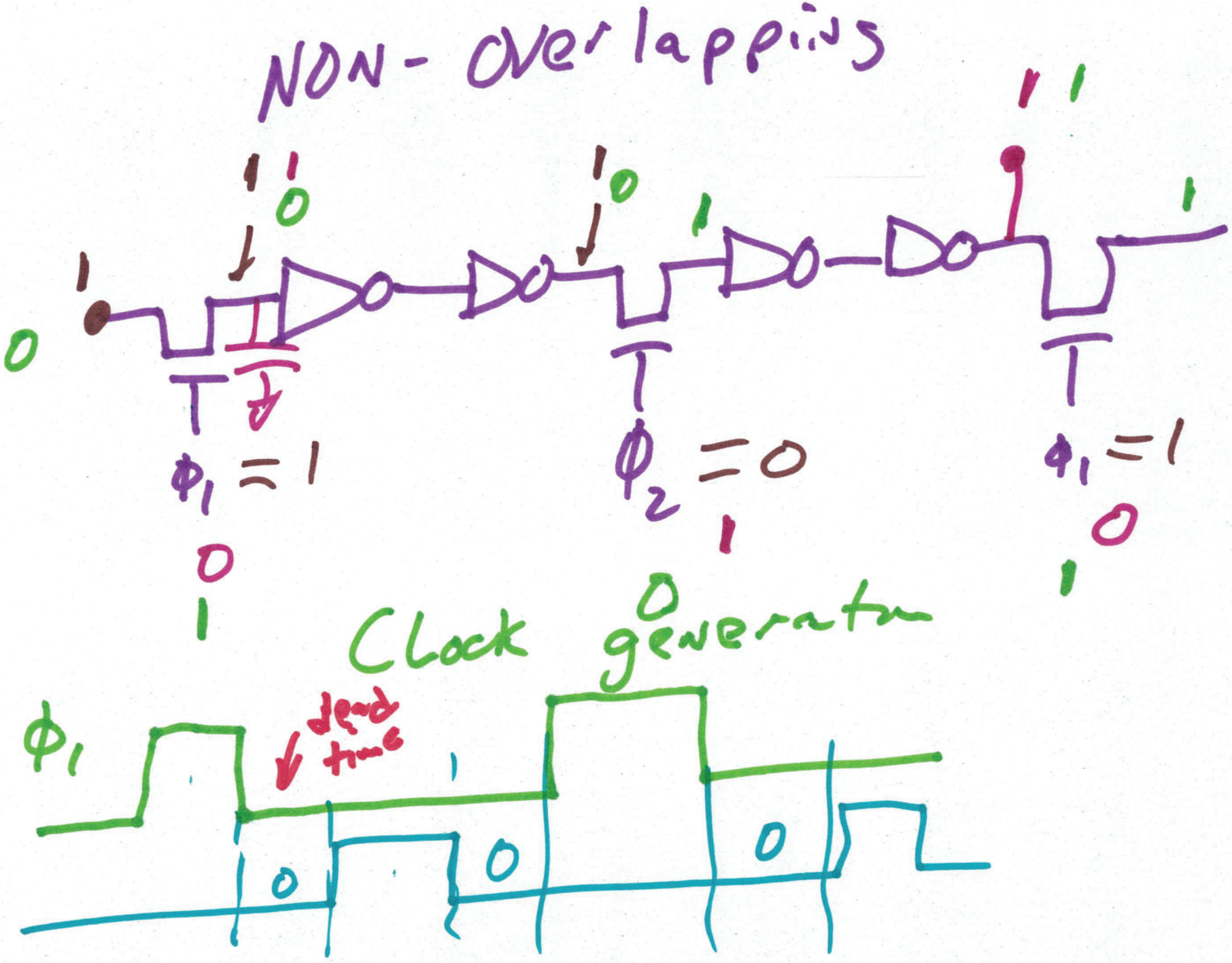


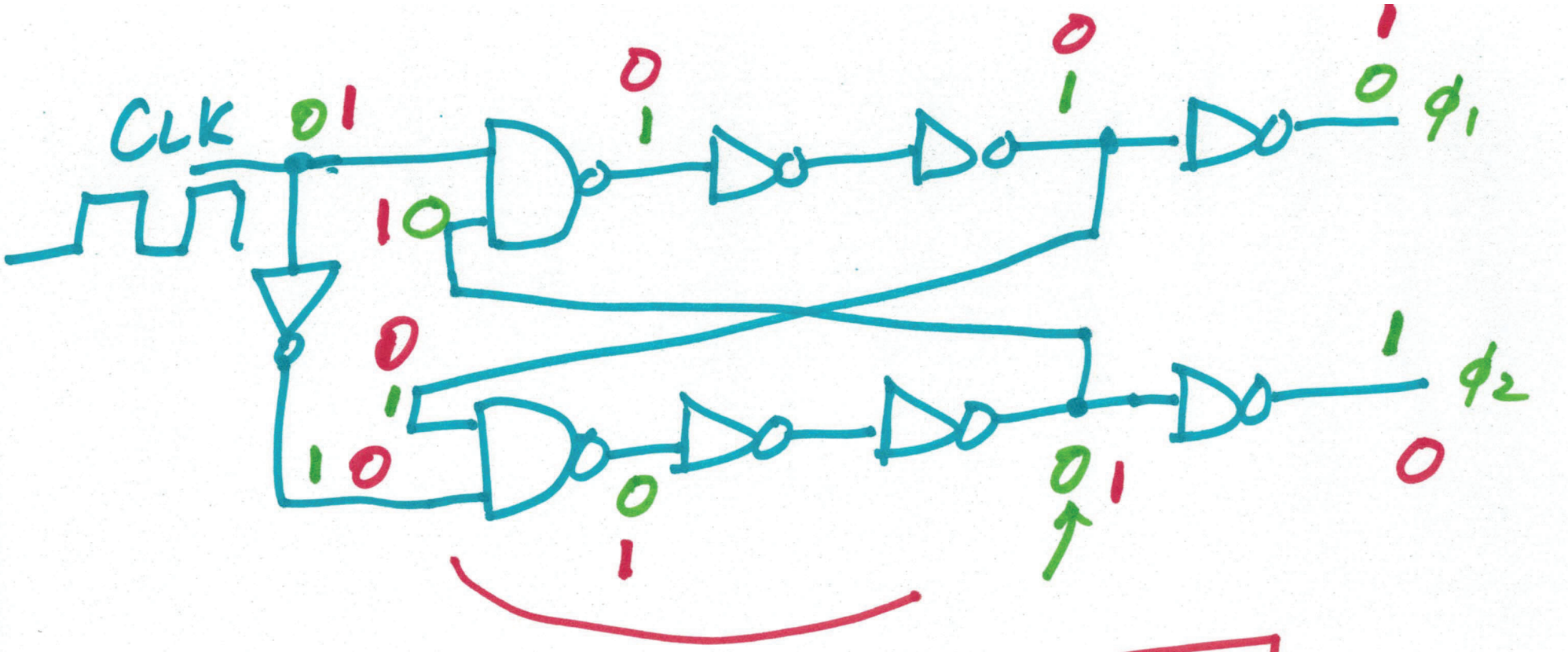
trench gate

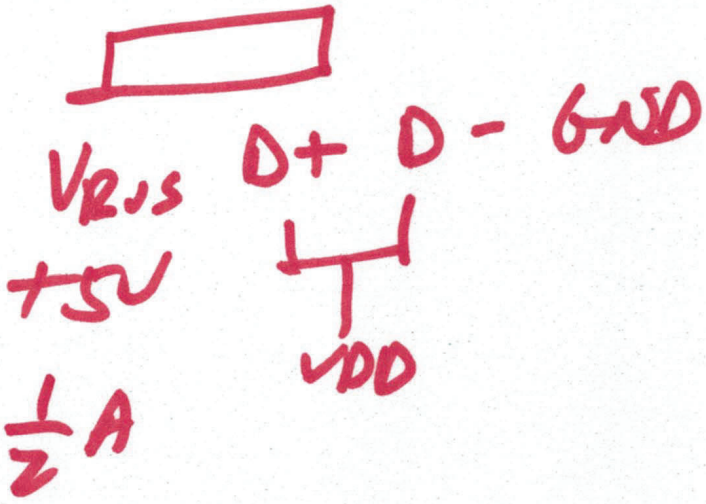
1-transistor, 1-capacitor memory cell

1T1C → DRAM (DYNAMIC RANDOM ACCESS MEMORY) computer memory




NON-Overlapping
$\phi_1 = 1$
$\phi_2 = 0$
$\phi_1 = 1$
Clock generator
ϕ_1
dead time


CLK
0 1
1 0
0 1
1 0
0 1
1 0
0 1
1 0
0 1
1 0
0 1
1 0
q_1
q_2

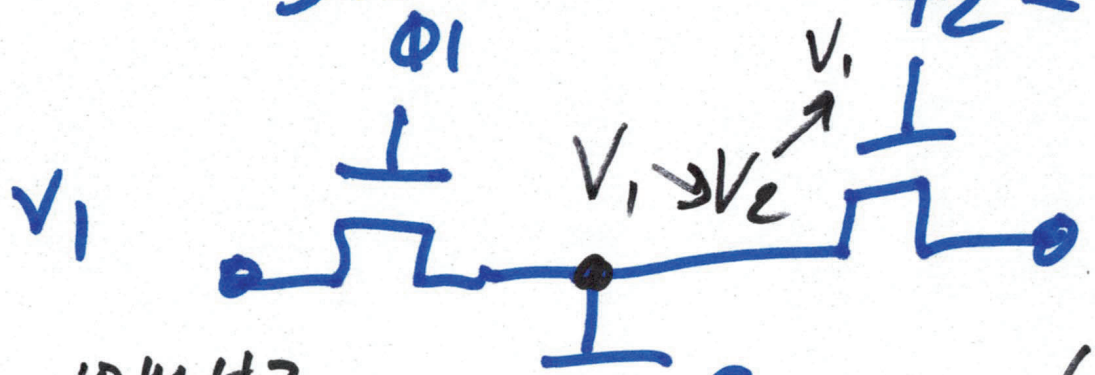

V_{BUS}
+5V
$\frac{1}{2}$A
D+
D-
GND
VDD

b)

IMEG

V_1 —/\/\/\— V_2 RC

Switched-capacitor ← Non-overlapping

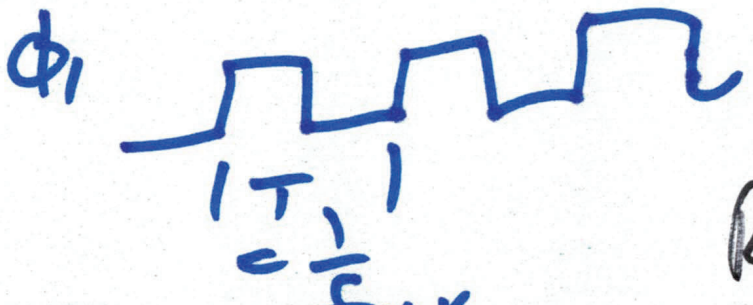


$CV = Q$

$C(V_1 - V_2) = Q$

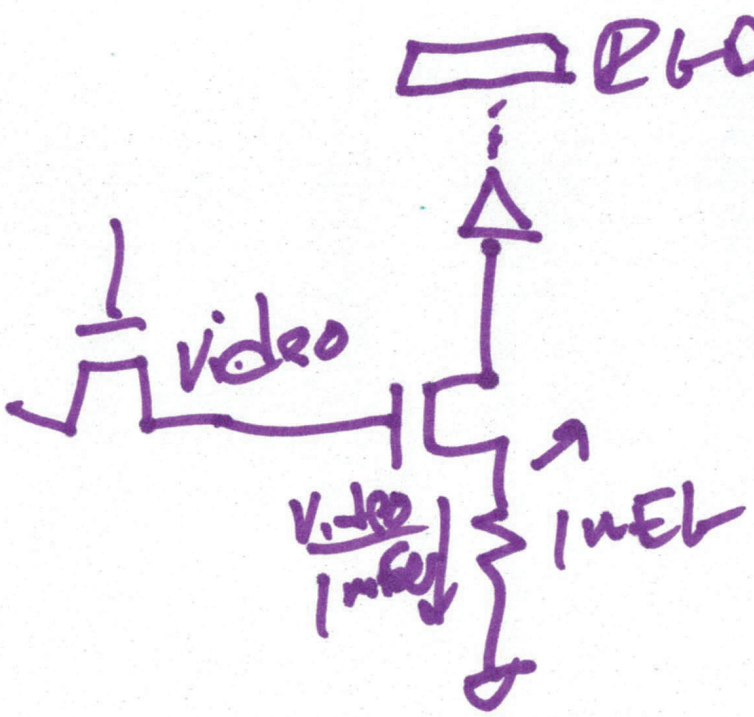
1pF · 10MHz

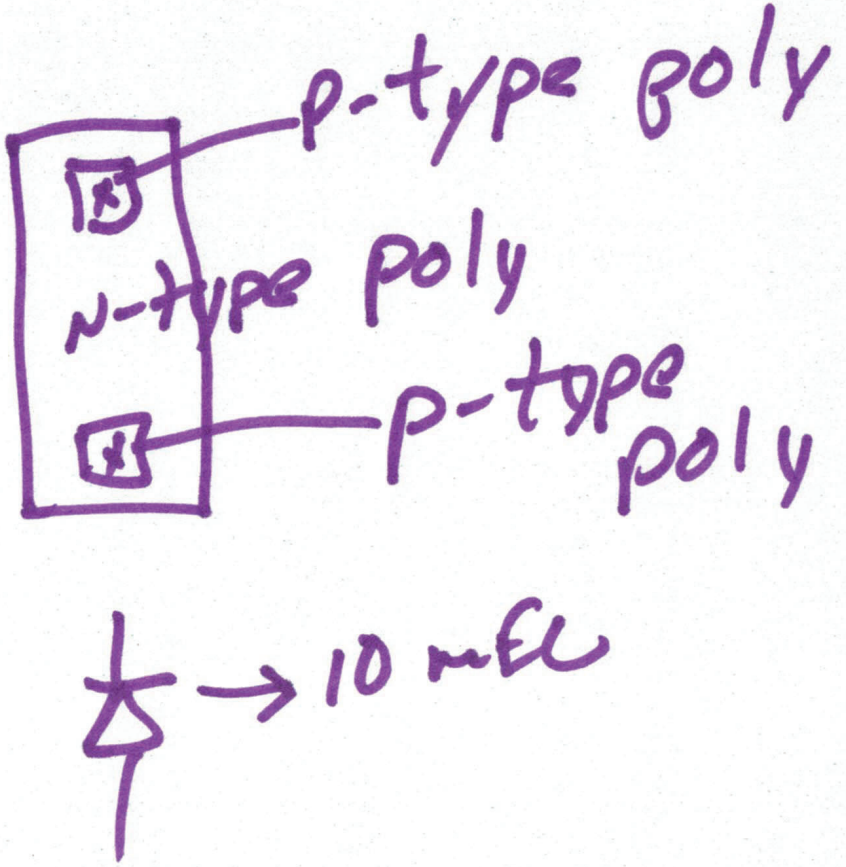
$\frac{1}{10^7 \cdot 10^{-12}} = \frac{1}{10^{-5}} = 100K$

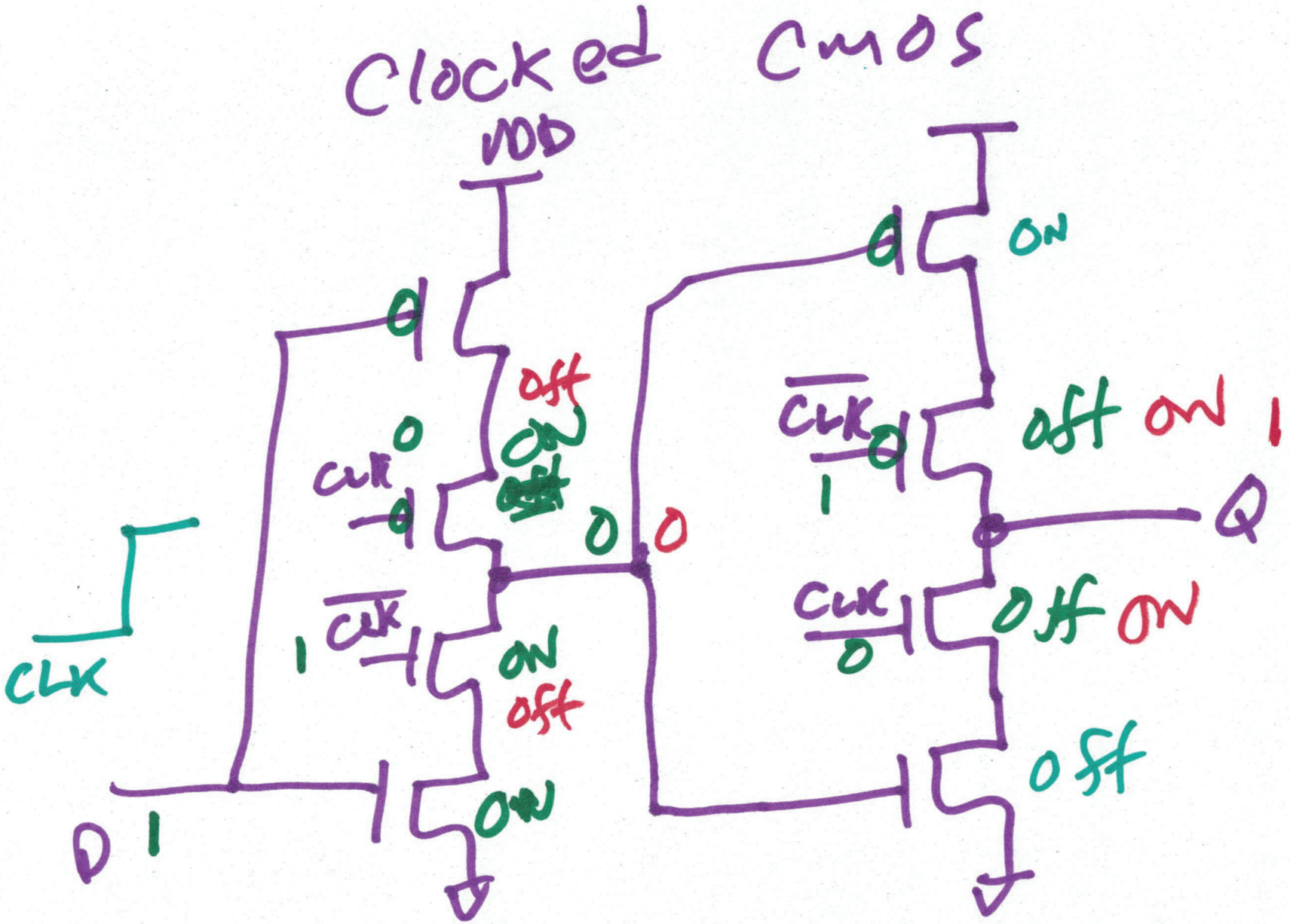


$I_{AVG} = \frac{Q}{T} = \frac{Qf}{\Sigma}$

$R_{SC} = \frac{V_1 - V_2}{I_{AVG}} = \frac{1}{fC}$

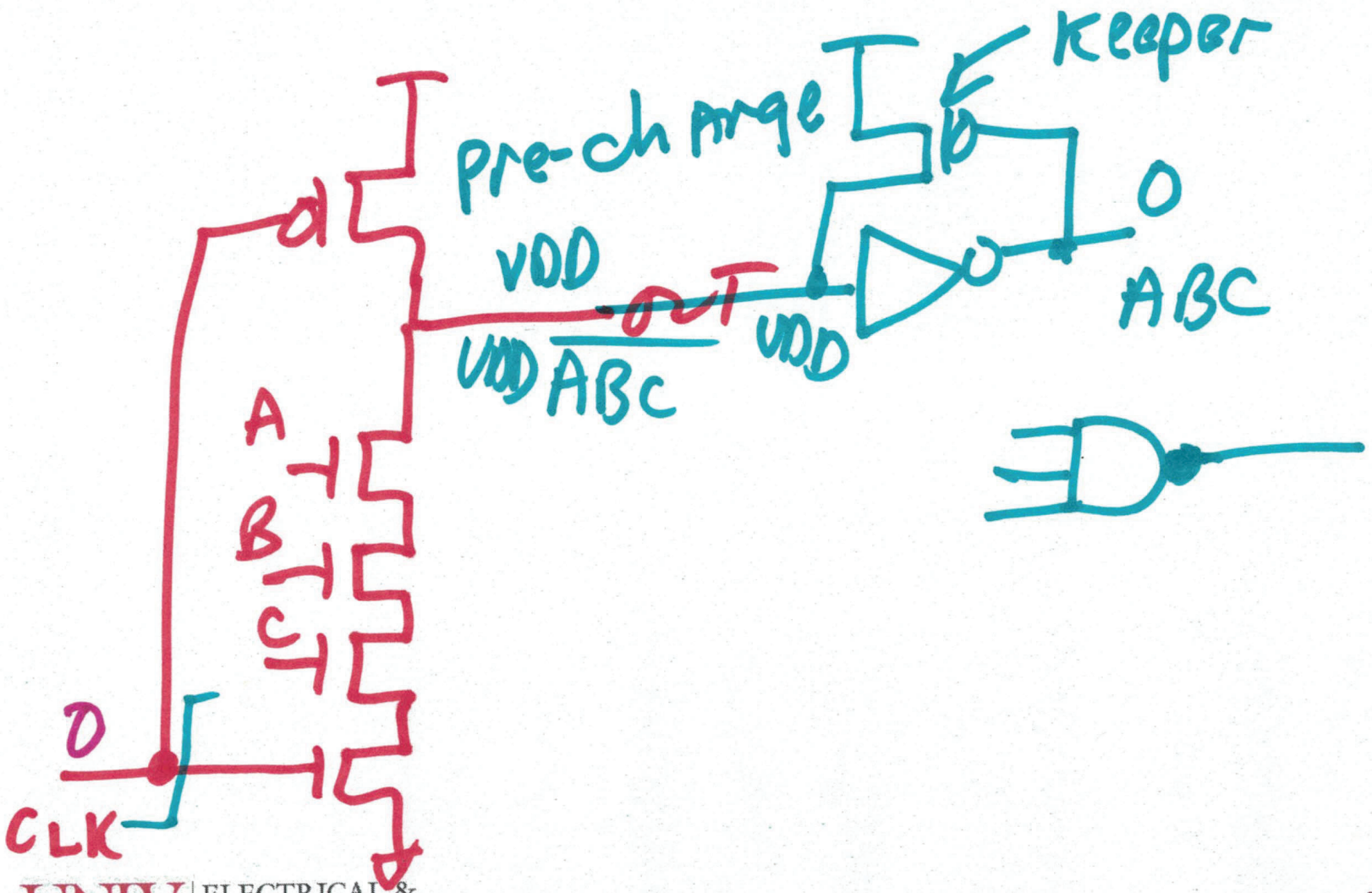

RGO
Video
1mEL


p-type poly
n-type poly
p-type poly
10 mEL


Clocked CMOS
VDD
CLK
D
Q
ON
off

Pre-charge Evaluate

PE-logic



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