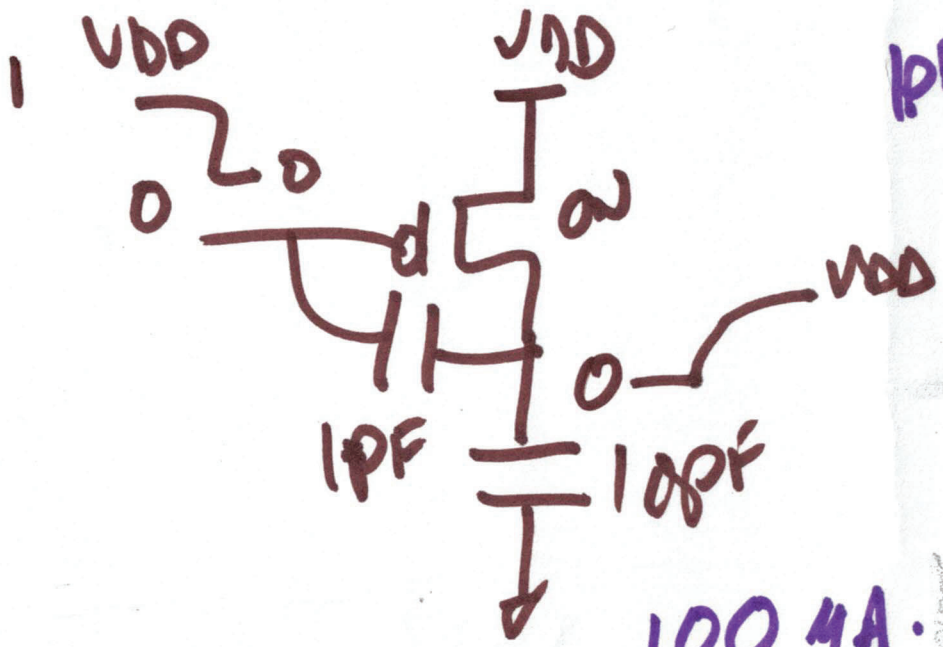
EE 421 / ECG 621
Digital IC Design
Oct. 20, 2021



$1pF(V_{DD}-0)$ —

$1pF(0-V_{DD})$

$2V_{DD}\cdot 1pF$

$100\,\mu A \cdot 100\,ns \quad 10\,pC$

$10{,}000 \cdot 10^{-15} C$

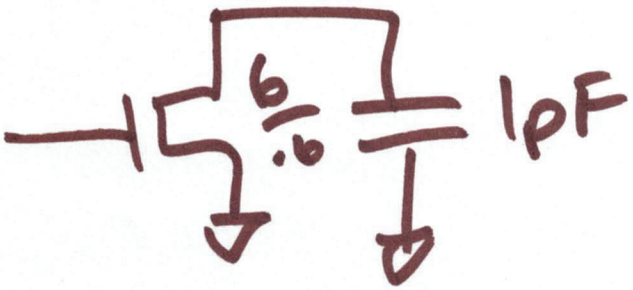
$10\,pC$!

Quiz 11 – EE 421/ECG 621 Digital Electronics and Digital IC Design, Fall 2021

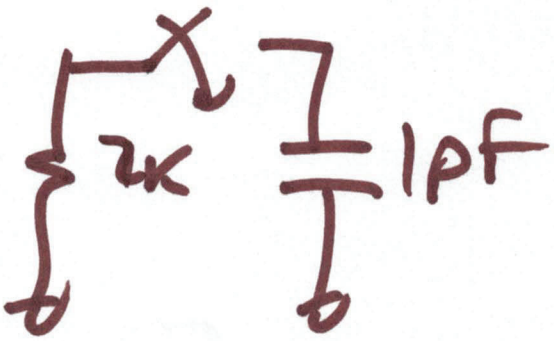
NAME:_____

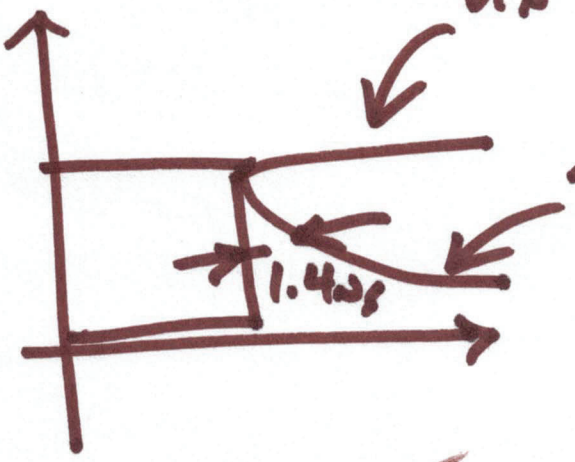
Open book and closed notes.
Show your work for credit!

1. Using the C5 process (R'n = 20k and VDD = 5V) estimate the delay a 6u/0.6u NMOS device will have discharging a 1 pF capacitor. Sketch the schematic, voltages on the gate/drain of the MOSFET, and show your hand calculations. (5 points)



$R_N = 20k \cdot \frac{.6}{6} = 2k$





$t_d = 0.7RC$

$= 0.72k \cdot 10^{-12}$

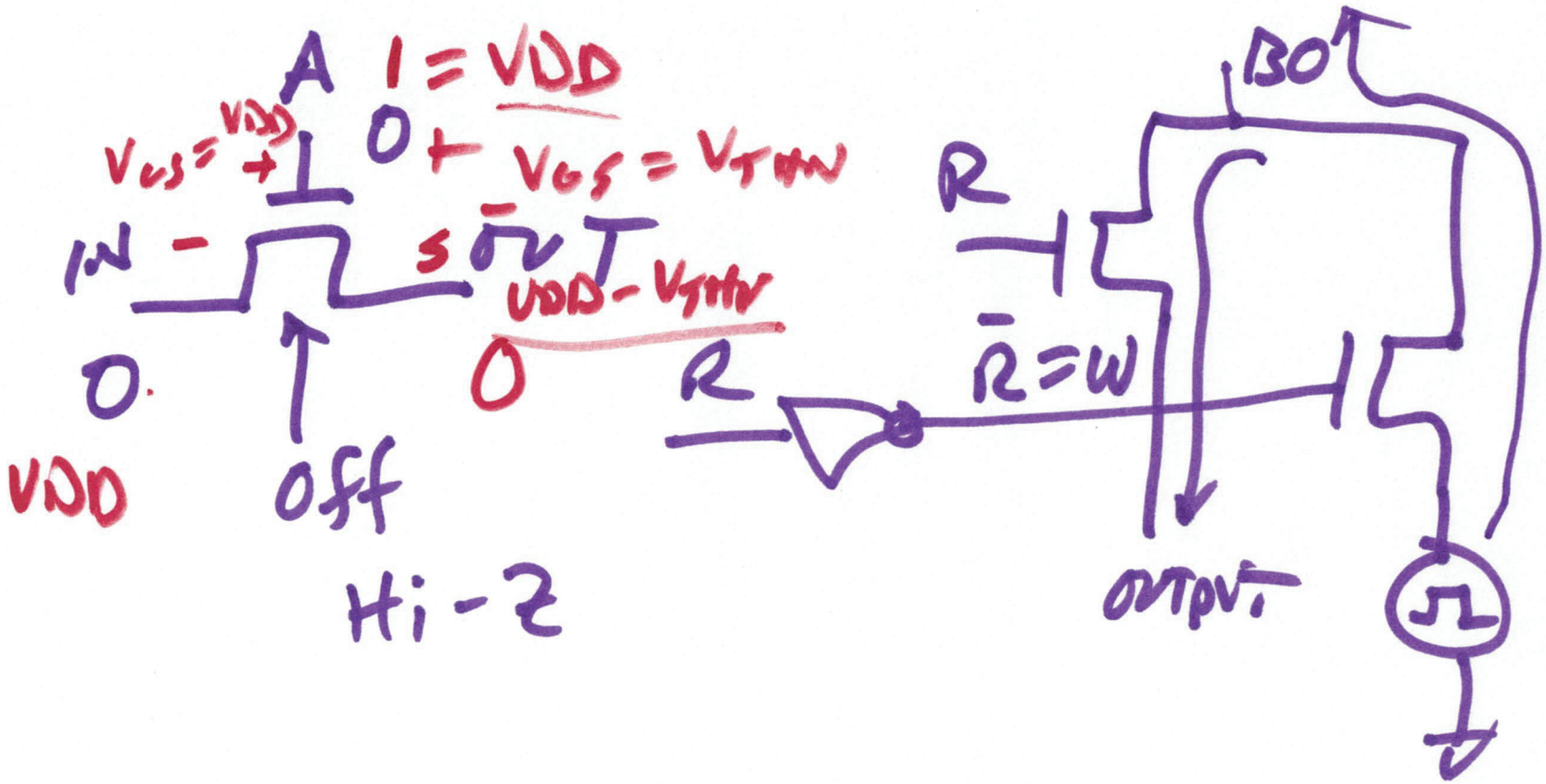
$= 700ps$

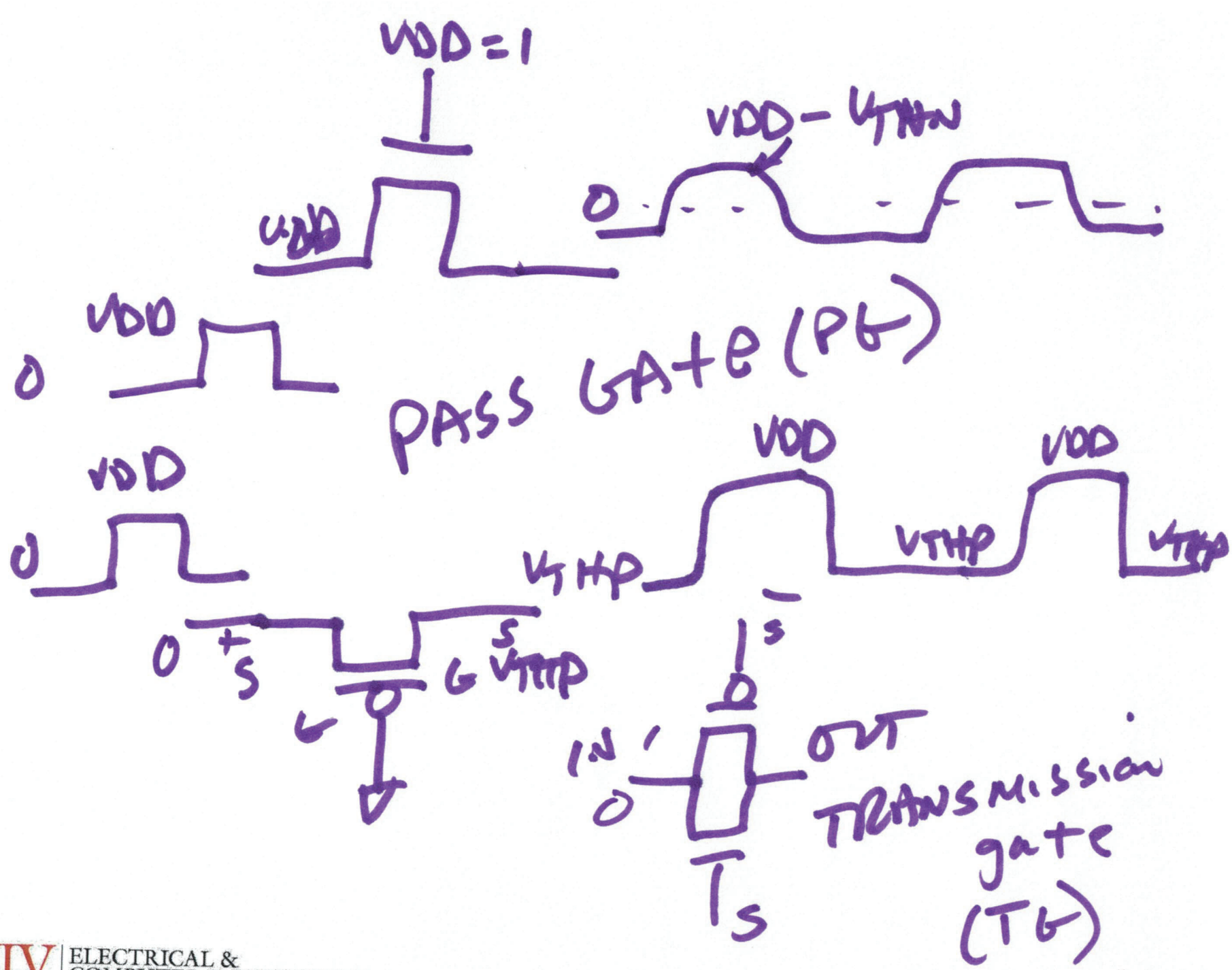
$1400ps$

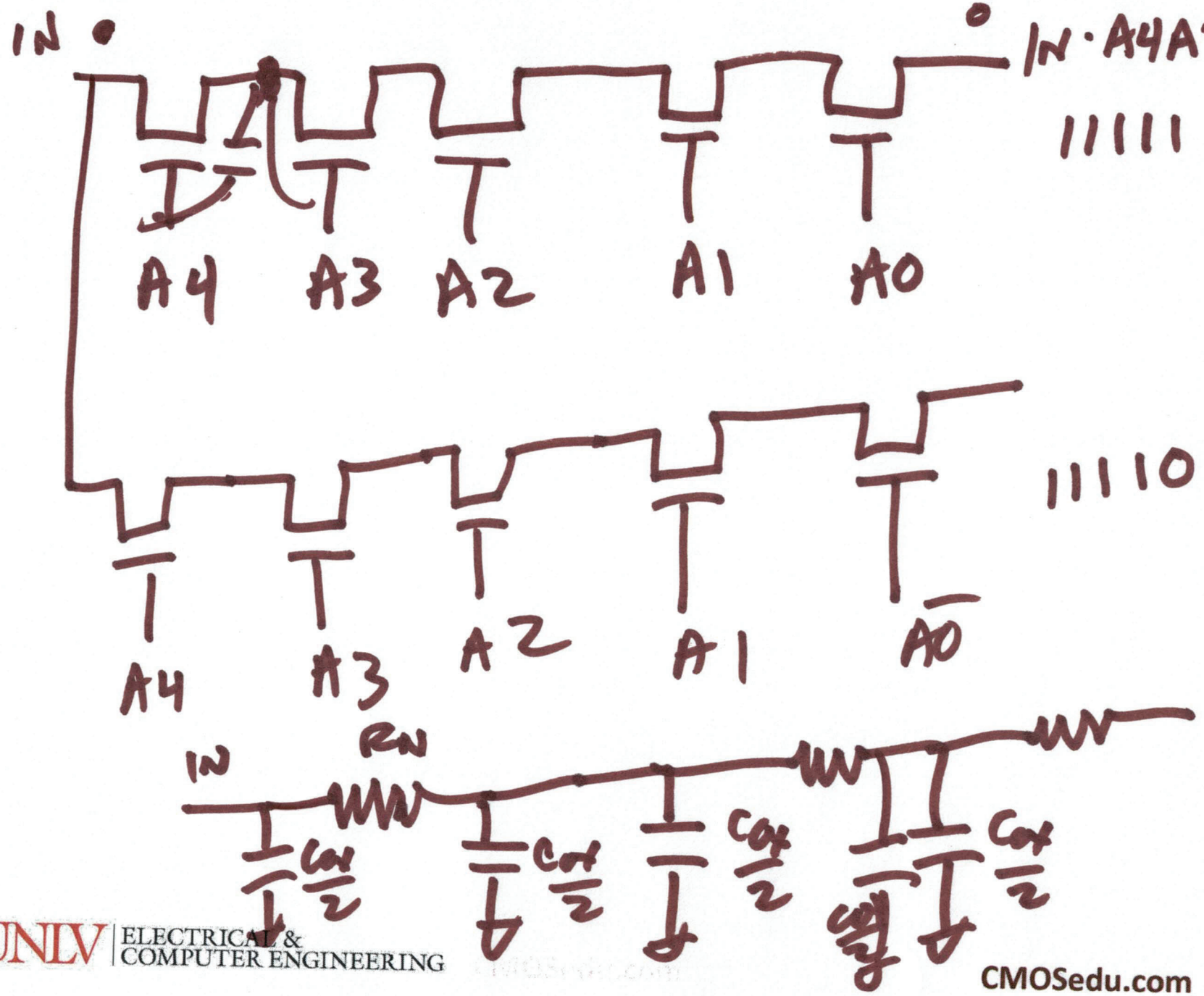
$= 1.4ns$

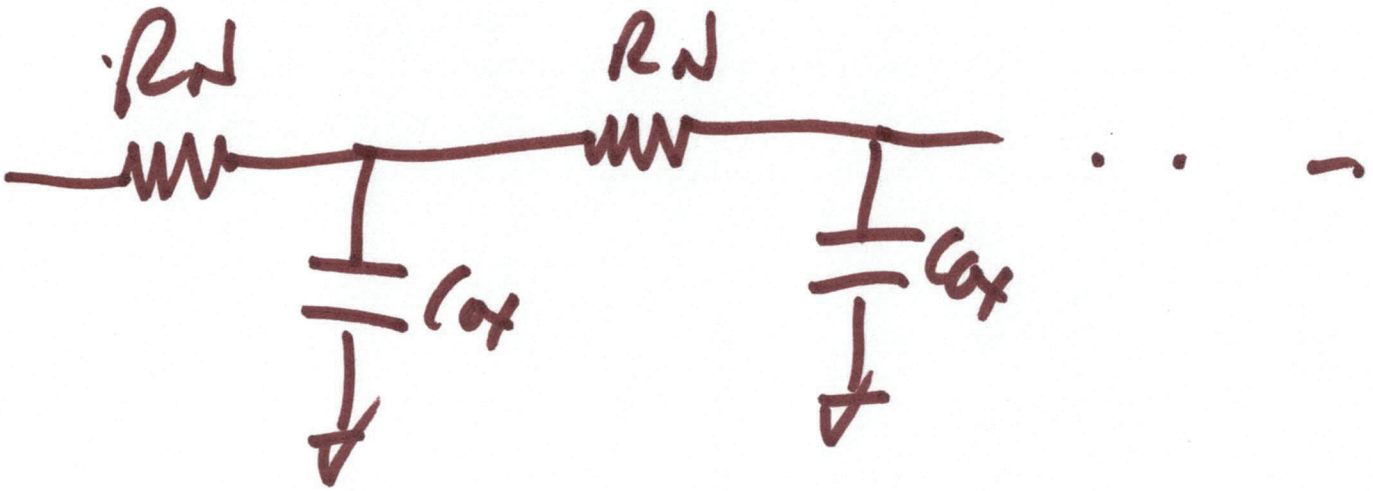
✓

21

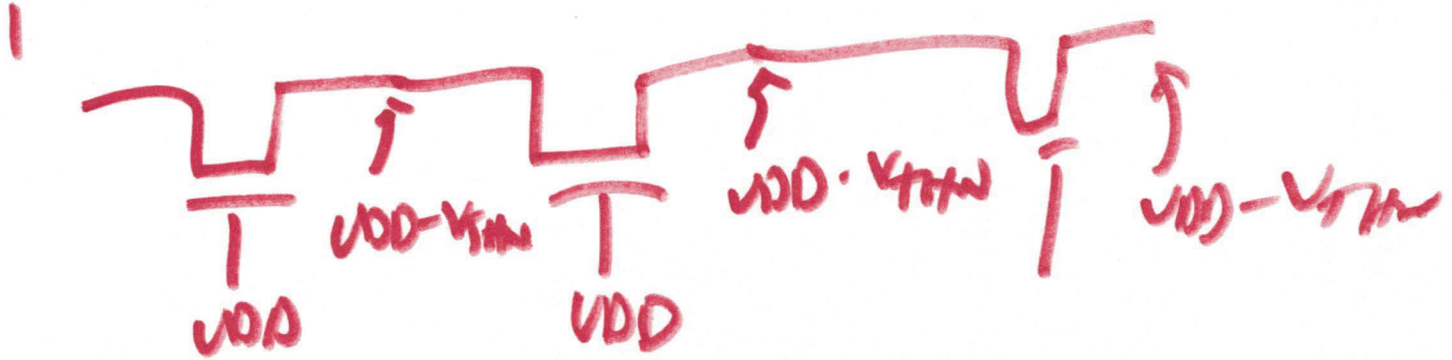

A
1 = VDD
0 +
VGS = VDD
VGS = VTHN
IN
S
VDD - VTHN
0
0
R
R̄ = W
R
VDD
off
Hi-Z
BO
OUTPUT

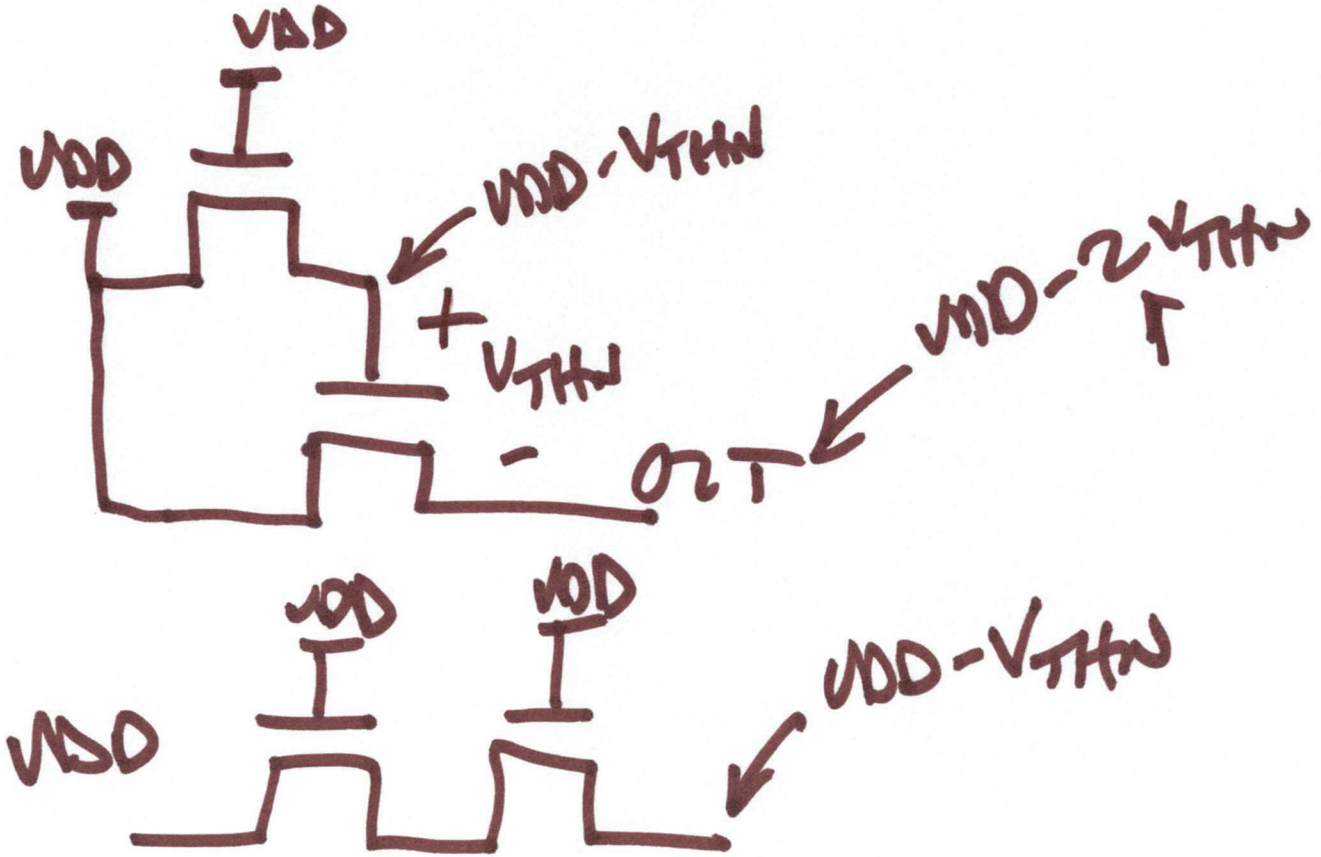

VDD=1
VDD
0
VDD - VTHN
VDD
0
PASS GATE (PG)
VDD
0
VDD
VTHP
VDD
VTHP
VTHP
0
+
S
G
S
VTHP
S
IN
OUT
0
TRANSMISSION
gate
(TG)
TS


IN
IN·A4A3·A2A1
11111
A4
A3
A2
A1
A0
11110
A4
A3
A2
A1
A0
IN
RN
Cox/2
Cox
Cox/2
Cox
Cox/2
Cgd
Cox/2

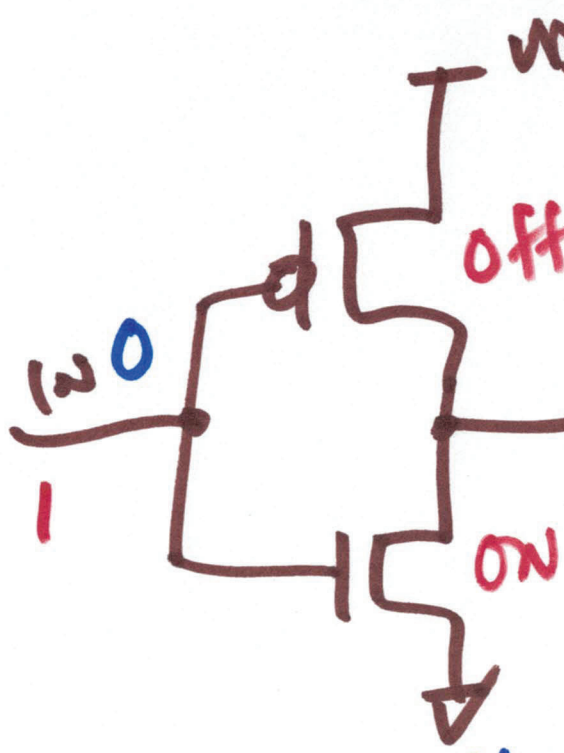


$$t_d = 0.35 \cdot R_N \cdot C_{OX} \cdot \ell^2$$




VDD
VDD
VDD - VTHN
+
VTHN
-
VDD - 2VTHN
VDD
VDD
VDD
VDD - VTHN

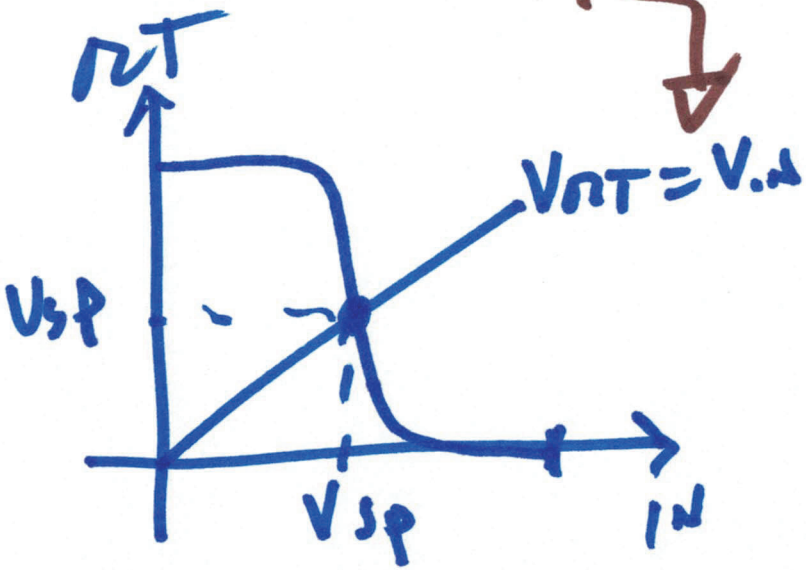
Inverter

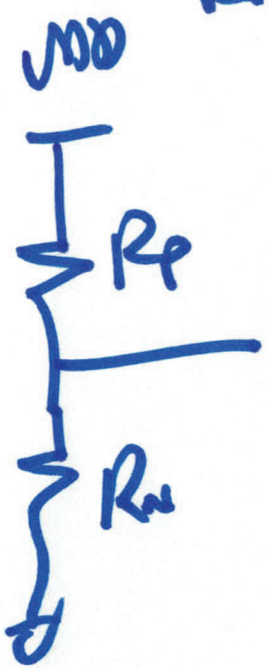


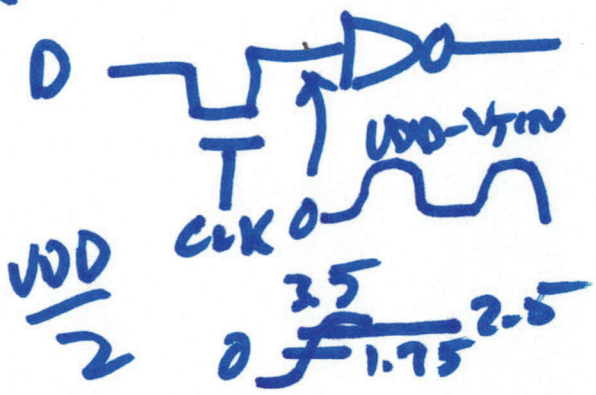
$R_p = R_p' \cdot \frac{L_p}{W_p}$

$\frac{.6}{12}$

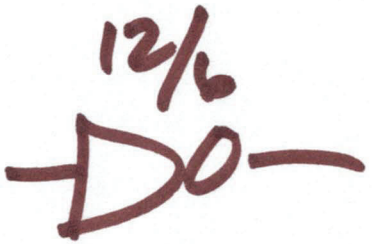
$R_n = R_n' \cdot \frac{L_n}{W_n} \rightarrow \frac{6}{6}$

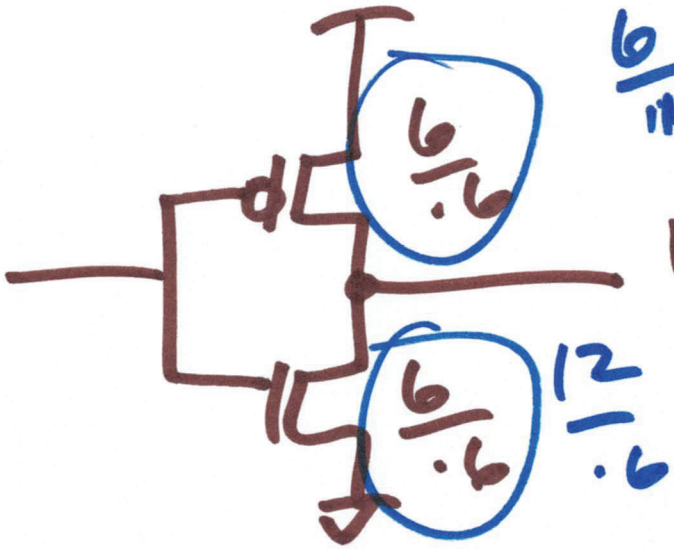




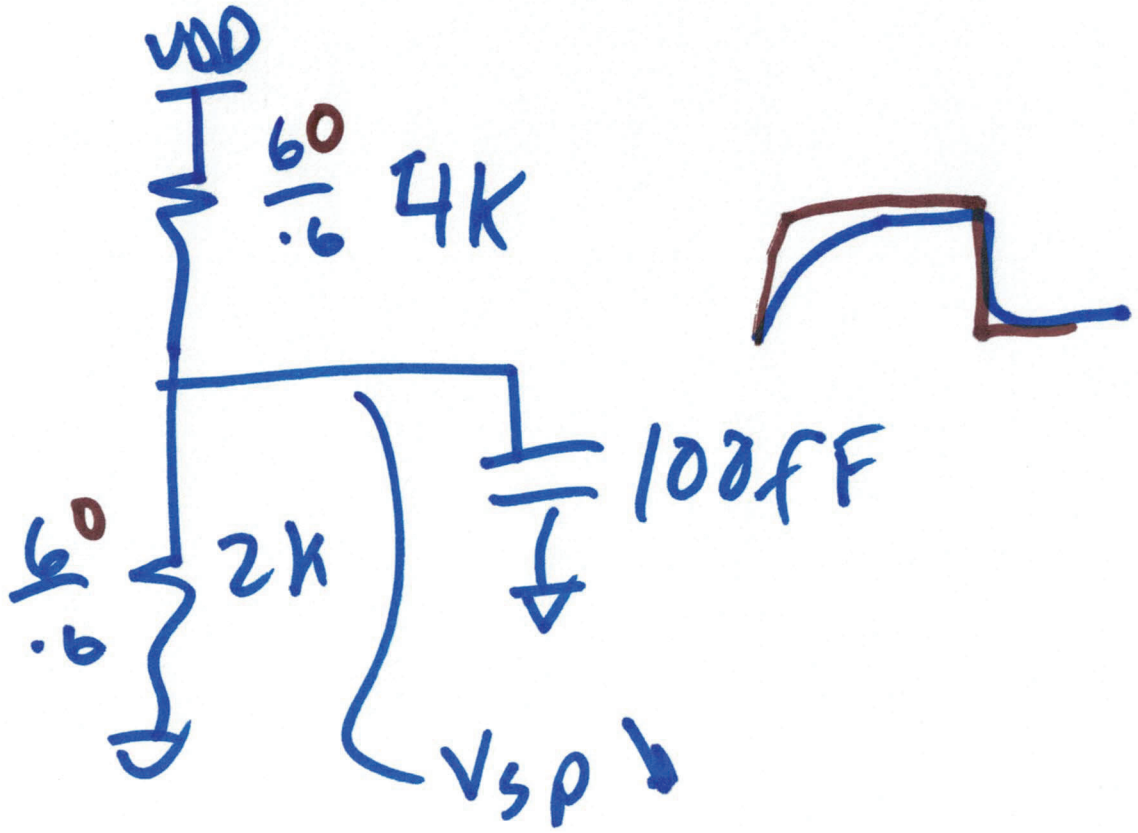


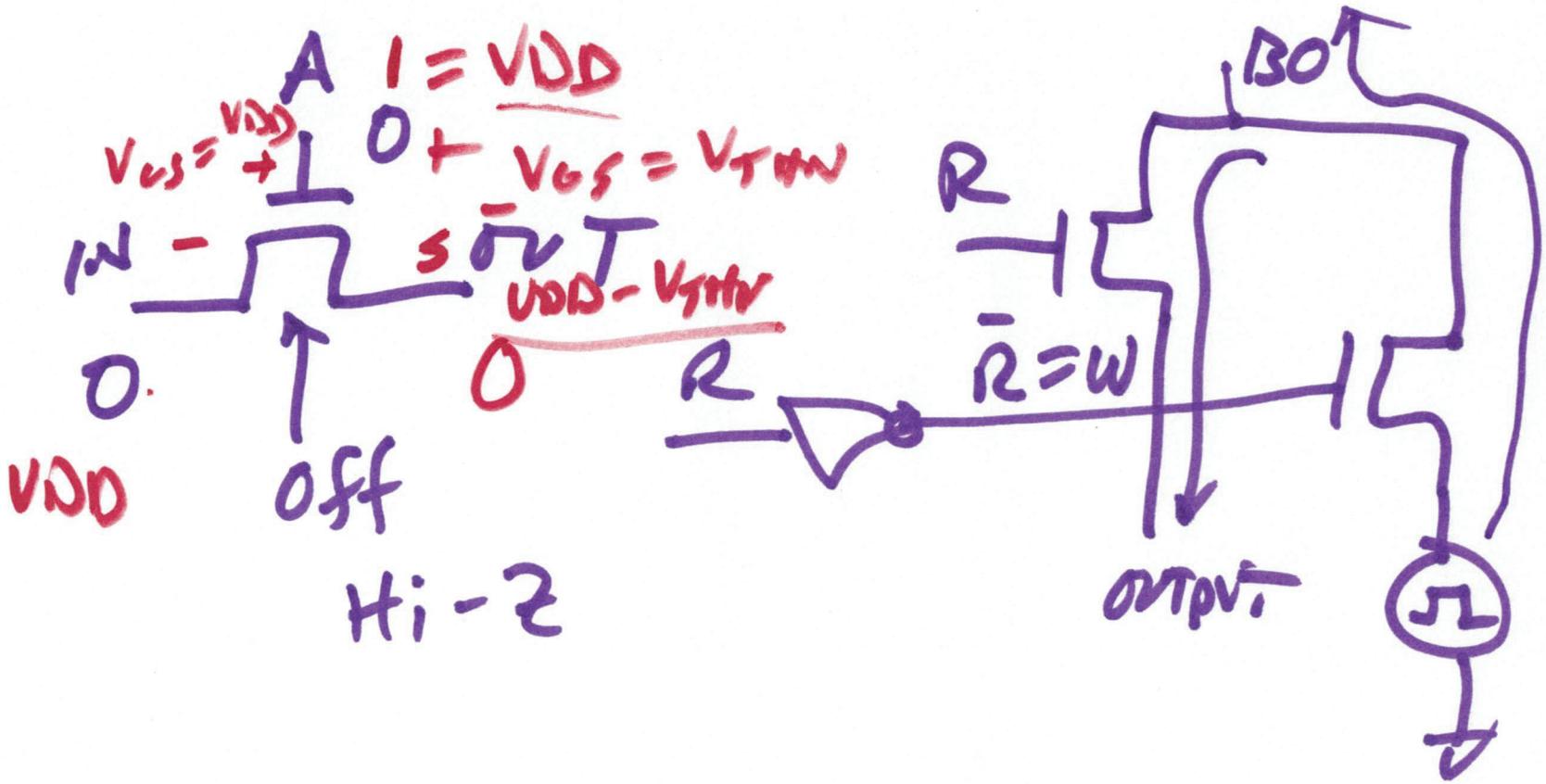
$V_{sp} \approx 2.5V$

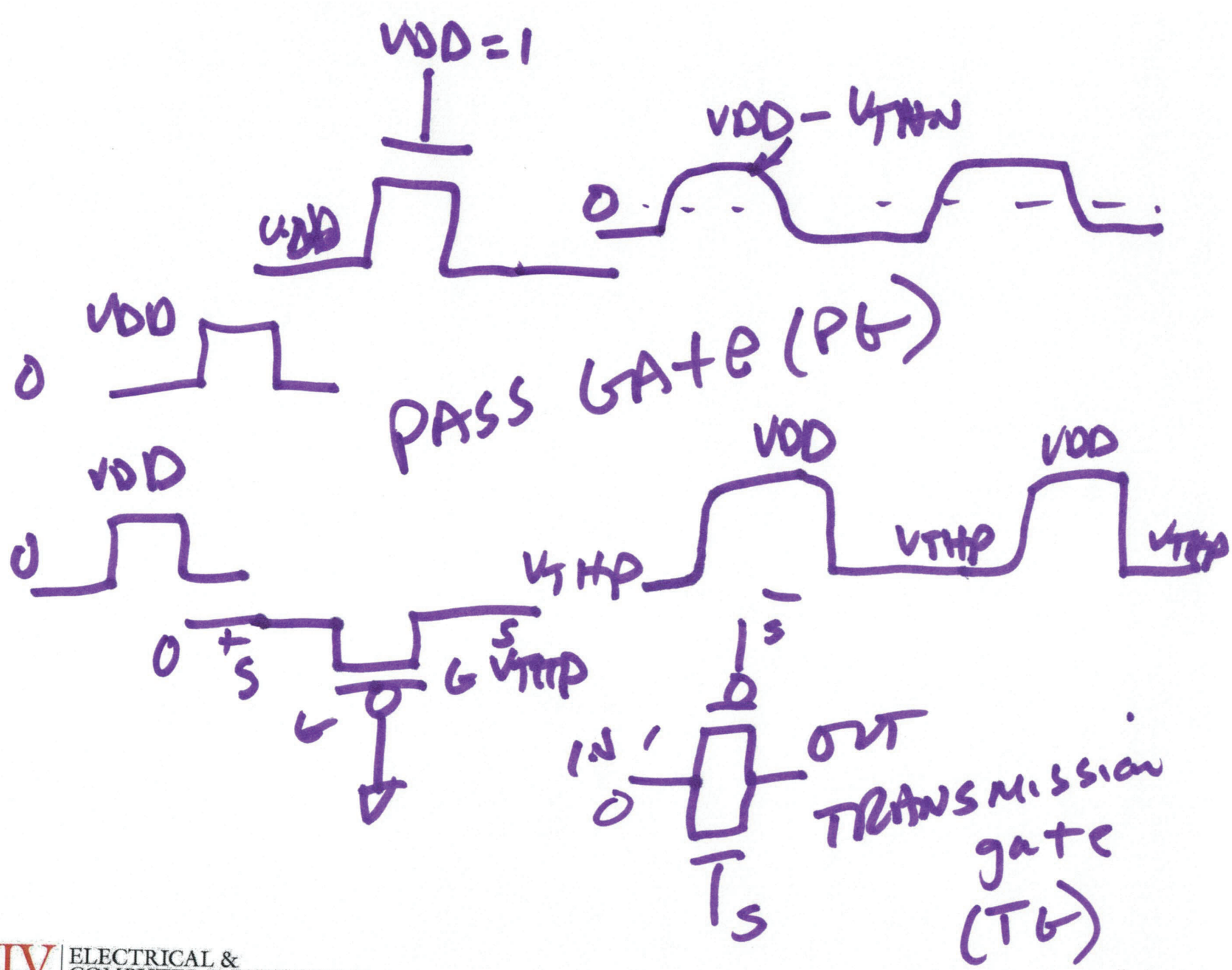


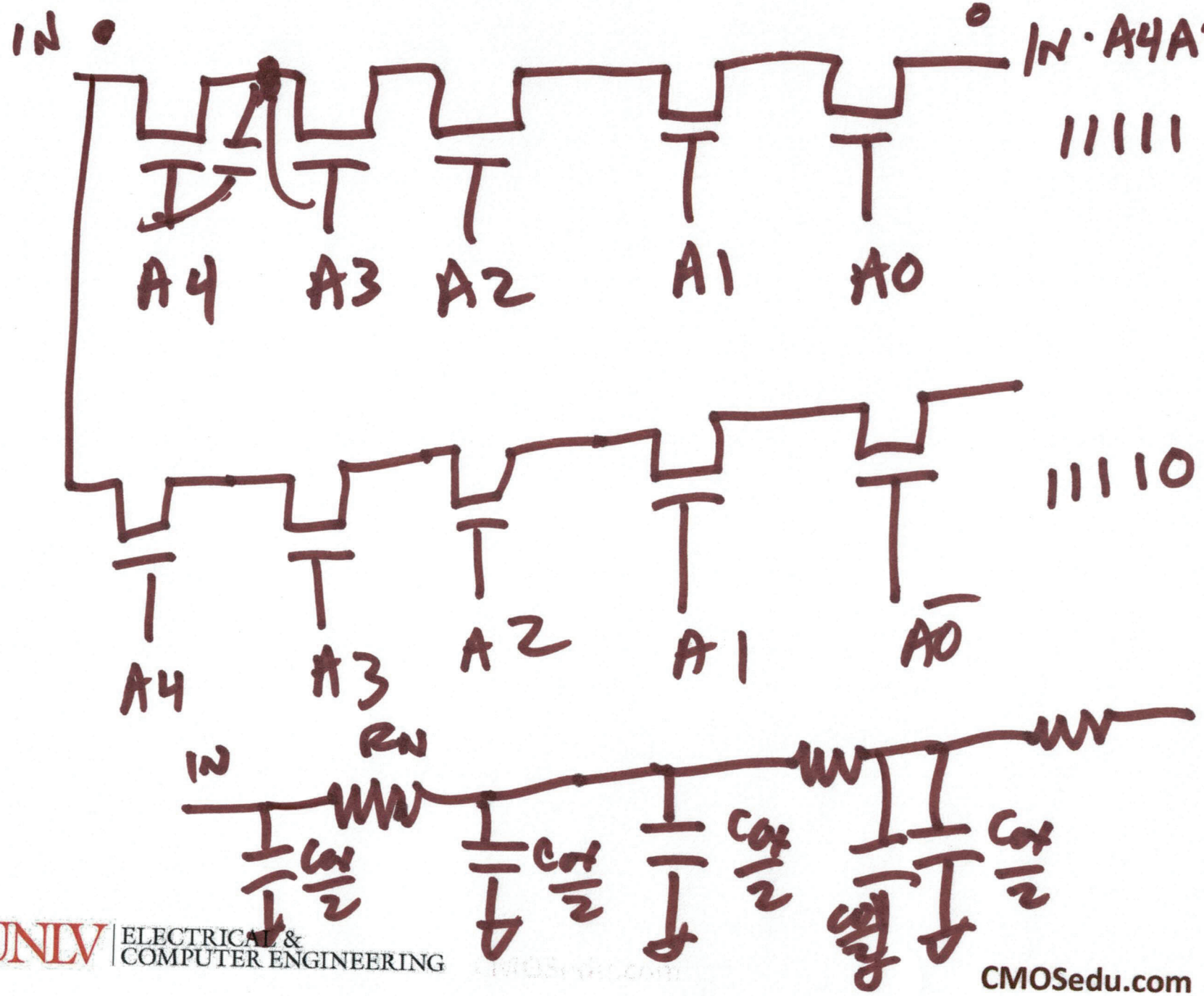


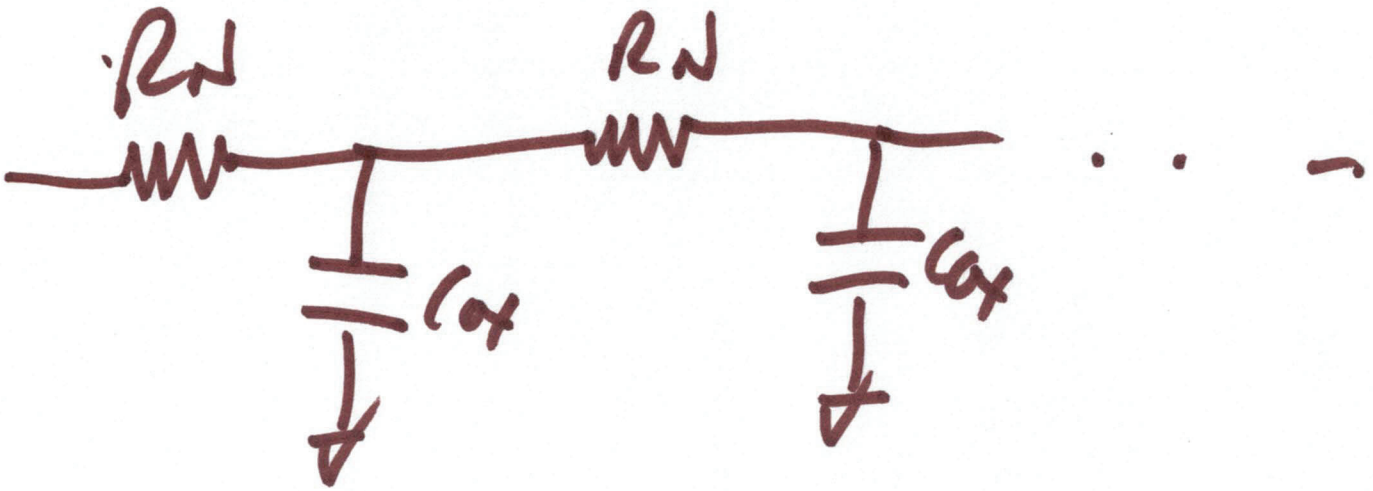
$U_{sp} \stackrel{?}{=} 2.2V$


VDD
60
.6
4K
100fF
60
.6
2K
Vsp


A
1 = VDD
0 +
VGS = VDD
VGS = VTHN
IN
S
VDD - VTHN
0
0
R
R̄ = W
R
VDD
off
Hi-Z
BO
OUTPUT


VDD=1
VDD
0
VDD - VTHN
VDD
0
PASS GATE (PG)
VDD
0
VDD
VTHP
VDD
VTHP
VTHP
0
+
S
G
S
VTHP
S
IN
OUT
0
TRANSMISSION
gate
(TG)
TS


IN
IN·A4A3·A2A1
11111
A4
A3
A2
A1
A0
11110
A4
A3
A2
A1
A0
IN
RN
Cox/2
Cox
Cox/2
Cox
Cox/2
Cgd
Cox/2



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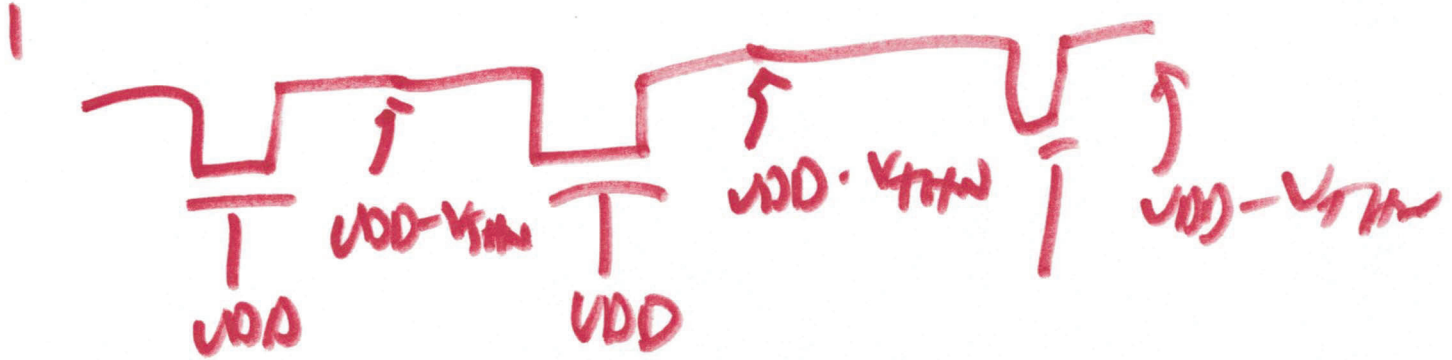
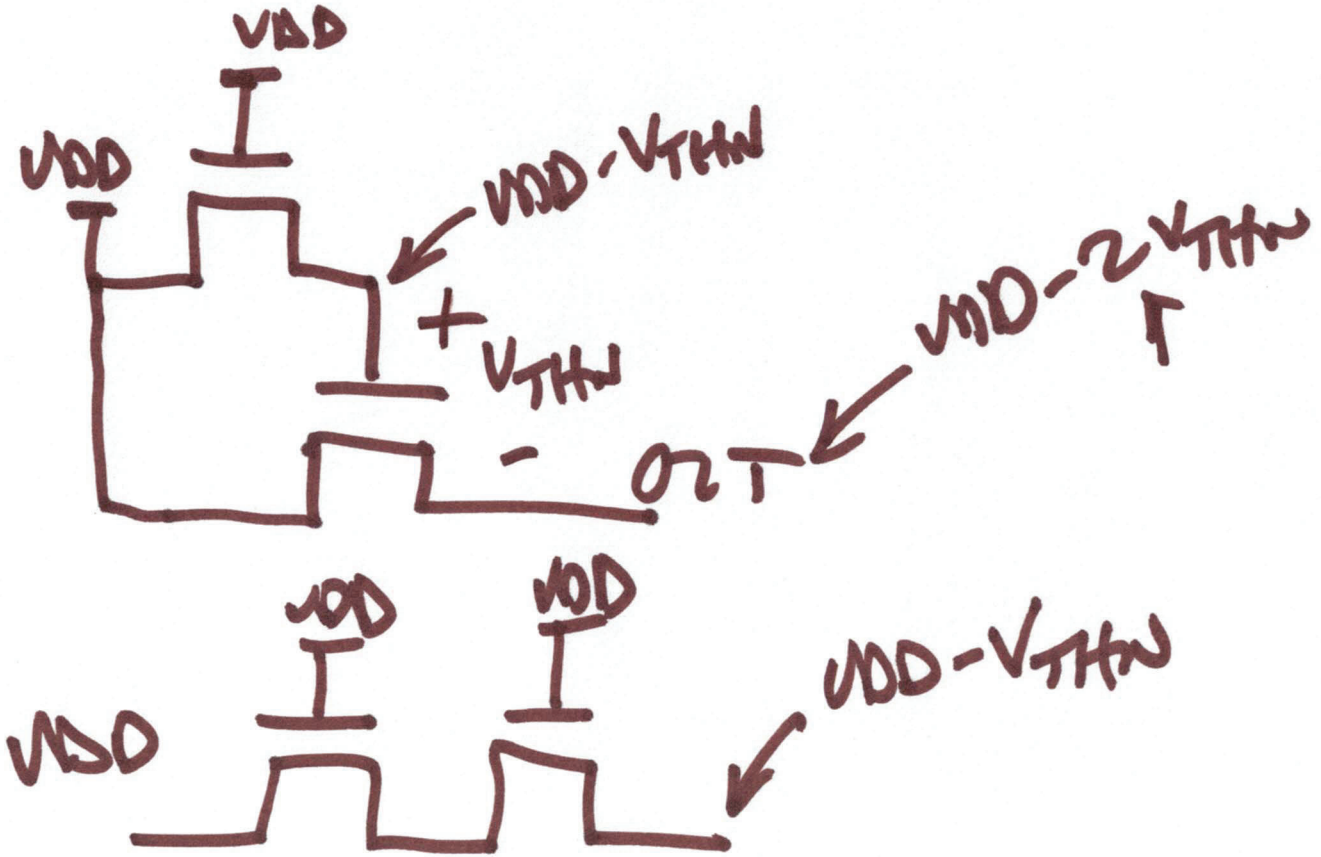
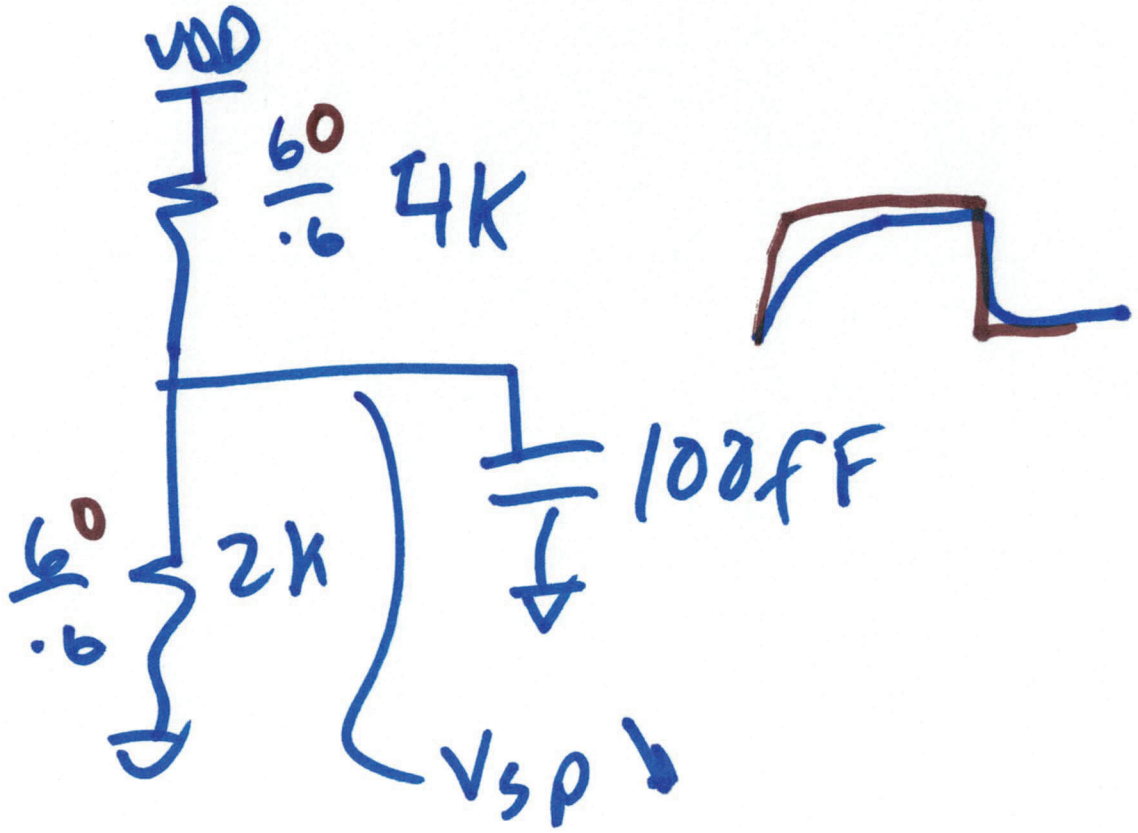



VDD
VDD
VDD - VTHN
+
VTHN
-
VDD - 2VTHN
VDD
VDD
VDD
VDD - VTHN


VDD
60
.6
4K
100fF
60
.6
2K
Vsp