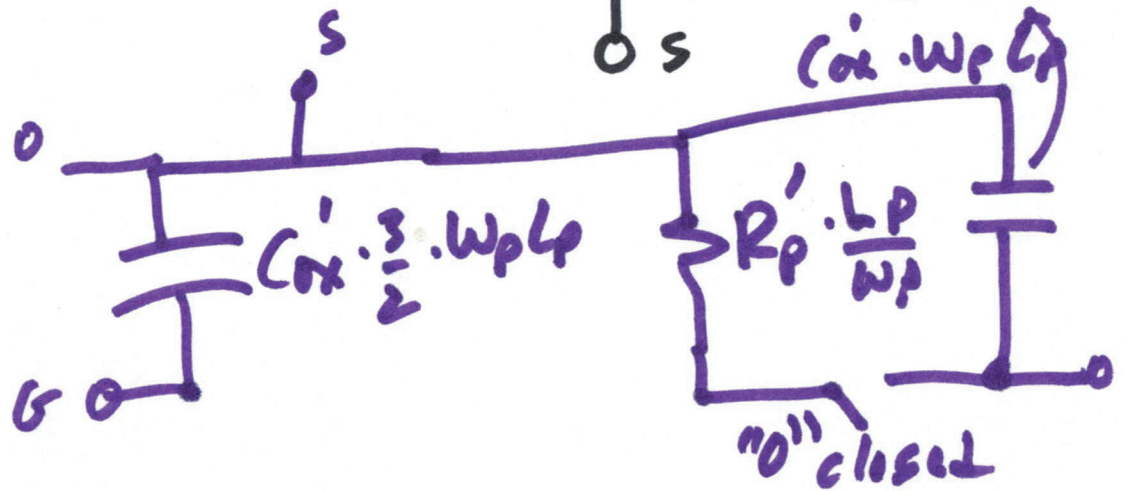
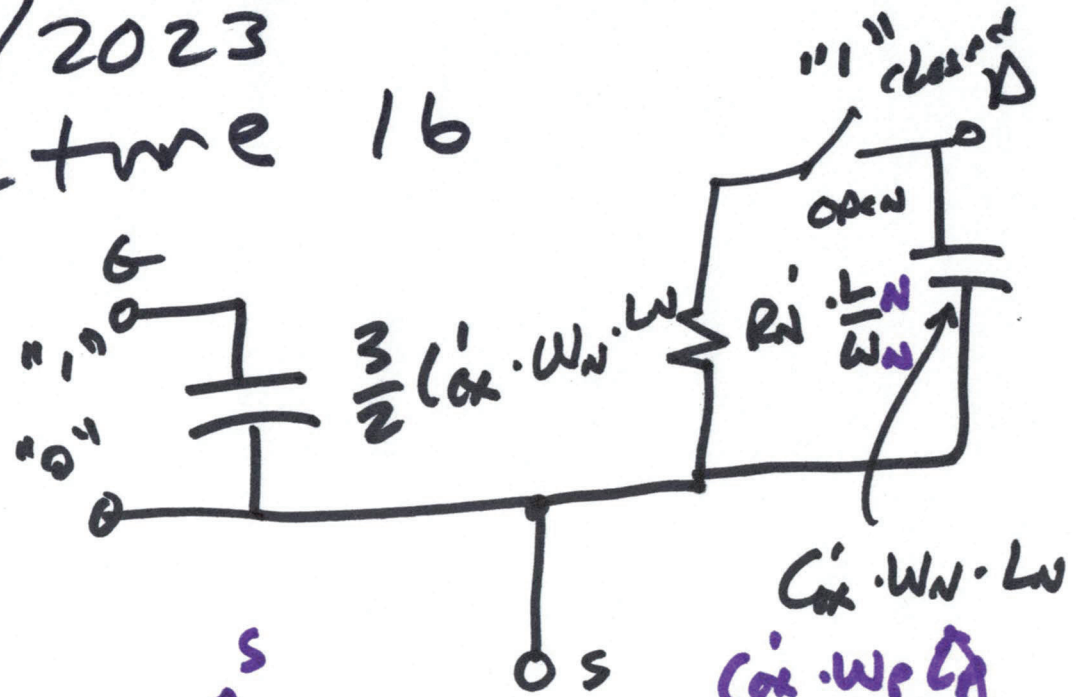
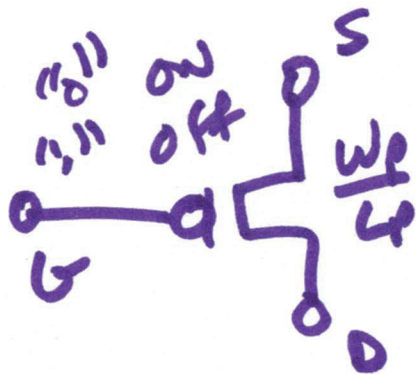
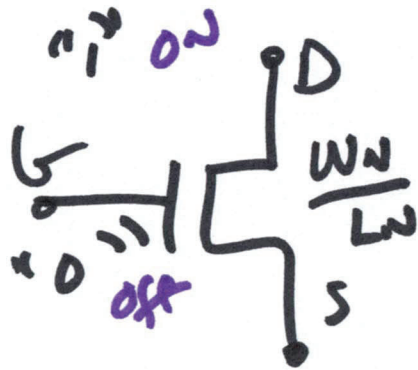


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# Digital IC Design

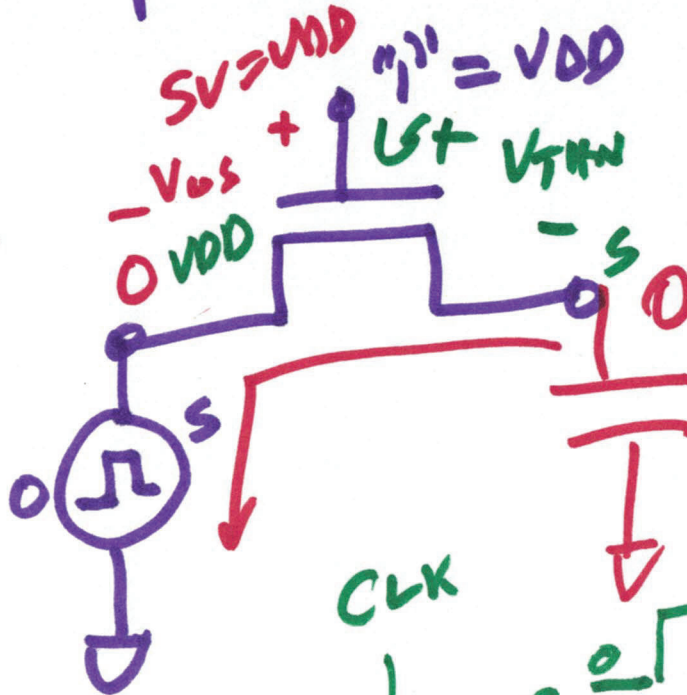
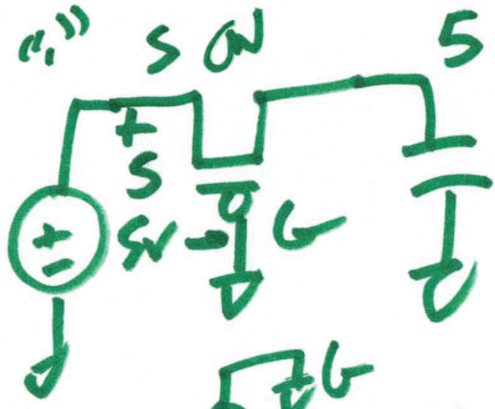
10/25/2023

## Lecture 16

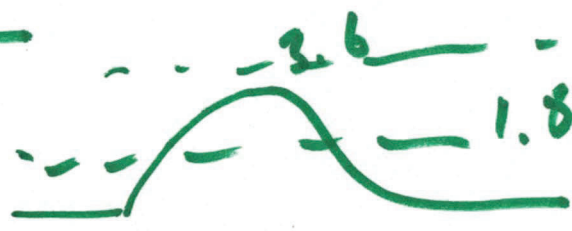
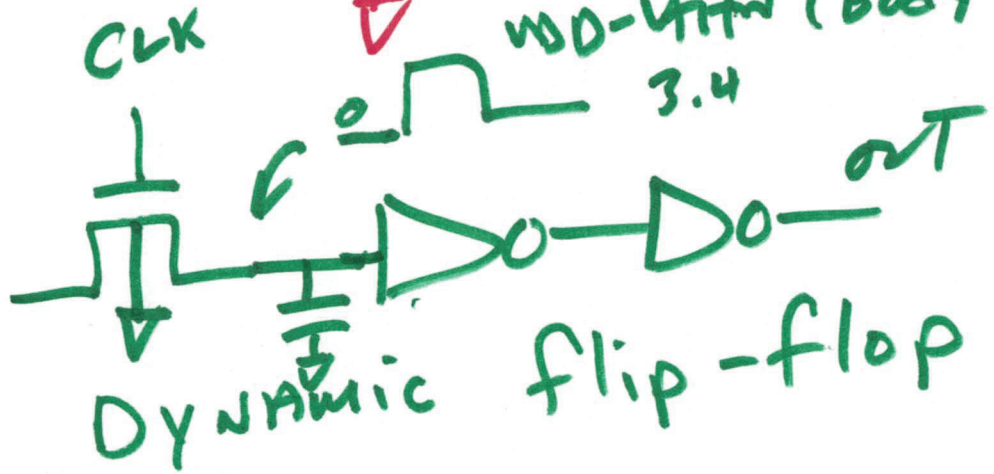
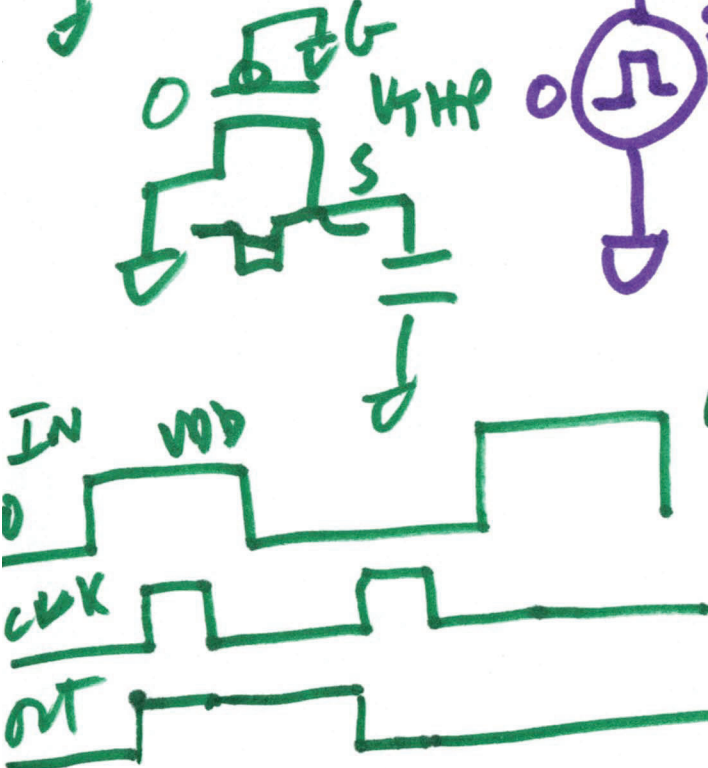


# Pass GATES (PG)

pmos → "1" well

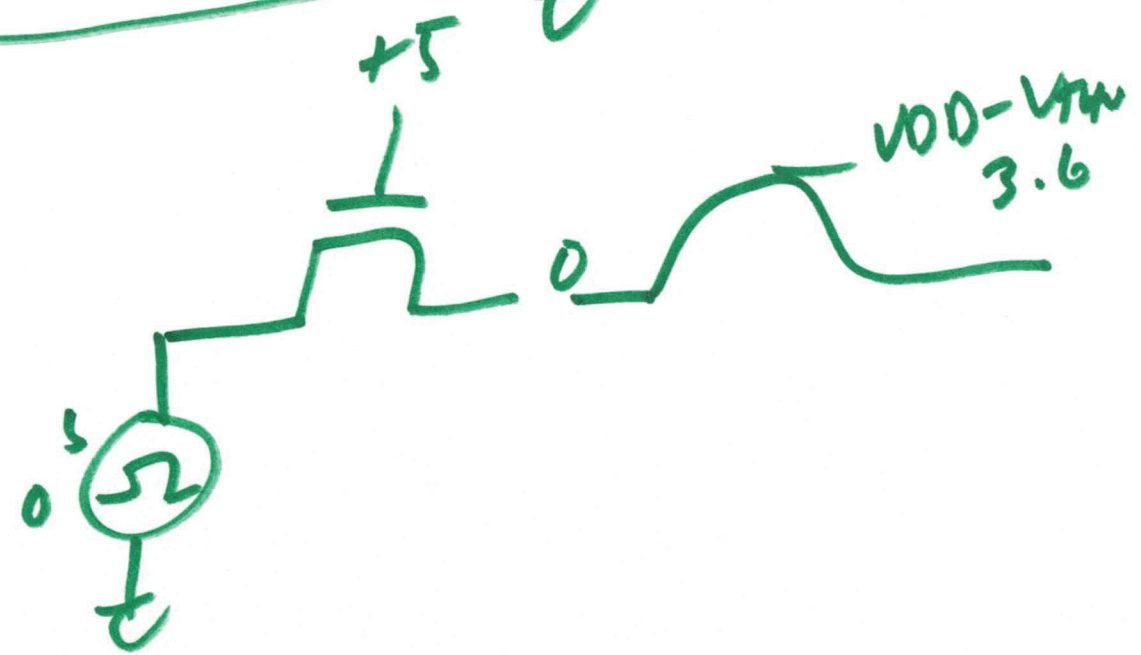
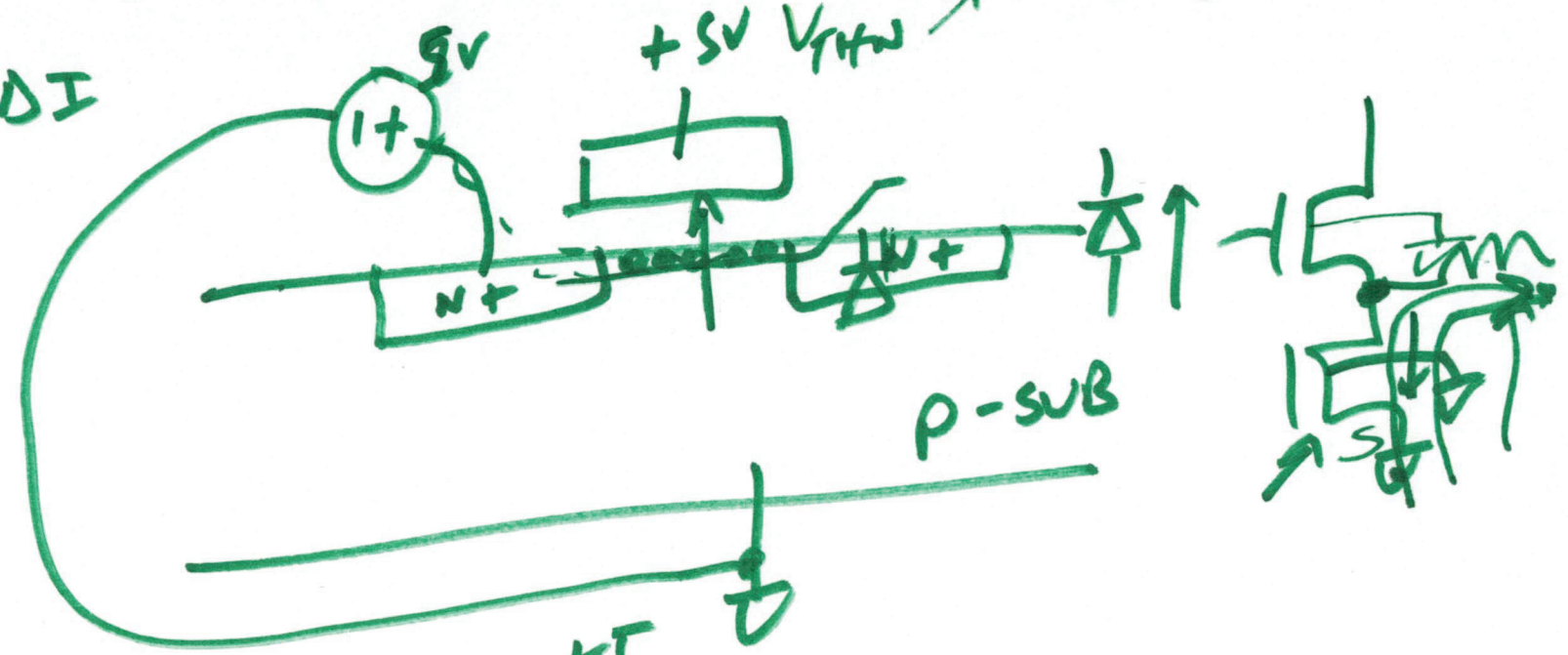


NMOS doesn't pass a "1" good; pass a "0" good; (Body effect)

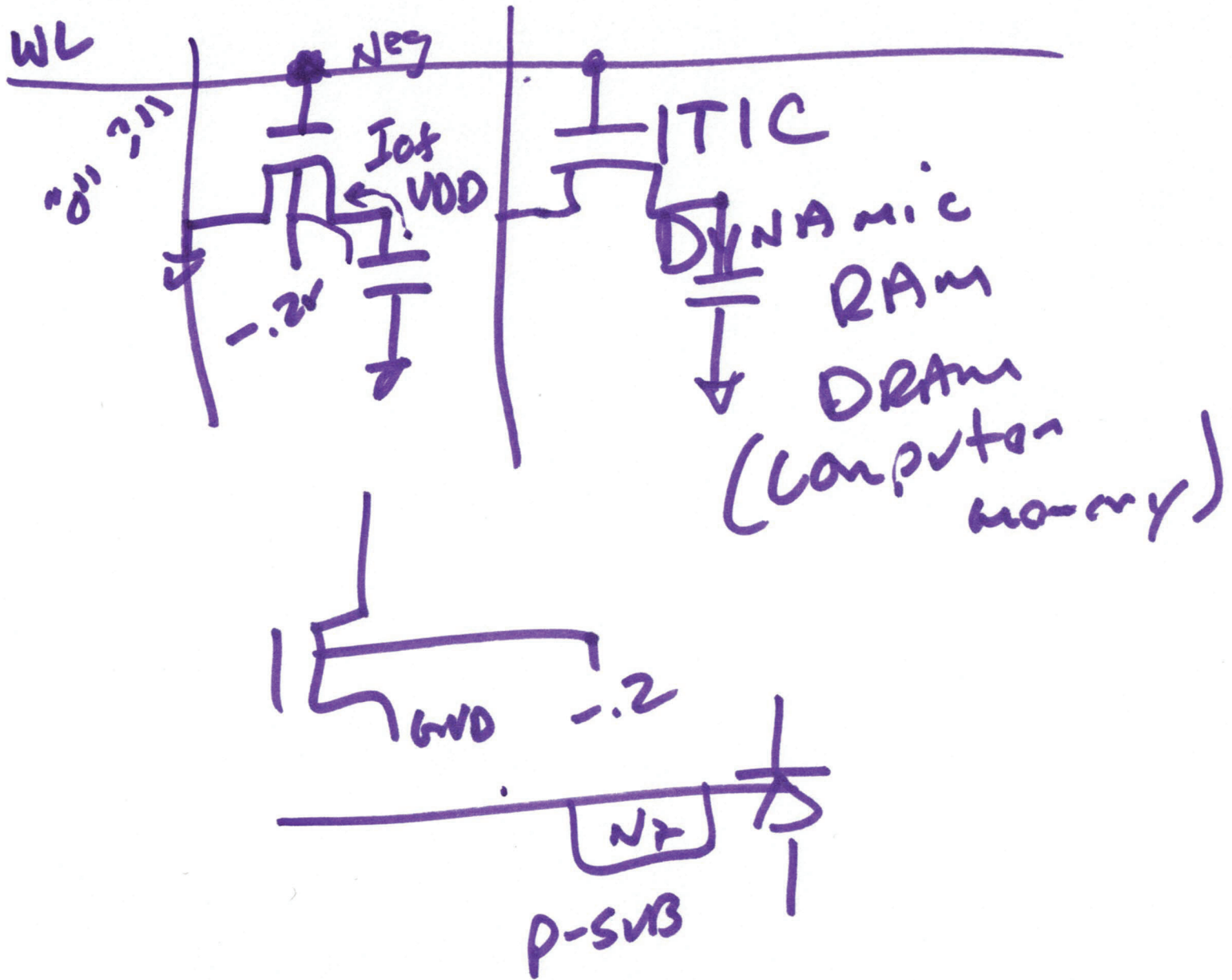


2)

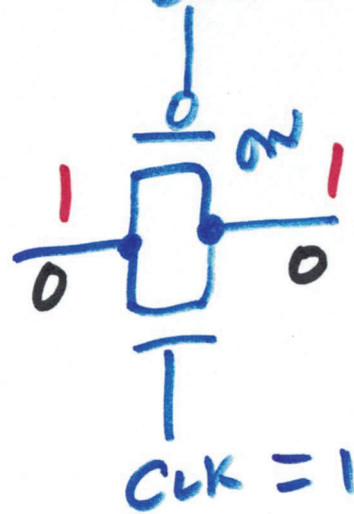
Body effect  $\rightarrow V_{TH} \uparrow$



3)



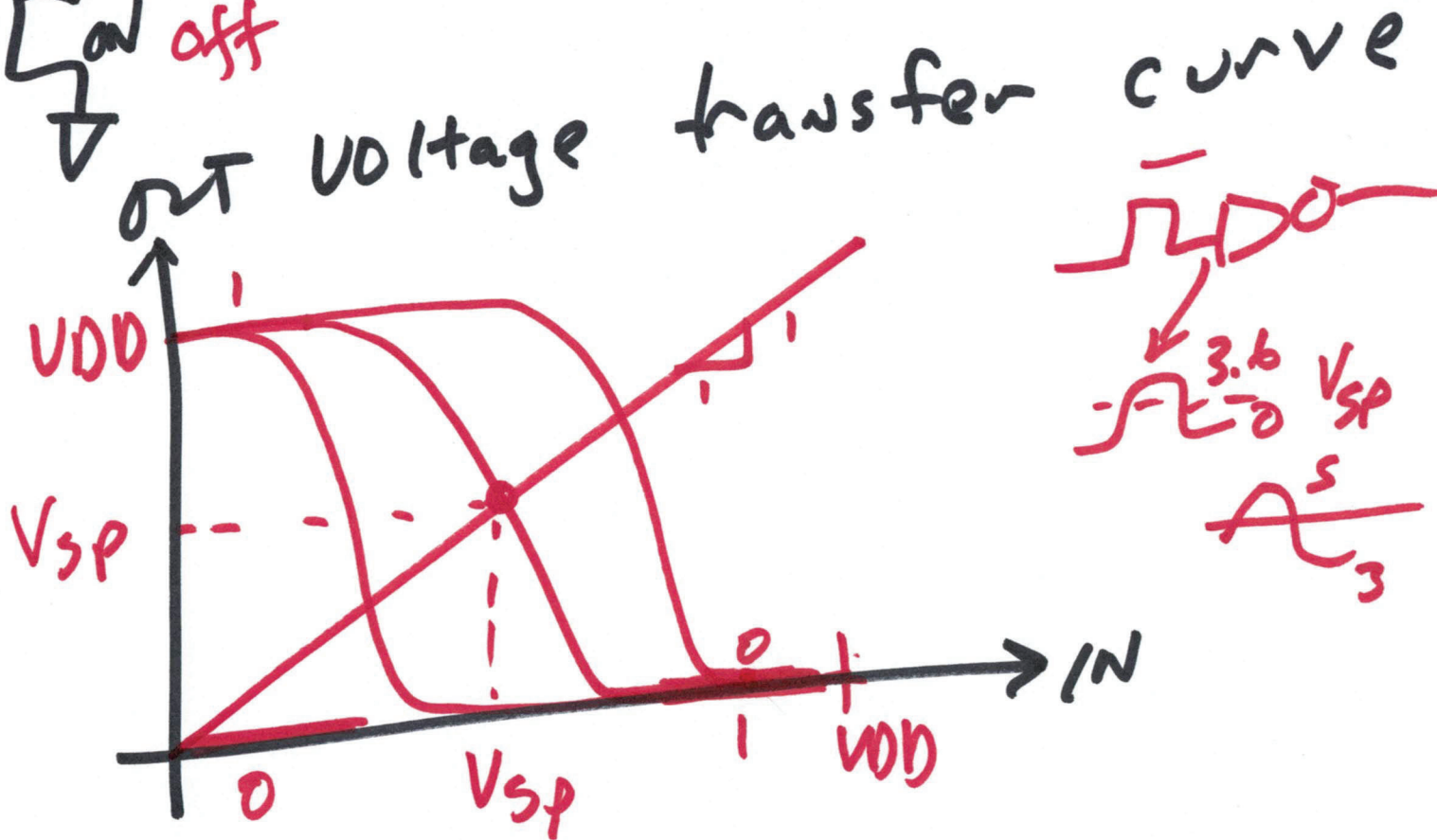
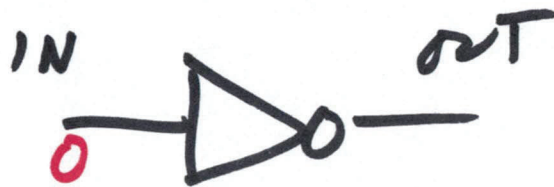
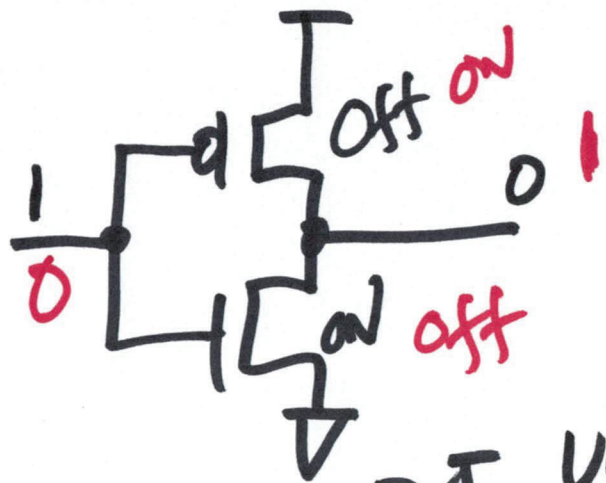
# TRANSMISSION Gate (TG)



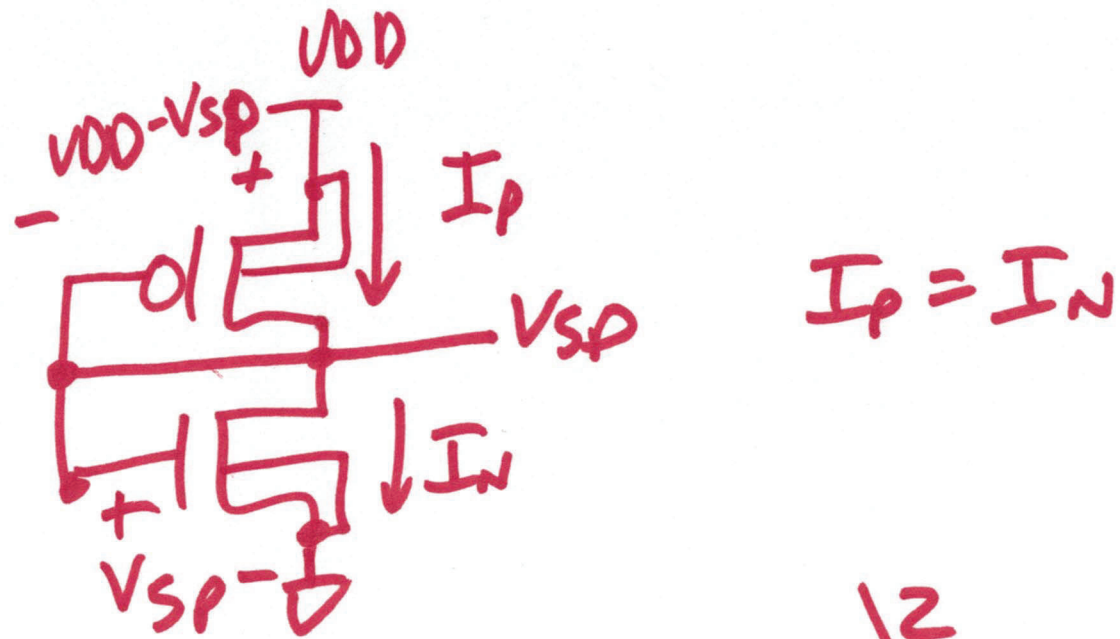
more layout  
Area

2 clocks  
instead of  
1

# Inverter



b)



$$\frac{K_{Pp}}{2} \cdot \frac{W_p}{L_p} (V_{DD} - V_{sp} - V_{thp})^2 = \frac{K_{Pn}}{2} \cdot \frac{W_n}{L_n} (V_{sp} - V_{thn})^2$$