

A17.1 & A17.2

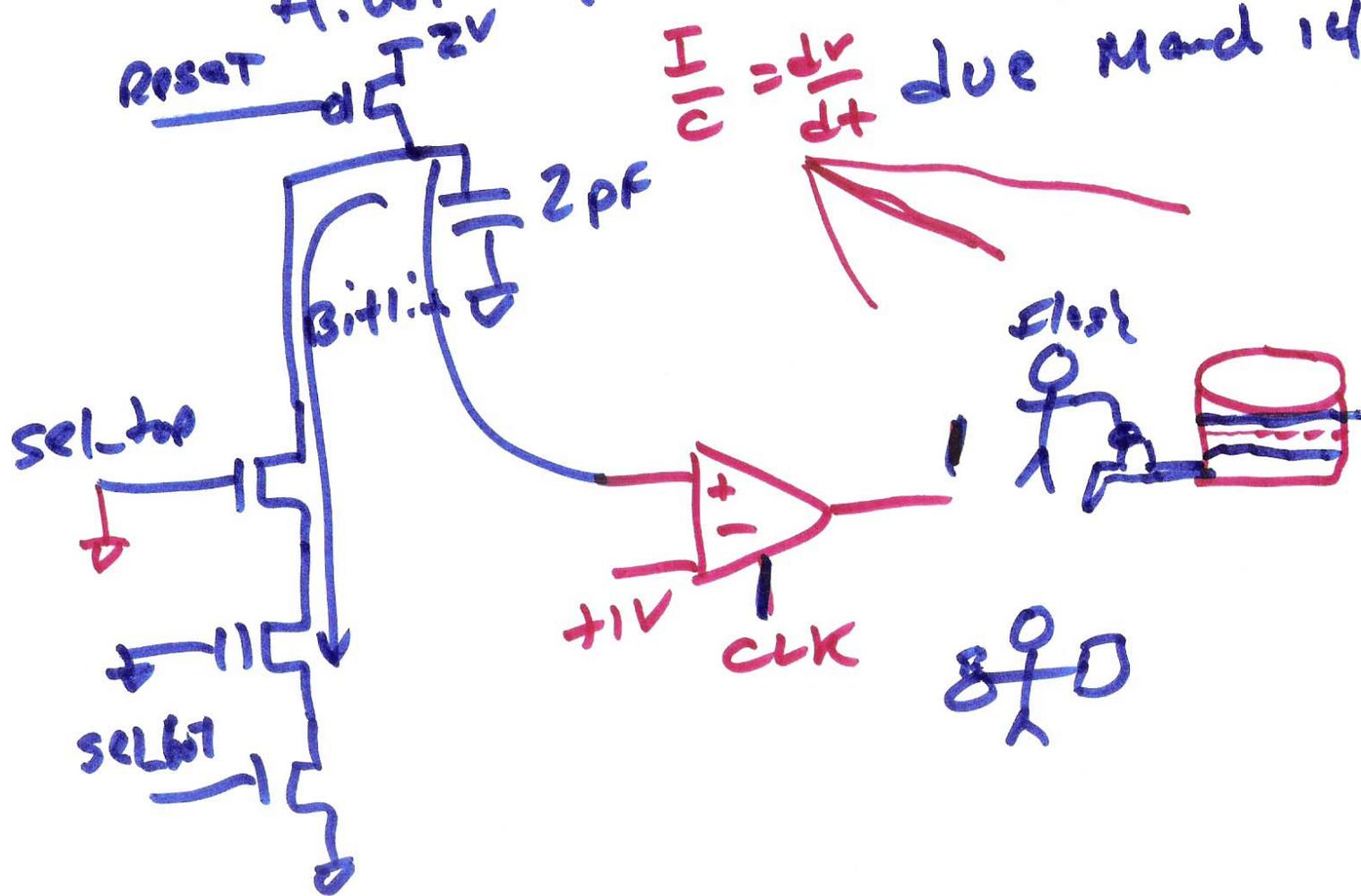
Lecture 13, March 7, 2011

ECE 5/418 memory ckt design

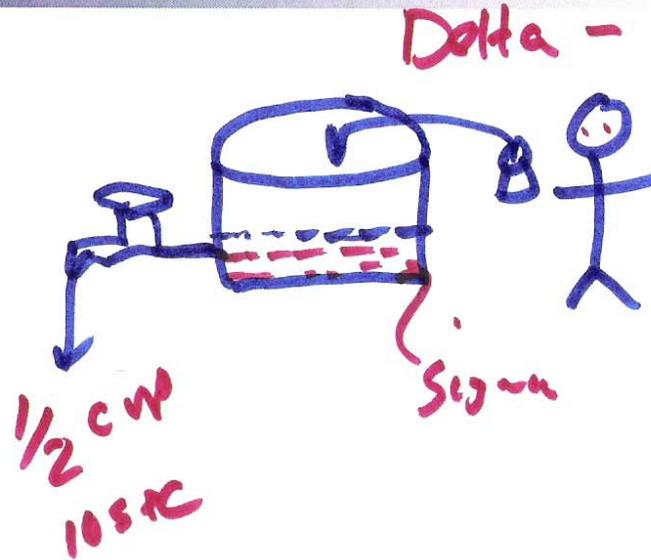
H.W. # 10

A17.1 & A17.2

$I/C = \frac{dv}{dt}$ due March 14



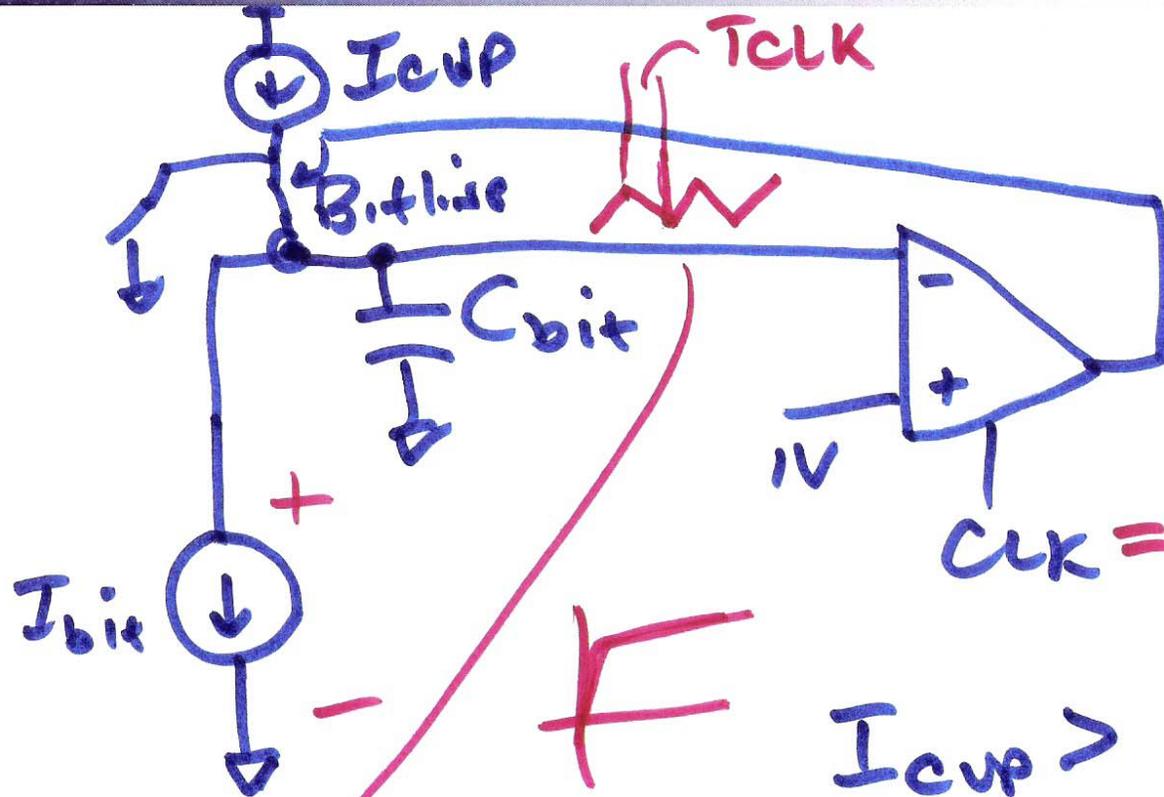
1)



time	ADD
0	1
10	0
20	1
30	0
40	0
50	1
60	1

1 cup $\cdot \frac{50}{100}$ 100

2)



$$\frac{dV}{dt} \cdot \Delta T_{CLK} = \Delta V$$

$$CLK = f_{CLK} = \frac{1}{T_{CLK}}$$

$$I_{cup} > I_{bit}$$

$$\Delta V_{bit}|_{max} = \frac{I_{bit} \cdot T_{CLK}}{C_{bit}} \text{ OR}$$

$$\frac{I_{cup} \cdot T_{CLK}}{C_{bit}}$$

N = total # of times we clock the cap.

M = # of output high times $\frac{M}{N} \cdot I_{cup} = I_{bit}$

3)

$$I_{cup} \cdot \frac{M}{N} = I_{bit}$$

$$104 \cdot \frac{50}{100} = 5.4$$

$$\text{Resolution} = .14$$

$$= \frac{104}{100} = \frac{I_{cup}}{N} I_{bit} = 5.14A$$

$$\text{Res.} = \frac{I_{cup}}{N}$$

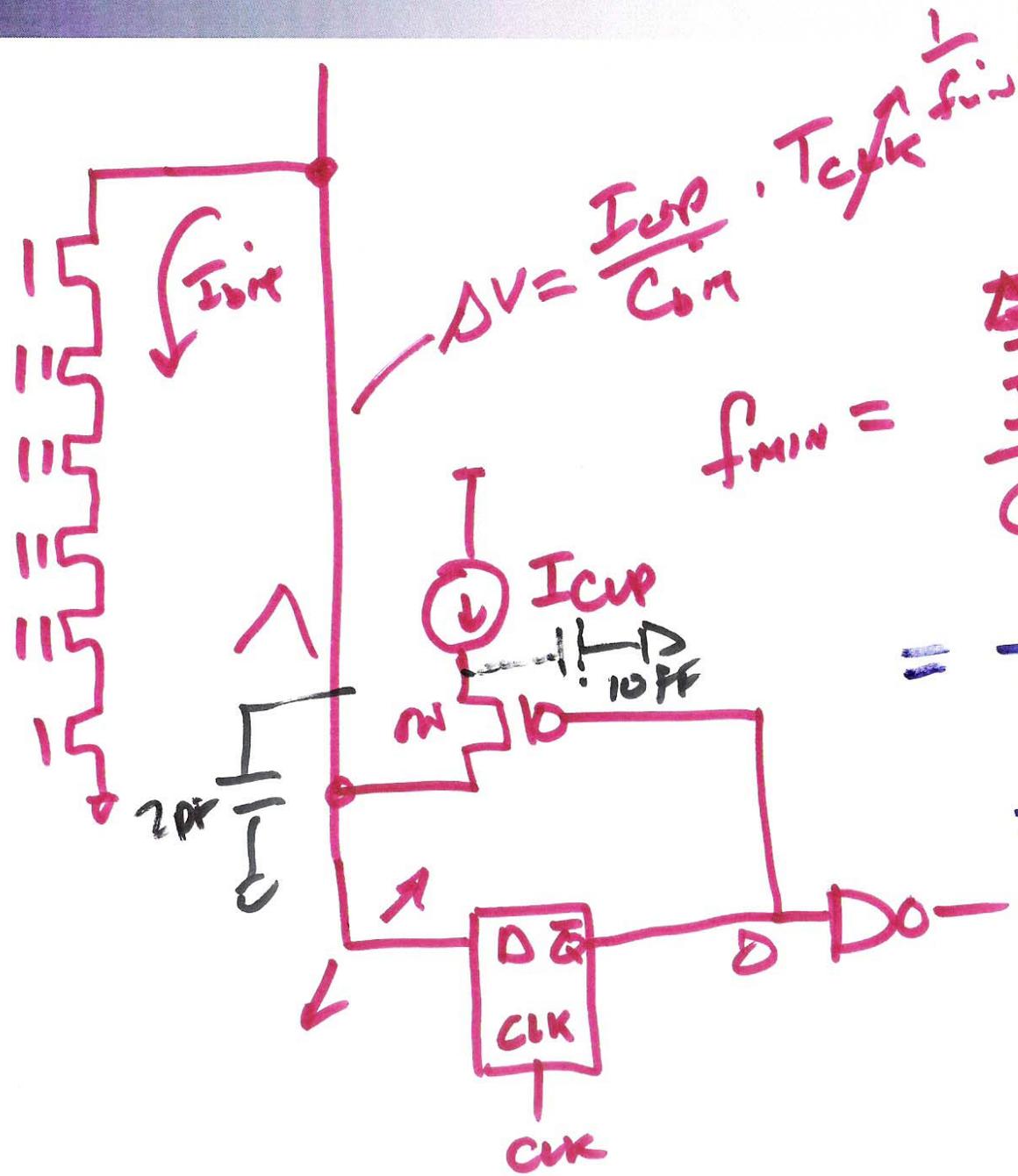
$$N = 100,$$

$$I_{cup} = 104A$$

$$I_{bit} = 54A$$

$$M = 50$$

4)



$$\Delta V = \frac{I_{CUP} \cdot T_{CYCLE}}{C_{bit}}$$

$$f_{min} = \frac{I_{CUP}}{C_{bit} \cdot \Delta V_{MAX}}$$

$$= \frac{104}{2pF \cdot 250mV}$$

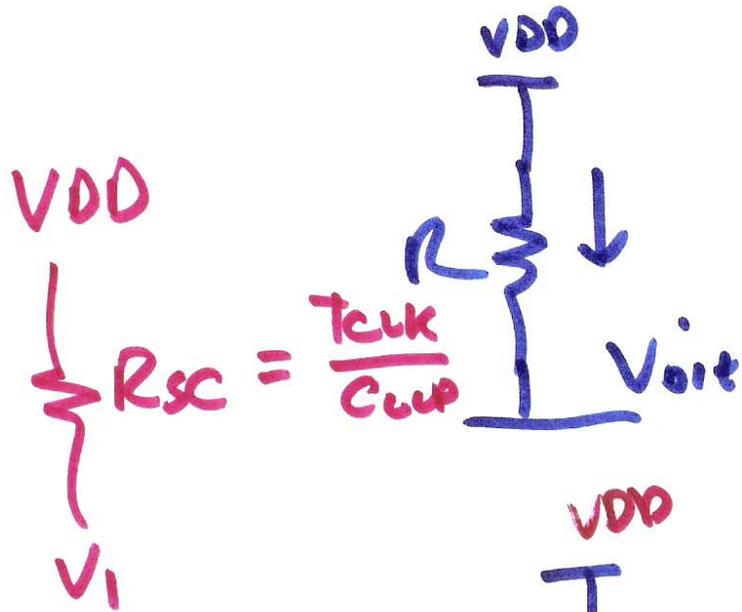
$$= \frac{10}{500} \cdot 10^9$$

$$= \frac{1}{50} \cdot 10^9$$

$$= \underline{\underline{20 MHz}}$$

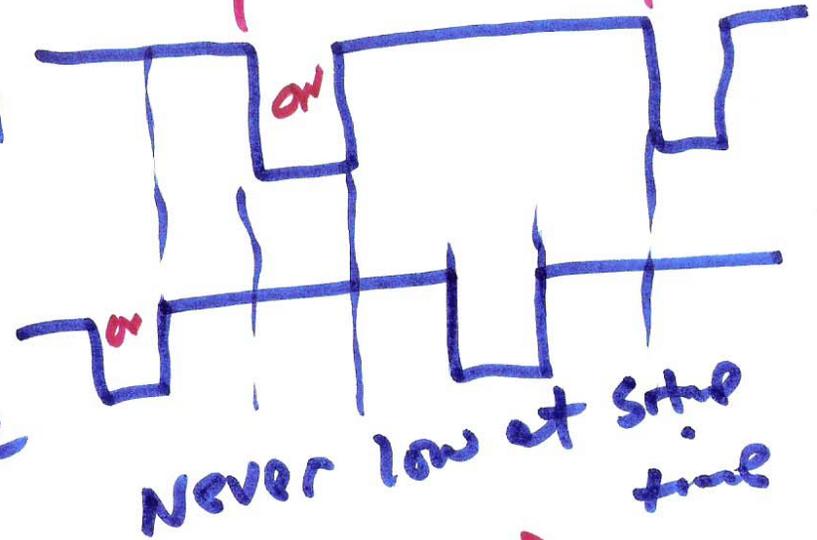
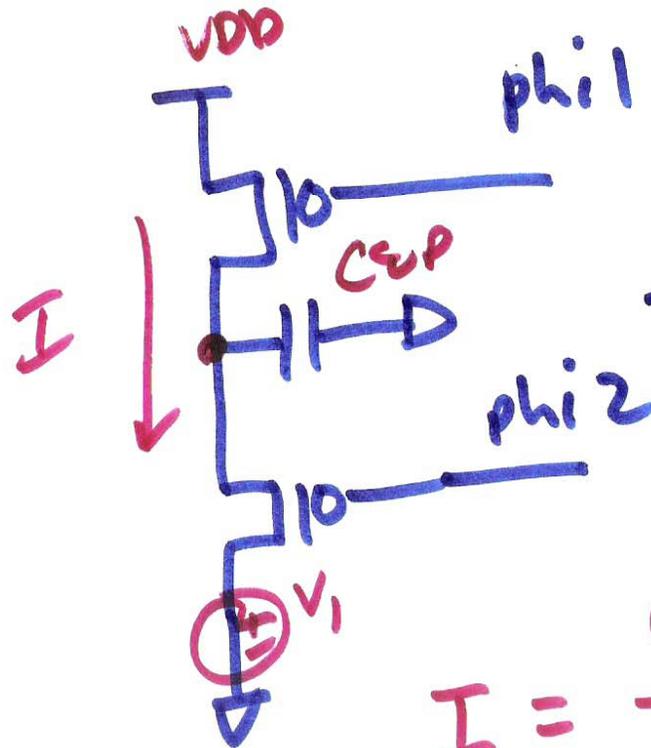
5)

$$I = \frac{V_{DD} - V_{iit}}{R}$$



$$= \frac{1}{f_{clk} T_{clk}}$$

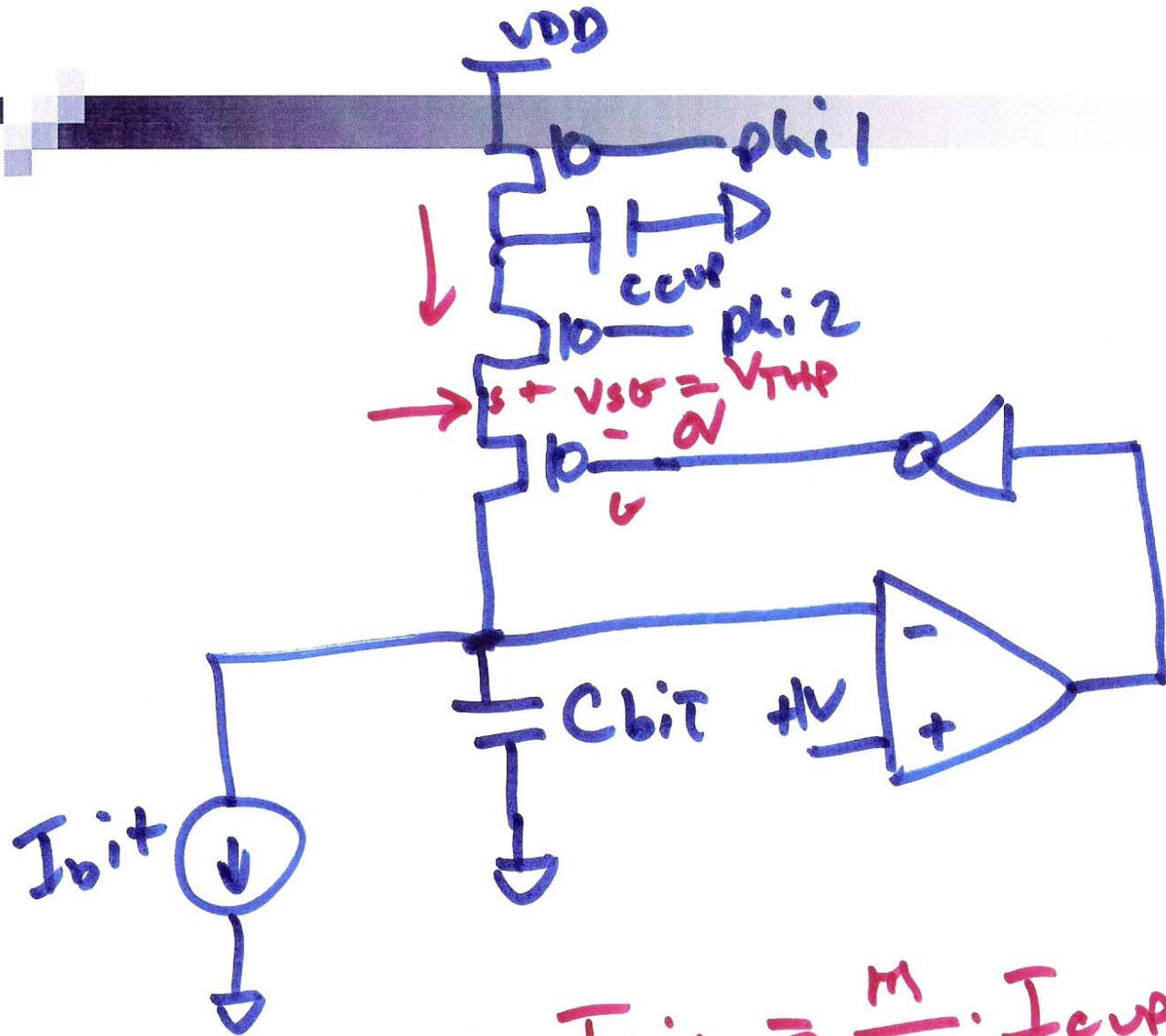
$$C_{cup} \cdot V_{DD} - C_{cup} \cdot V_i$$



$$I = \frac{C_{cup} (V_{DD} - V_i)}{T_{clk}}$$

$$= \frac{V_{DD} - V_i}{R_{sc}} \Rightarrow R_{sc} = \frac{1}{f_{clk} \cdot C_{cup}}$$

6)



$N = \# \text{ of CLKs}$
 $m = \# \text{ of times comp output goes high}$

$$R_{sc} = \frac{T_{clk}}{C_{cup}}$$

$$I_{bit} = \frac{m}{N} \cdot I_{cup}$$

$$I_{cup} = \frac{V_{DD} - V_{THP}}{R_{sc}}$$

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