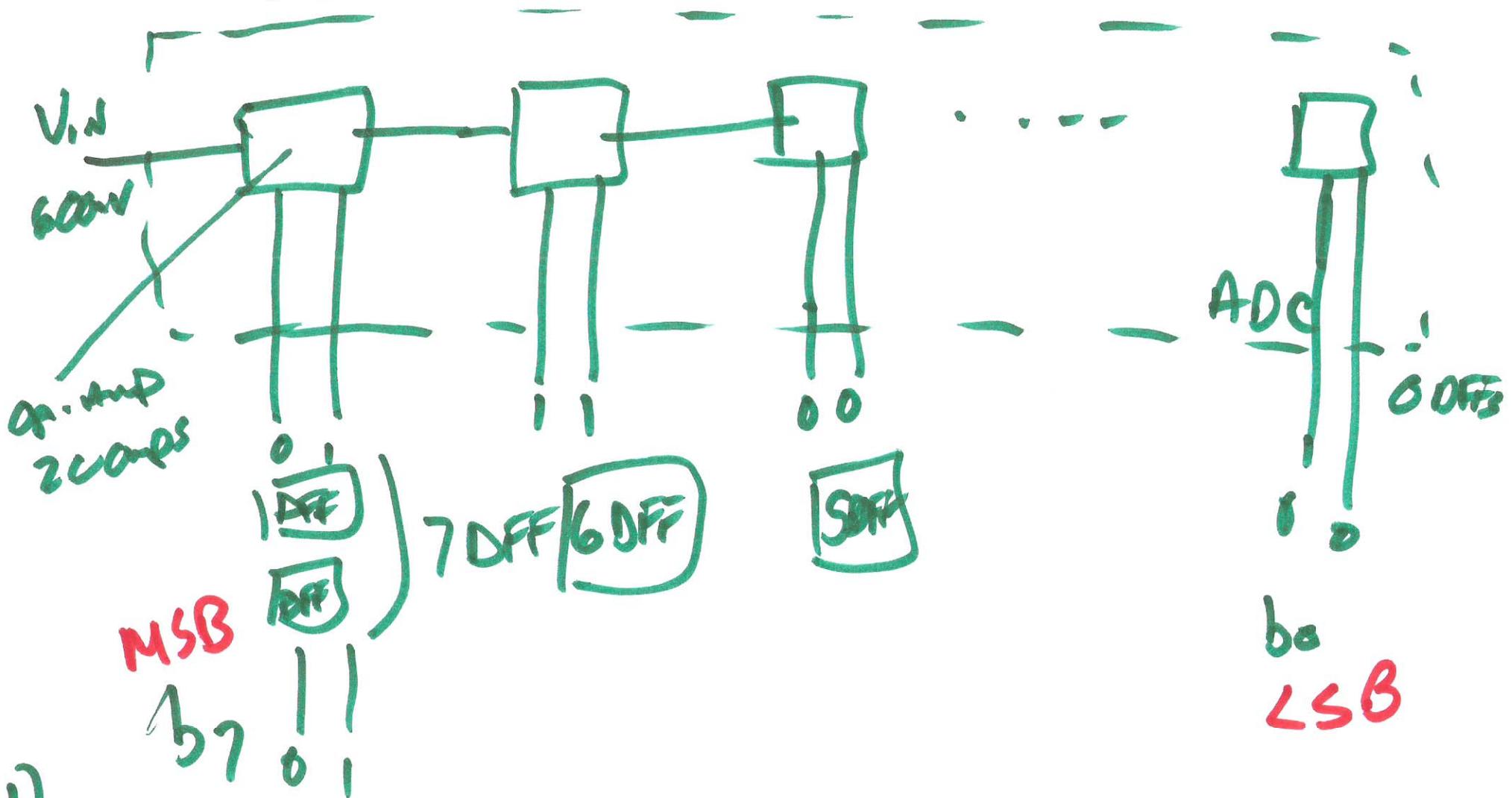


# ECE 614 Advanced Analog IC Design

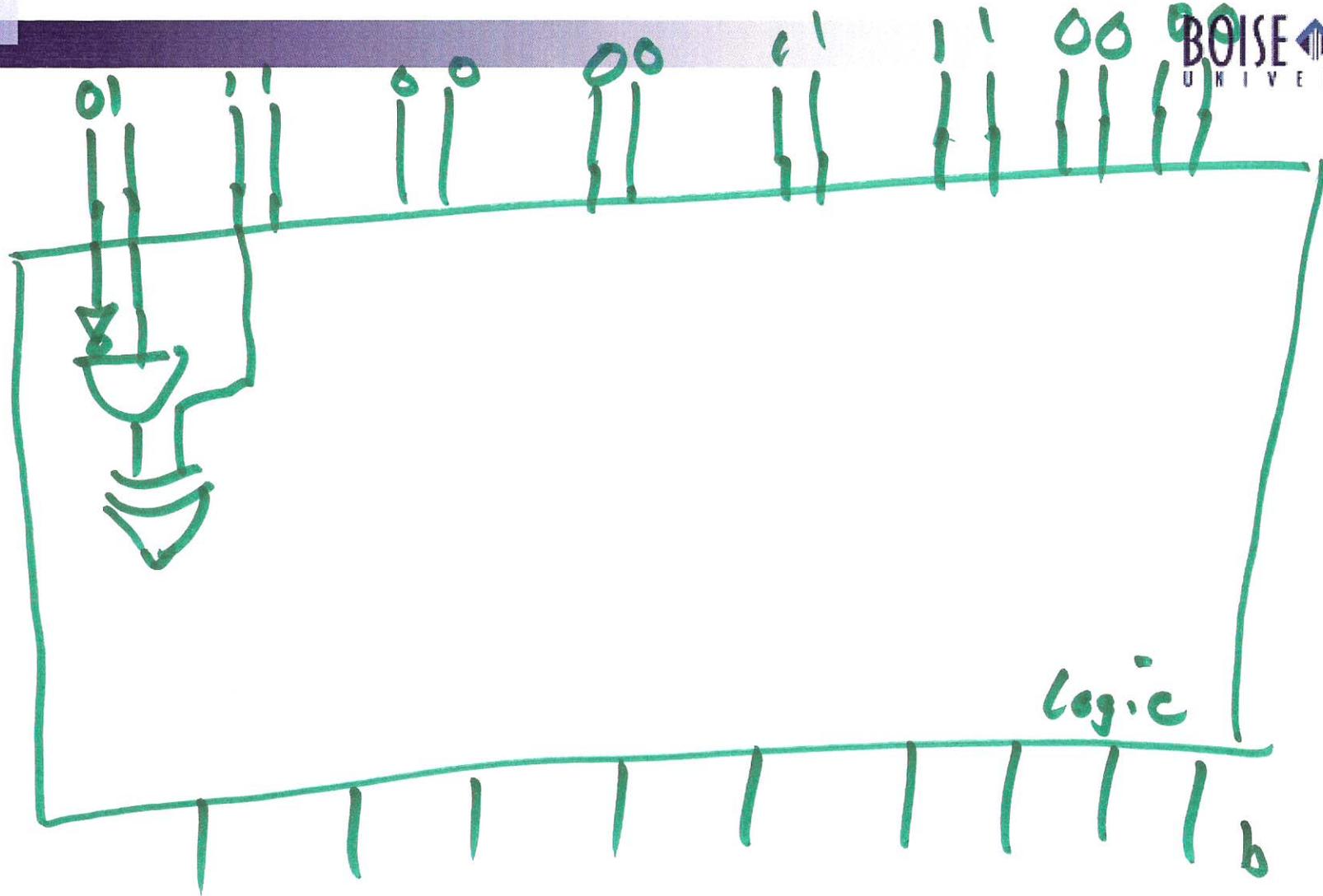
NOV. 29, 2011

Lecture 25

EX 30.17



11



0 → V<sub>REF+</sub>  
 V<sub>REF-</sub> → V<sub>DD</sub>

0000... → 0  
 1111... → V<sub>DD</sub> - 1 LSR  
 100000 → V<sub>DD</sub>

2)

Fastest Speed  
use minimum L

$V_{ov} = V_{gs} - V_{THN}$   
 $V_{ov} = V_{gs} - V_{THP}$   
high speed  
use large  $V_{ov}$

$V_{THN} = 280mV$

$V_{ov} = 120mV!$   
 $= 2f_{clk} \cdot V_{ov}$  12% of VDD

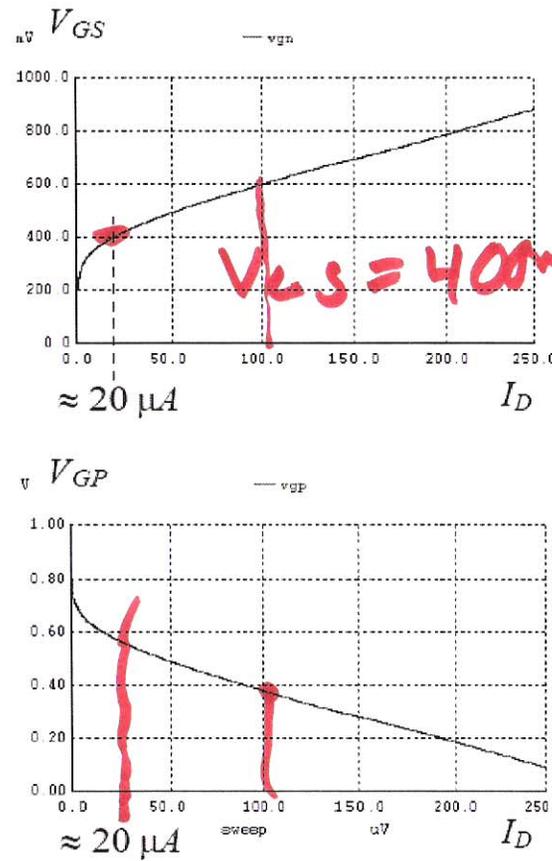
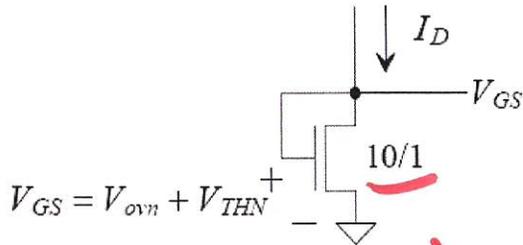
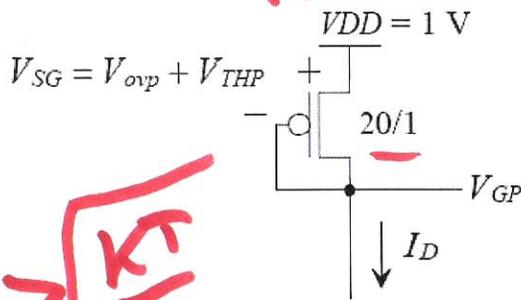


Figure 26.1 Gate-source voltages plotted against drain currents.



Problem is matching



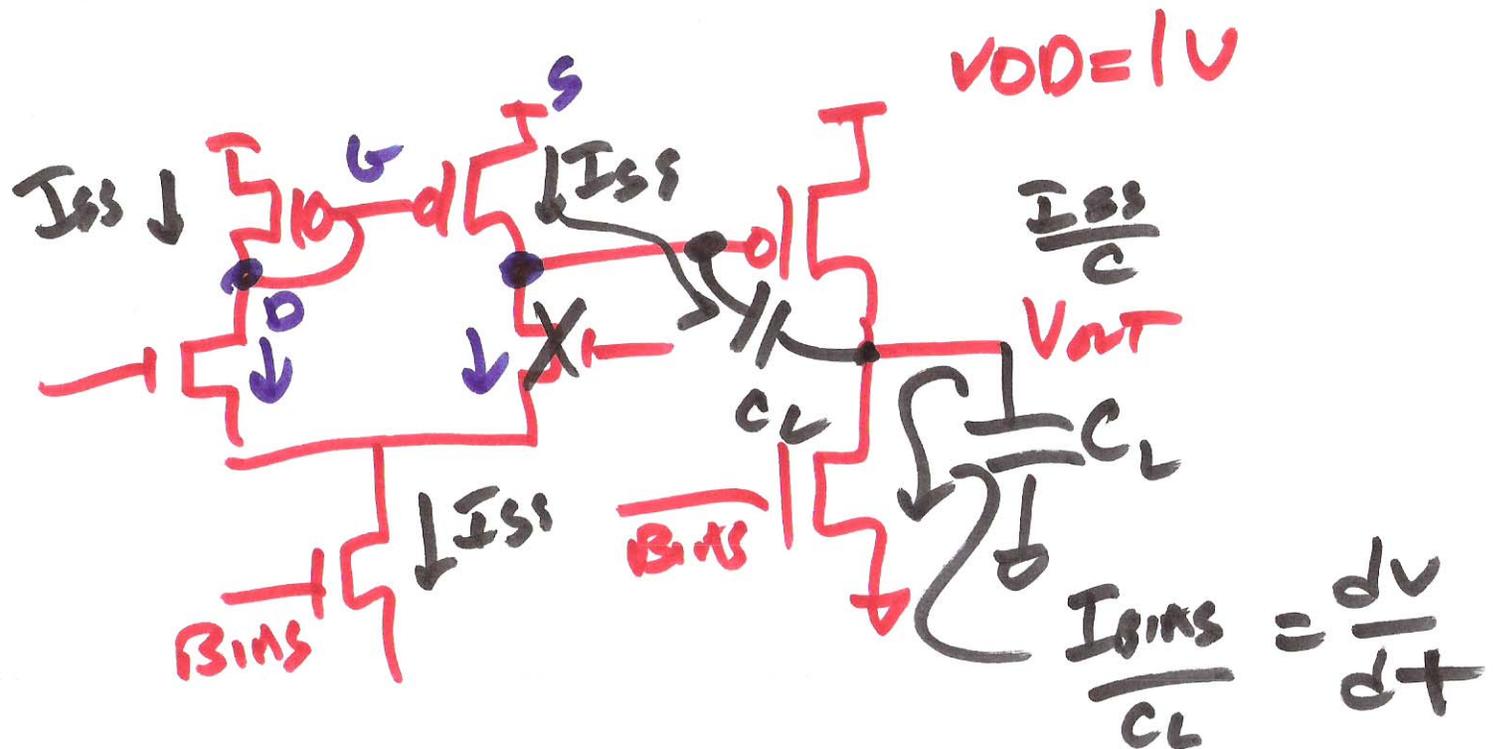
$LSB \propto \sqrt{\frac{kT}{C}}$

$\frac{I}{C} = \frac{dV}{dT} = \frac{\Delta V}{\Delta T} = \frac{V_{DD}}{T_{clk}/2}$   
How do I select C?  $\frac{I}{C}$   
 $\propto \frac{kT}{C}$  noise  $\rightarrow \frac{I}{C}$

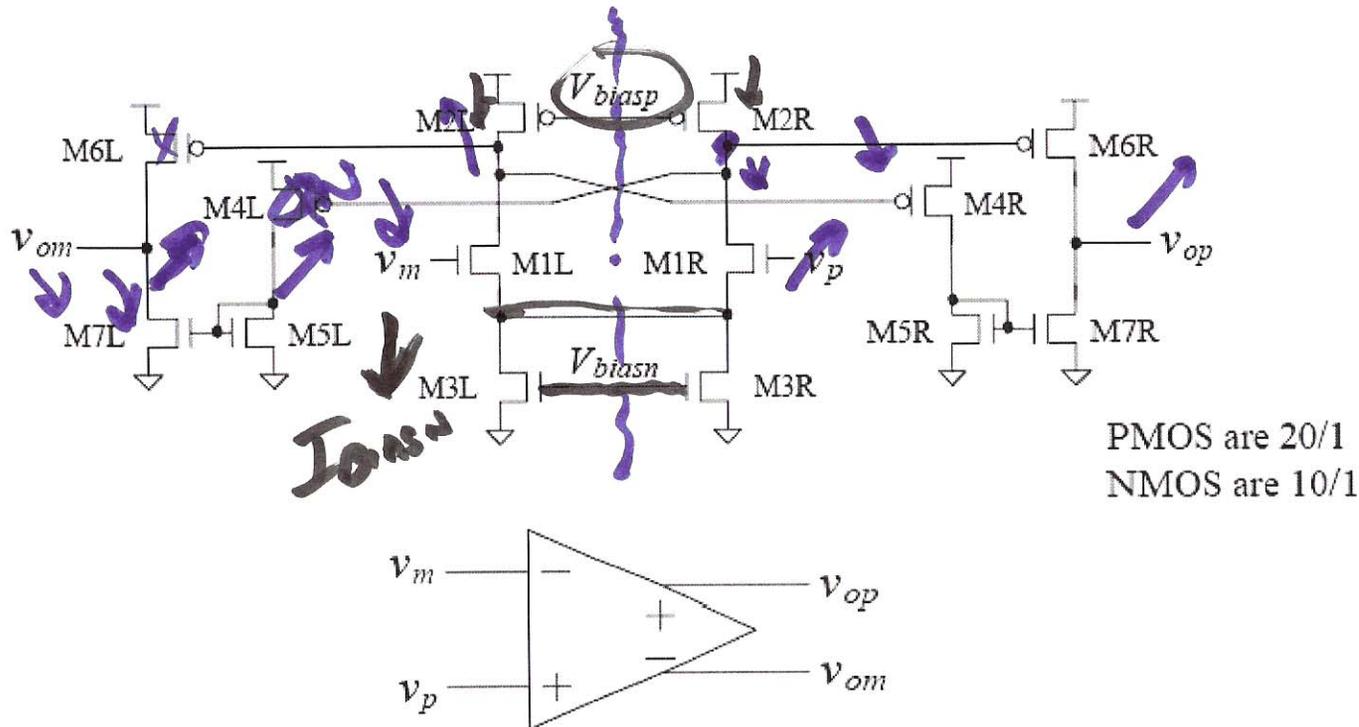
3)

$$250\text{fF} = C$$

$$\frac{I}{C} = \frac{100\text{mA}}{250\text{fF}} = \frac{dV}{dt} = 400\frac{\text{mV}}{\text{ns}}$$

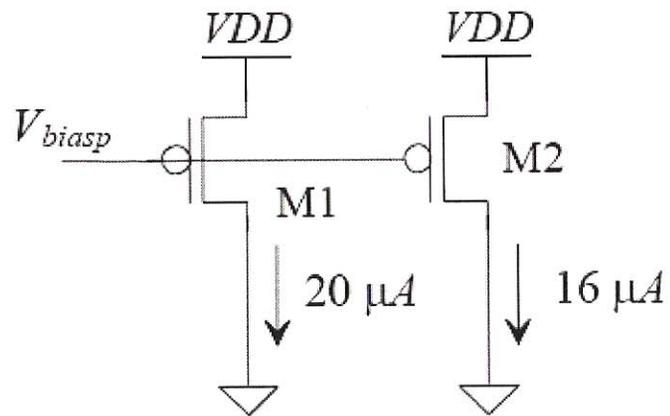


4)

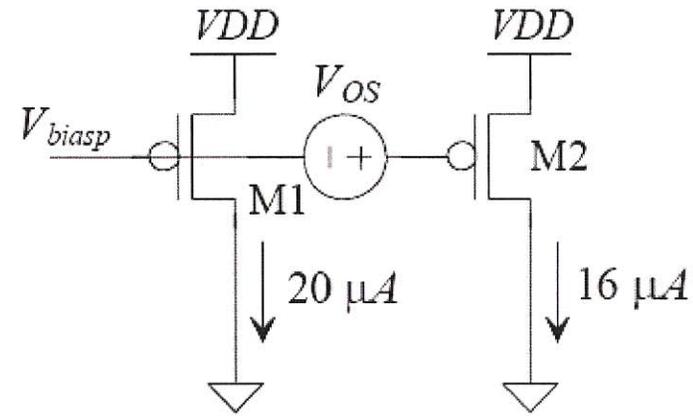


**Figure 26.2** A two-stage fully-differential op-amp. Compensation and CMFB are not shown. Output stage operates class AB. See discussion in the next section concerning the output voltage of the diff-amp.

5)



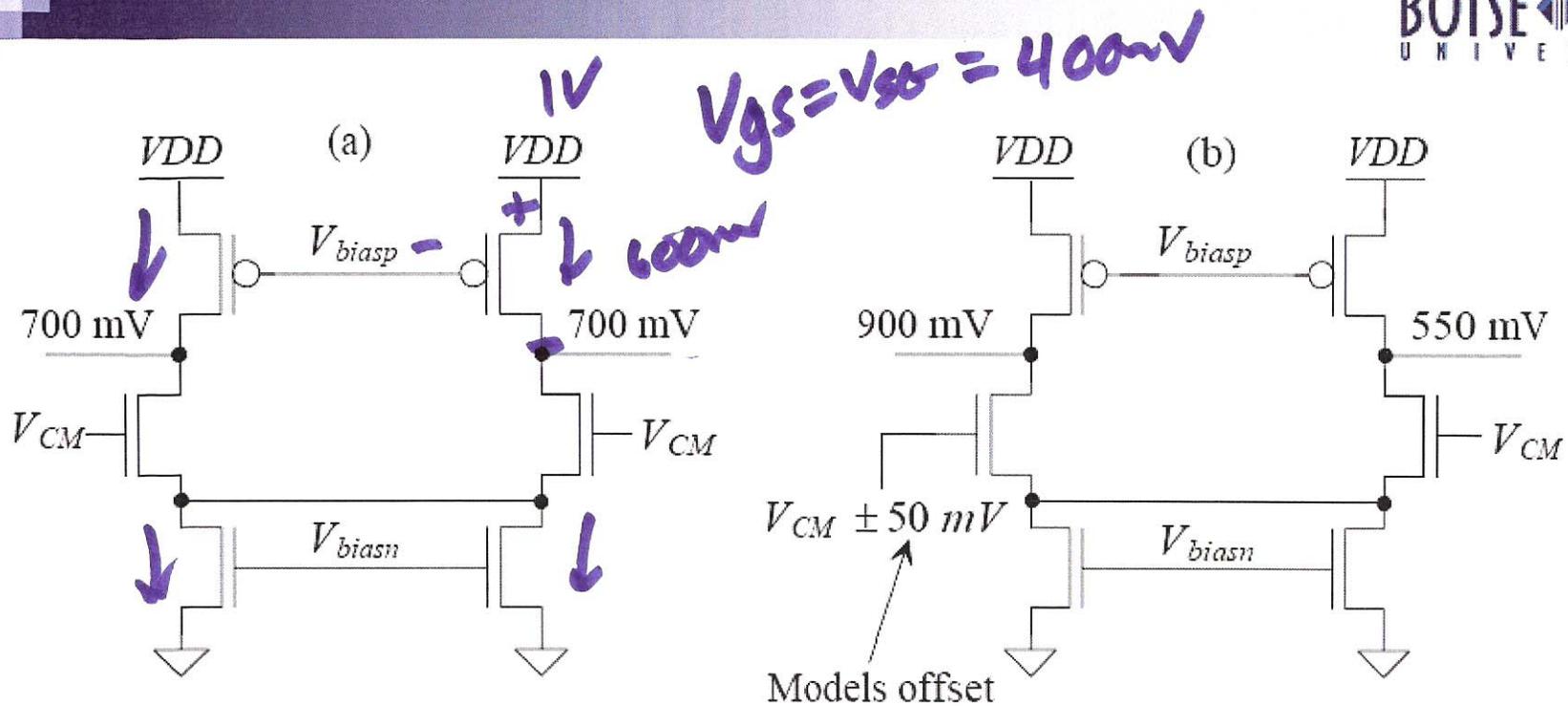
(a) M1 and M2 are mismatched.



(b) M1 and M2 are perfectly matched (as in a SPICE simulation).

**Figure 26.5** How we add an offset into the circuit to model mismatch.

6)



NMOS are 10/1  
 PMOS are 20/1  
 Bias circuit seen in Fig. 26.3

$$V_{CM} = V_{DD}/2 = 500 \text{ mV}$$

Figure 26.6 Comparing the diff-amp's output voltages with and without an offset.

→

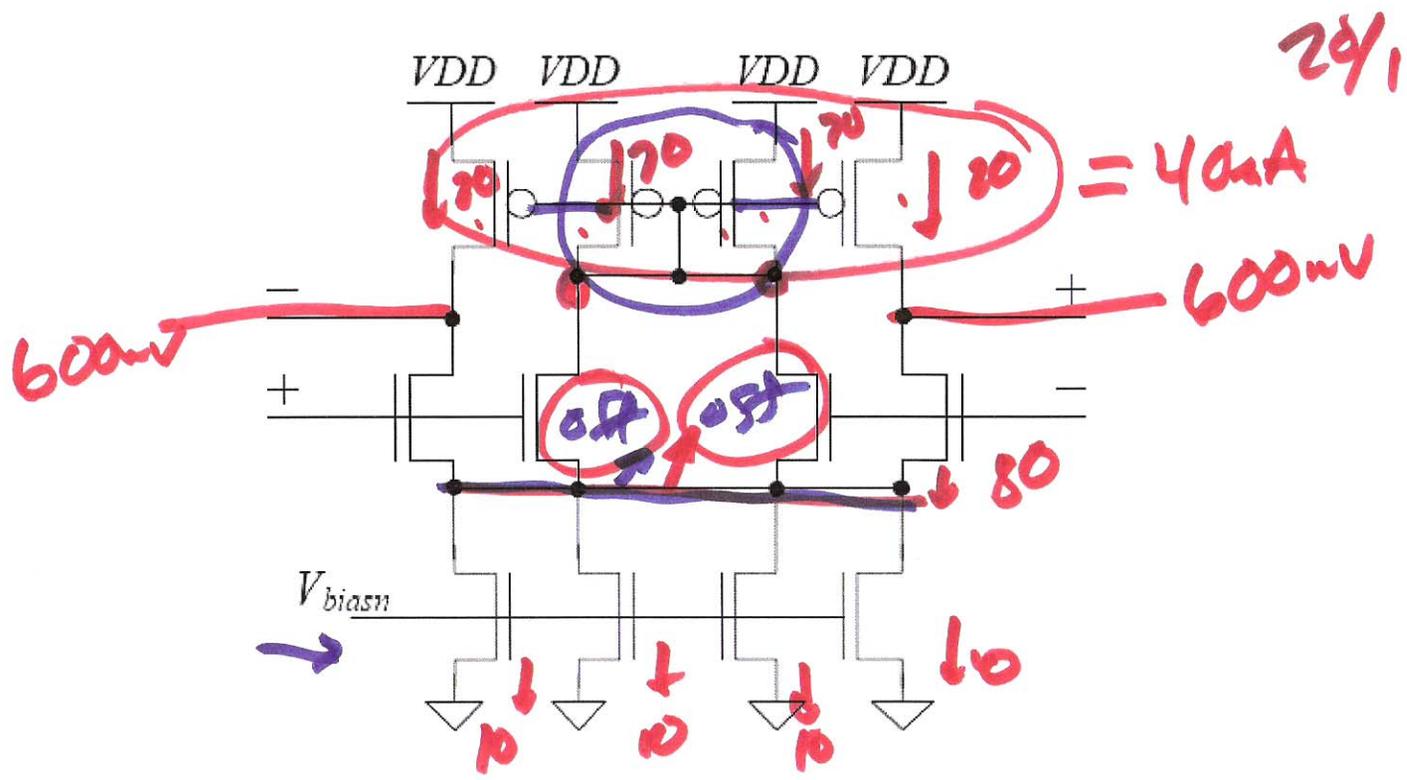


Figure 26.7 A fully-differential diff-amp that generates its own bias for the PMOS.

8)

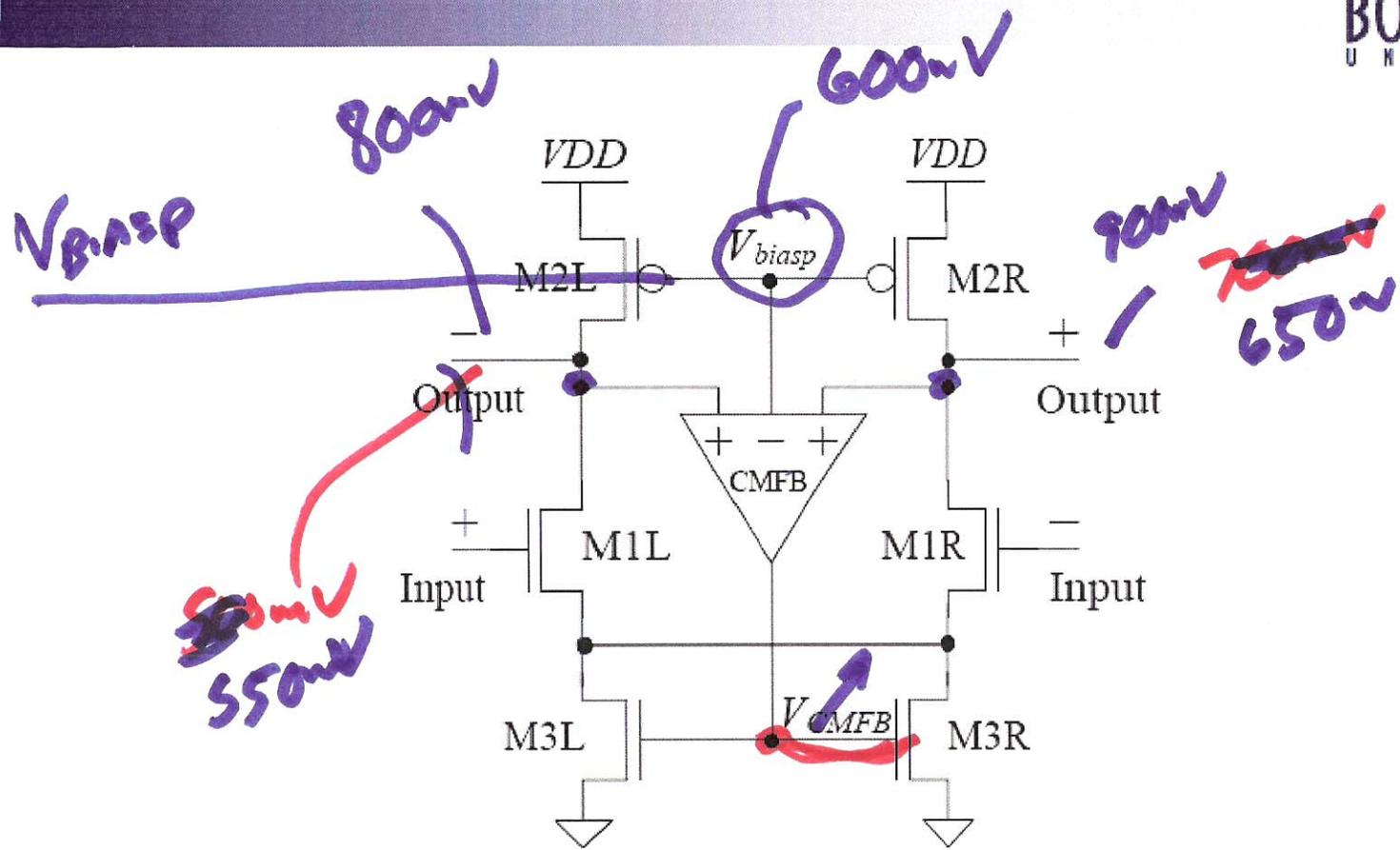
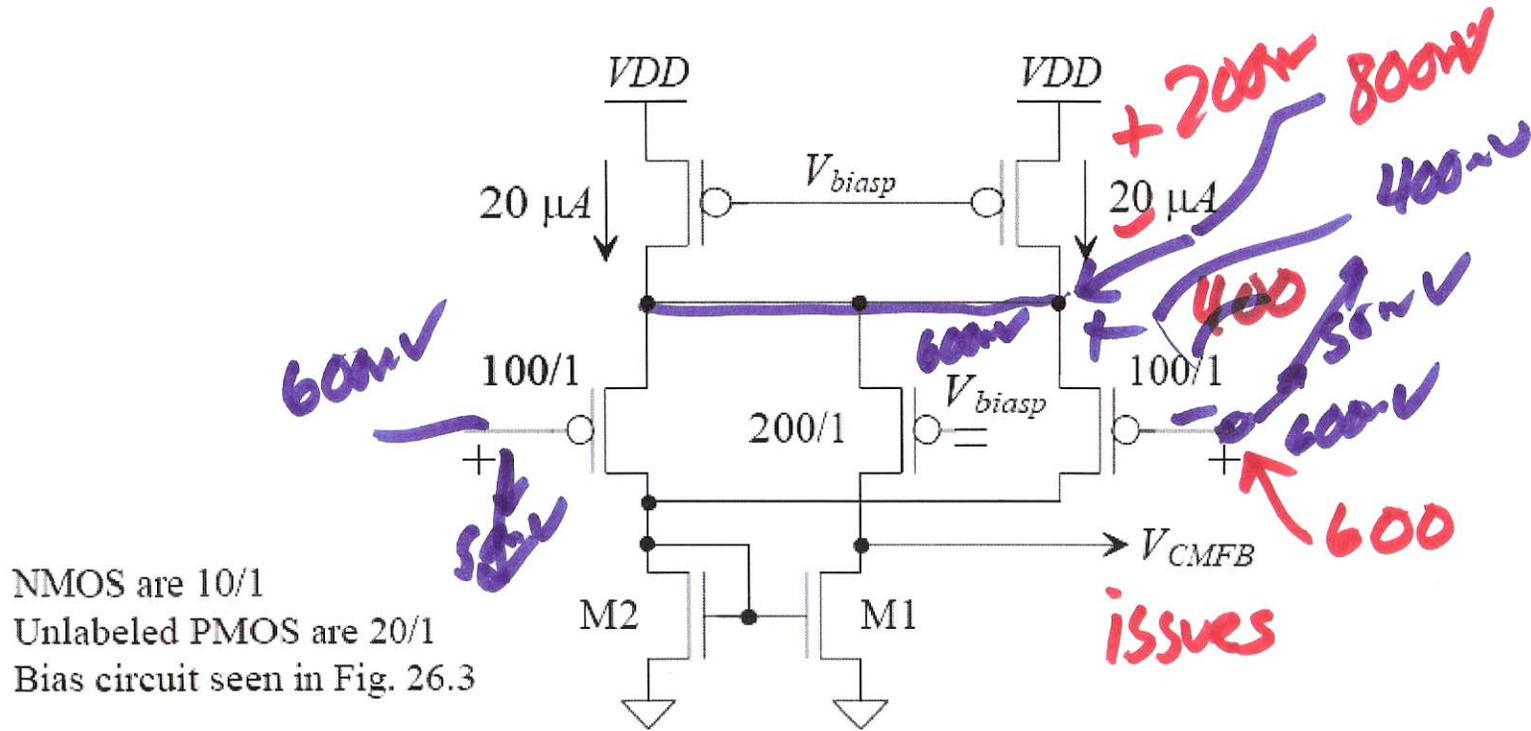


Figure 26.8 Using a common-mode feedback (CMFB) amplifier to set the output voltages.

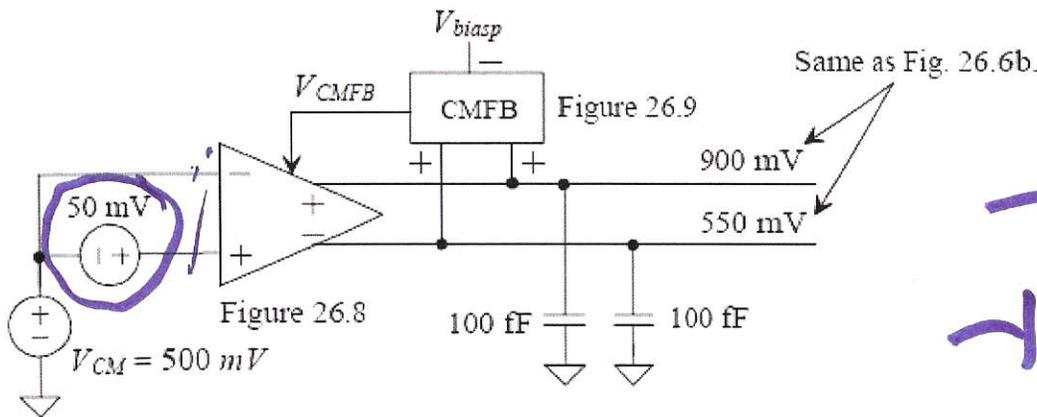
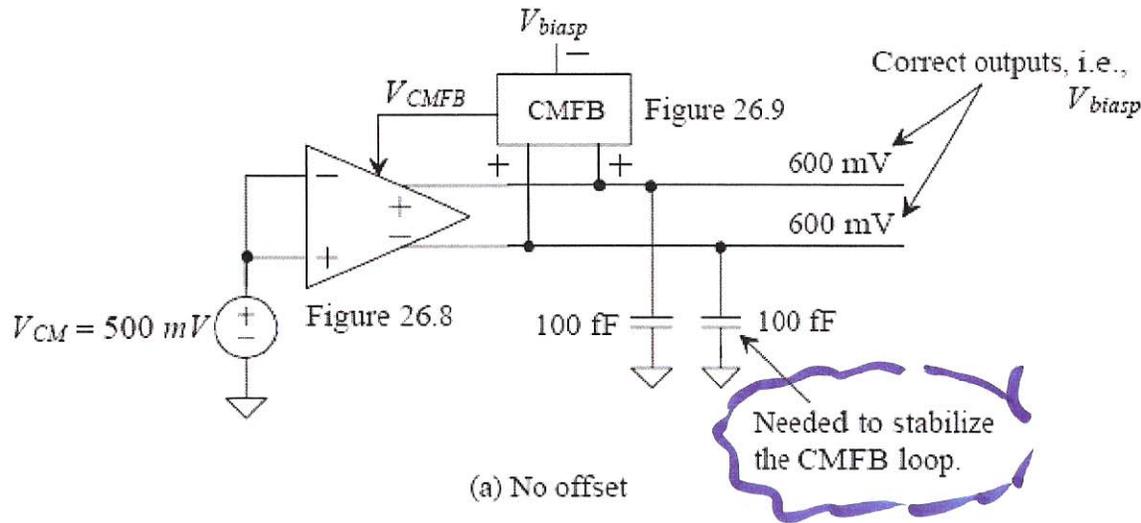
9)



NMOS are 10/1  
 Unlabeled PMOS are 20/1  
 Bias circuit seen in Fig. 26.3

Figure 26.9 Implementation of the CMFB amplifier in Fig. 26.8.

10)



(b) With a 50 mV offset. Note how the CMFB isn't doing anything.

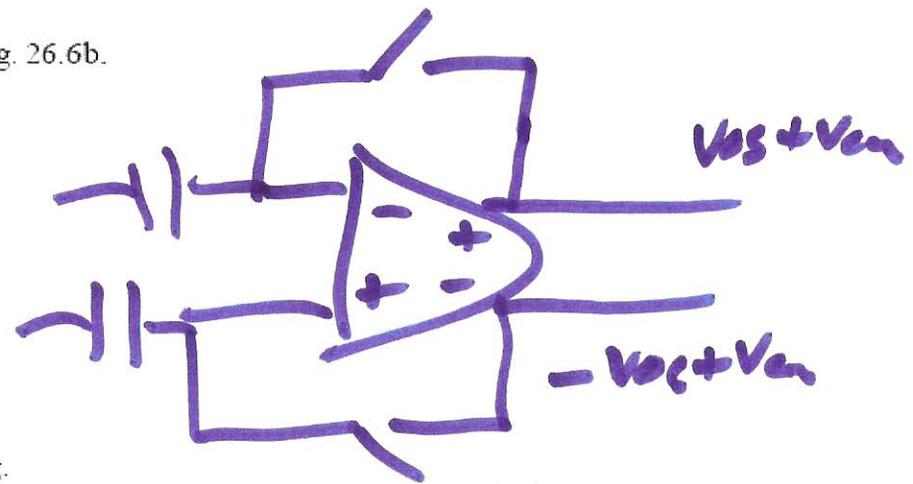


Figure 26.10 Simulating the operation of the CMFB circuit in Fig. 26.9.

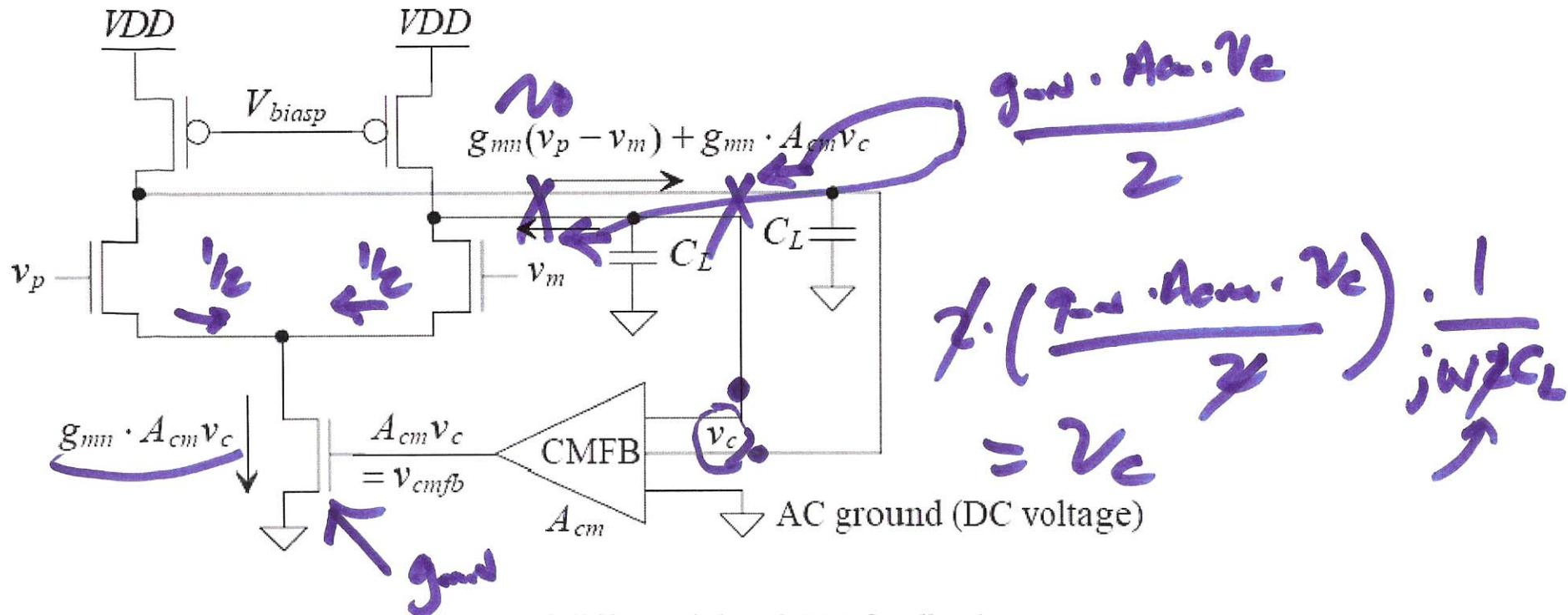


Figure 26.11 Schematic view of differential and CM feedback.

$$v_o = g_{m_n} \cdot A_{cm} \cdot v_c \cdot \frac{1}{j\omega C_L}$$

$$\frac{v_o}{v_c} = \frac{g_{m_n} \cdot A_{cm}}{j\omega C_L}$$

$A_{cm} \leq 1$

to compensate both diff & cm loads!

12)

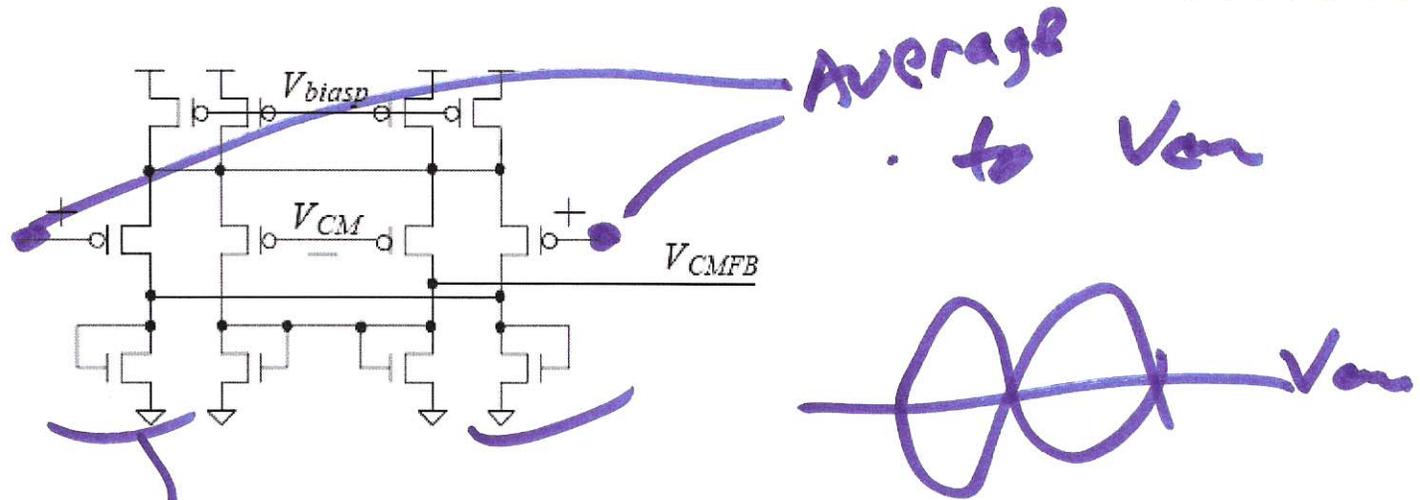


Figure 26.12 A CMFB amplifier with a gain of nominally unity.

why? Lowers  $A_{cm}$ !

13)

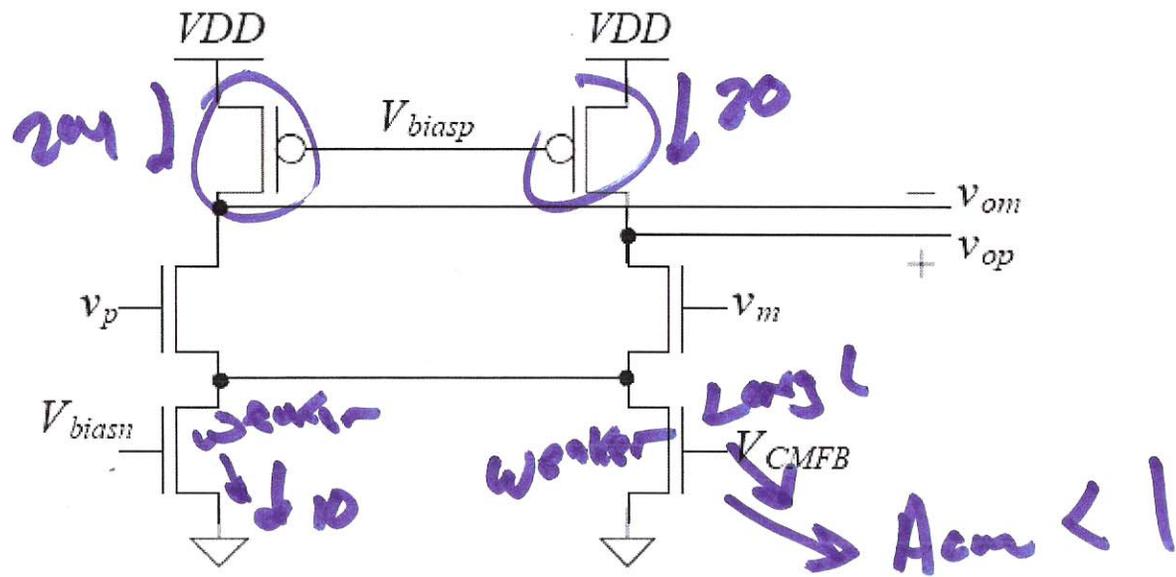
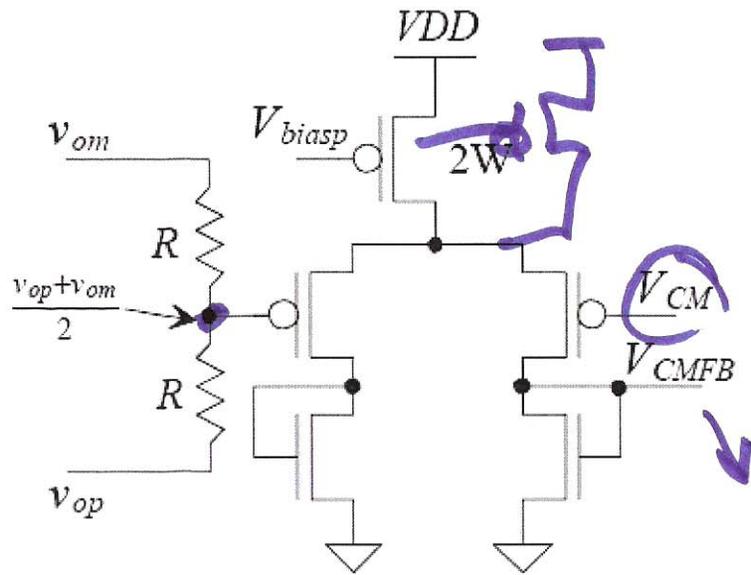


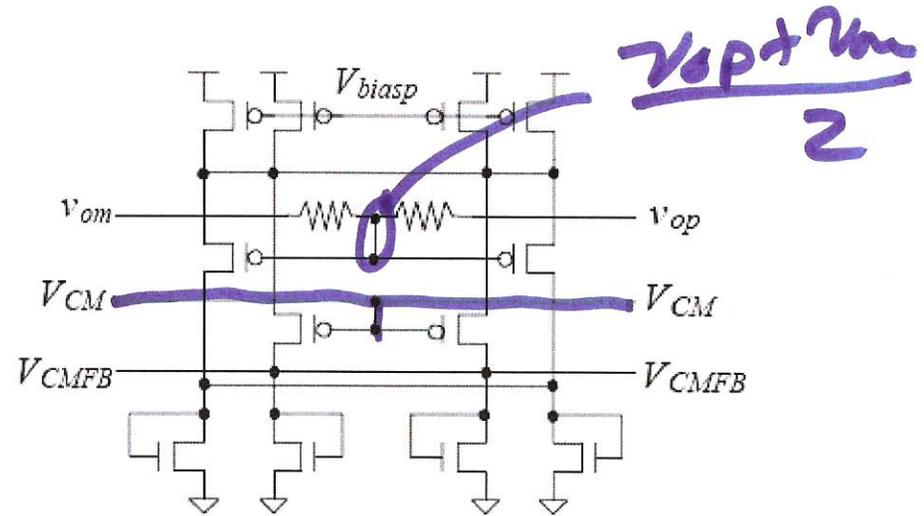
Figure 26.13 Reducing the forward gain of the CMFB loop.



14)



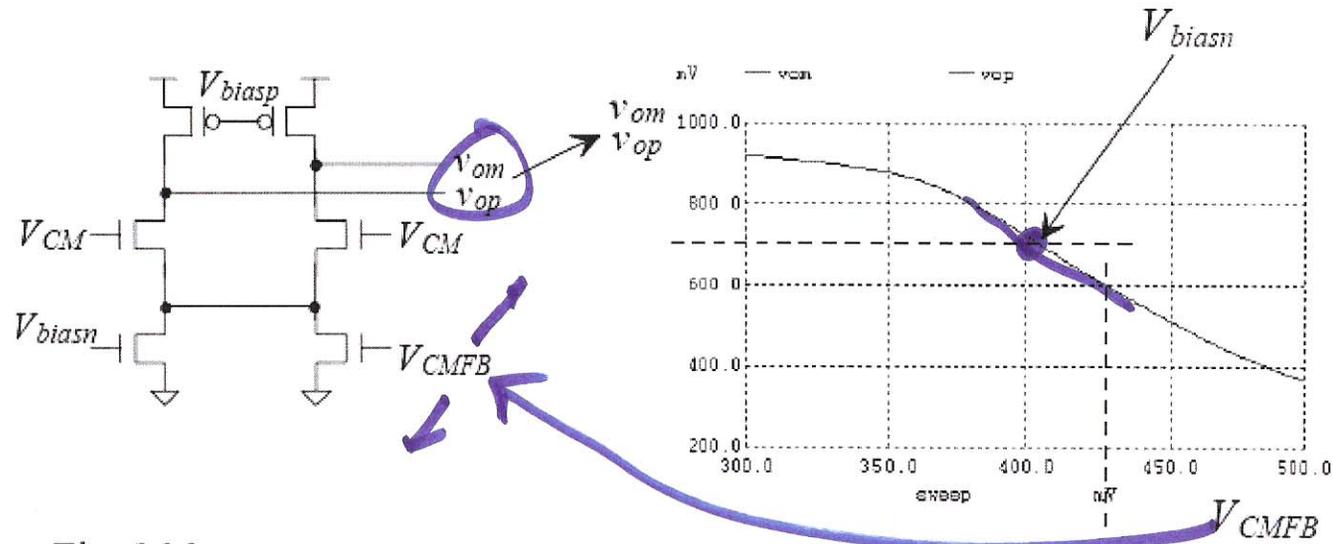
(a) Using resistors to average differential output signals.



(b) Symmetrical implementation of the CMFB circuit in (a).

Figure 26.14 Increasing CMFB amplifier input range.

15)



NMOS 10/1  
 PMOS 20/1  
 Bias circuit from Fig. 26.3

Value of CM feedback voltage when the outputs are 600 mV.

Figure 26.17 Plotting the output voltages as a function of the CM feedback voltage.

16)