Additional end-of-chapter problems for Chapter 30 – Implementing Data Converters

*CMOS: Circuit Design, Layout, and Simulation*

**A30.1** Verify, using simulations and a 3-bit data converter with *VREF*+ = 0 and *VREF*= 1V, that Eq. (30.4) is correct. What are the LSB of the converter and the converter’s output swing (verify your simulations using an ideal op-amp)?

**A30.2** What is the output swing of the traditional voltage-mode R-2R DAC seen in Fig. 30.2 if *VREF*+ = 0 *VREF*= 1 V? Does Eq. (30.7) describe the operation of the DAC when *VREF*+ < *VREF*? Assume both reference voltages are positive.

**A30.3** Using simulations, and a 4-bit DAC, verify that Eqs. (30.14) and (30.17) accurately predit the DNL and INL error, given the assumed matching of the resistors used to derive these equations, of the DAC topology seen in Fig. 30.3.

**A30.4** Design, and simulate the operation of, an 8-bit DAC based upon the wide-swing current-mode *R*-2*R* DAC seen in Fig. 30.3 where the upper two bits are split apart into 4-segments. Comment on the resistor matching requirements to achieve a DNL of less than 1 LSB.

**A30.5** Rederive Eqs. (29.59)-(29.60) using the shunt-shunt amplifier topology discussed in Sec. 30.2.

**A30.6** Show, using simulations, that Eq. (30.50) is still valid if the op-amp has a 50 mV offset voltage.

**A30.7** Derive an equation, similar to how Eq. (30.50) was derived, to describe the transfer function of the S/H seen in Fig. 30.31.

**A30.8** Derive an equation, similar to how Eq. (30.50) was derived, to describe the transfer function of the S/H seen in Fig. 30.34.

**A30.9** Repeat Ex. 30.10 if the ADC’s input is 720 mV.

**A30.10** Explain, in your own words, how the circuit in Fig. 30.42 operates. Use simulations to augment your explanation.

**A30.11** Sketch, similar to Fig. 30.53, the digital logic used to combine the outputs of each stage in a 4-bit pipeline ADC that uses 1.5 bits/stage. Assuming *VDD* = *VREF*+ = 1 V and *VREF* = 0 describe the outputs of each stage, and the digital logic used to combine these outputs, if the input to the ADC is 323 mV. Ensure that you also show how the delay elements used on the outputs of each pipeline stage are connected to the logic.

**A30.12** Repeat Ex. 30.17 but with an input voltage of 323 mV.

**A30.13** Repeat the derivations seen in the section covering *Capacitor Error Averaging* assuming all capacitors are perfectly matched but the op-amps have finite gain, *AOL*. Verify your derivation results using simulations with *AOL* = 100.