Additional end-of-chapter problems for Chapter 28 – Data Converter Fundamentals

*CMOS: Circuit Design, Layout, and Simulation*

**A28.1** Can clock jitter be related to aperture error? Why or why not? Develop a relationship between aperature error and peak-to-peak clock jitter, *Tjitter*, in a S/H.

**A28.2** Find the number of bits required of a DAC if *VREF* = *VDD* = 1V and a resolution < 5 mV is required.

**A28.3** What will happen to the output voltage of a DAC if the DAC is nonmonotonic between the codes 1000 0000 and 1000 0001 if the input is changed from 1000 0000 to 1000 0001? Will the output of the DAC go up, go down, or stay the same? Why?

**A28.4** Is DNL or INL a measure of small-signal linearity? Which parameter is a measure of large signal linearity? Give examples using a DAC’s transfer curves.

**A28.5** Suppose a DAC has both specified gain and offset errors but, at the same time, the DAC’s INL is (for all values) specified as 0. Comment on the method used to determine INL.

**A28.6** If it is desirable to generate a signal using a DAC with a 1,000:1 dynamic range, *DR*, estimate the number required of the DAC. What is the assumption made with this estimate between the minimum signal generated and the LSB of the DAC?

**A28.7** Estimate the RMS value of the quantization error voltage in Fig. 28.20.

**A28.8** Does a DAC introduce quantization noise into its digital input signal? Does an ADC introduce quantization noise into its analog input signal? Why or why not?

**A28.9** In your own words comment on why the ADC’s transfer curves in Fig. 28.20 are shifted from the curves transfer curves seen in Fig. 28.19.

**A28.10** Estimate the minimum sampling frequency, *fsample*, required if an input signal, with the spectrum seen below, is to be digitized (using a S/H and an ADC) so that any aliased signal in the resulting output spectrum is at least 60 dB below the desired signal in the frequency range from DC to *fsample*/2. Sketch the signals’ spectrum after sampling using the value you determine up to a frequency of 3*fsample*.

**Figure A28.10** Input signal for problem 28.10.

*f*

 30 dB/dec

Analog input signal

10 MHz