Additional end-of-chapter problems for Chapter 26 – Operational Amplifiers II

*CMOS: Circuit Design, Layout, and Simulation*

**Unless otherwise indicated use the 50 nm process from the book.**

**A26.1** Using *VSG* = *VGS* = 400 mV and an NMOS size of 20/1 and a PMOS size of 40/1 (scale factor is 50nm) we can design an op-amp with larger margins for changes (in temperature, process, or *VDD*) to maintain high speeds when driving a 250 fF capacitor. Regenerate Figs. 26.1 and 26.4 with these changes in device sizes. How will the power dissipation change? How much will *VSG* and *VGS* have to increase to pulse the drain currents to 100 A?

**A26.2** What will happen to the inherent speed of an op-amp if we keep the biasing currents fixed while we increase the widths of the MOSFETs? Why? What will happen to the maximum current the MOSFETs can source? Use SPICE to verify your answers.

**A26.3** What happens to the bias currents in Fig. 26.4 if we change the 10/20 PMOS device to 10/2? Explain what is going on. Use simulations to support your explanations.

**A26.4** Simulate the operation of the circuit in Fig. 26.8 using a CMFB amplifier that you design that doesn’t have problems with input common-mode range. Verify the operation of your design using SPICE.

**A26.5** Verify, using a SPICE transient simulation, that the circuit in Fig. 26.10 becomes unstable when the 100 fF load capacitors are removed. Show the details of how Eq. (26.2) is derived.

**A26.6** Will the SC CMFB circuit seen in Fig. 26.16 on page 874 work without using the *C*2 capacitors (that is, using the *C*1 capacitors for the averaging)? Why or why not? Use SPICE to verify your comments.

**A26.7** Suggest a topology to remove two of the switches used in the SC CMFB circuit seen in Fig. 26.16 on page 874 (so the SC CMFB circuit uses 6 TGs instead of 8). Verify the correct operation of your topology with SPICE but comment on the practical problems associated with the modification (is there a DC path to *VCMFB*?).

**A26.8** Perform an operating point analysis using SPICE for the diff-amp seen in Fig. 26.19. Identify the transistors operating in, or near, triode. Discuss, and verify with SPICE, how to move the devices further into the saturation region. Does your modification increase power and allow the diff-amp to operate with a VDD of 900 mV?

**A26.9** Regenerate the plots seen in Fig. 26.23 and 26.24 if the biasing circuit in Fig. 26.22 is replaced with the topologies seen in Figs. 26.52 and 26.63. Comment on the benefits and drawbacks of the new design.

**A26.10** Show, in Fig. 26.29, how adding a resistor in the source-side of the 20/1 MOSFET used in the output buffer can also be used to help with adjusting the common-mode level on the op-amp’s output. Ensure, in your solution, that it’s clear you understand the problem and the pros/cons of this approach.