Additional end-of-chapter problems for Chapter 29 – Data Converter Architectures

*CMOS: Circuit Design, Layout, and Simulation*

**A29.1** Suppose that the resistor string DAC seen in Fig. 29.2 is made using (nominally) 1k resistors that show a linear variation in their sheet resistance of 0.5% (the bottom resistor is 1k, the second from the bottom has a value of 1,005 Ω, the third resistor from the bottom has a value of 1,010 Ω, etc.). If the DAC has 10-bits resolution then estimate the DACs INL and DNL. Note that the nominal value of the resistor, *R*, is not 1 kΩ but rather the value of *R* that makes Eq. (29.2) valid.

**A29.2** Sketch the implementation of a resistor string DAC using the R-2R structure (note there isn’t an op-amp). Simulate the operation of your design using SPICE for a 3-bit resolution. What is the output resistance of your circuit? (Hint: see Fig. 29.52)

**A29.3** Sketch the transistor implementation of, and simulate the operation using the 50 nm process models, a 3-bit DAC (with one LSB = 10 A) using the topologies seen in Fig. 29.9 and 29.10. Assume that each of the DACs’ outputs is connected to 10kΩ loads to *VDD*. (Note that in Figs. 29.9 and 29.10 that one of the DACs’ outputs is connected to ground while the other is labeled *iout*.)

**A29.4** Simulate the operation of the charge-scaling DAC seen in Fig. 29.13 using a voltage-controlled voltage source for the op-amp (see Fig. 20.19, assume the open-loop gain of the op-amp is 106).

**A29.5** Sketch the implementation, based on the sample-and-hold seen in Fig. 25.19 (a S/H with a gain of 1), of the S/H with a gain of ½ used in a cyclic or pipeline DAC. Simulate the operation of your design.

**A29.6** Sketch the implementation of the decoder seen in Fig. 29.21.

**A29.7** For the op-amps in problem 29.21 estimate the gain-bandwidth product required of the op-amp used in the residue amplifier if the converter will run at 10 MHz.

**A29.8** Estimate the worst-case DNL and INL for an 8-bit Flash ADC if the resistor matching is 1%.

**A29.9** Estimate the worst-case DNL and INL for an 8-bit Flash ADC if the comparator offset is 1% of *VREF*.

**A29.10** Estimate the worst-case DNL and INL for a 10-bit Pipeline ADC if the gain of the amplifiers is 2 +/- 1% (that is, the gain varies from 1.98 to 2.02).

**A29.11** Estimate the worst-case DNL and INL for a 10-bit Pipeline ADC if the comparator offset is 1% of *VREF*.