Additional end-of-chapter problems for Chapter 25 – Dynamic Analog Circuits

*CMOS: Circuit Design, Layout, and Simulation*

**A25.1** Regenerate Fig. 25.2 using the 50 nm process from the book.

**A25.2** Using the 50 nm process demonstrate capacitive feedthrough, charge injection, and clock feedthrough using an NMOS device, PMOS device, and a TG.

**A25.3** Simulate the operation of the sample-and-hold circuit in Fig. 25.8 using a 1 pF hold capacitor, the 50 nm process, and a voltage-controlled voltage source for the op-amp. Show how the maximum input amplitude is limited by using only a 10/1 NMOS switch. Resimulate with a TG (use a 20/1 PMOS). Show, in both simulations, reducing the hold capacitor can: allow the circuit to operate faster (at the cost of increasing kT/C noise) and make the effects of the charge injection and capacitive feedthrough worse.

**A25.4** Derive the z-domain transfer function of the sample-and-hold seen in Fig. 25.15. For help you can refer to the second edition of the book *CMOS Mixed-Signal Circuit Design*.

**A25.5** Using the topology seen in Fig. 25.19 with 100 fF hold capacitors (instead of 1 pF capacitors) and the 50 nm process show how using bottom-plate sampling can reduce the effects of nonlinear charge injection and the effects of substrate noise.

**A25.6** Design a switched-capacitor RC circuit, Fig. 25.22, using the 50 nm process and a clock frequency of 100 MHz design a circuit with an *f*3*dB* frequency of 1 kHz. Simulate the operation of the design if the circuits’ input is 250 mV + 10 mV∙sin2π1000∙*t*.