Additional end-of-chapter problems for Chapter 3 – Analog Filters

*CMOS: Mixed-Signal Circuit Design*

**A3.1** For the simple RC circuit seen in Fig. 3.1, with *R* = 1k and *C* = 1 pF, determine an equation for the transfer function, and then sketch, both the magnitude and phase responses (the Bode plots). Verify your Bode plots with LTspice. From the frequency response plots sketch the input and output voltages of the circuit in the time-domain if the input is a 1-V peak sinewave centered around ground at 200 MHz. Verify your time-domain sketches using LTspice.

**A3.2** For the filter seen in Fig. 3.6 sketch the ideal (using an ideal op-amp) and non-ideal (due to finite op-amp *fun*) pole locations in the complex plane. State, and justify, any assumptions you make.

**A3.3** Suppose a RCF is needed on the output of a 10-bit DAC. Further suppose the filter will be implemented using a first-order active-RC topology with *VDD* = 1 V. Estimate the minimum integration capacitance required. What value of capacitance would you select for the design and why? If the bandwidth of the RCF is 100 kHz and the DAC is clocked with *fs* = 100 MHz then what is the maximum signal (amplitude) possible in the RCF’s output at 50 MHz? Show your work.

**A3.4** Determine the *z*-domain transfer function of the filter seen in Fig. 3.22. Using Eq. (2.48) estimate the frequency response of the filter and verify, at two different input frequencies, using LTspice.

**A3.5** Show the details of how the gains, *G*, are derived in Fig. 3.31.

**A3.6** Show the details of how the gains, *G*, are derived in Fig. 3.32

**A3.7** Show the details of how the gains, *G*, are derived in Fig. 3.34.

**A3.8** Determine the location of the poles, and if applicable zeroes, in the complex plane for the filters simulated in Examples. 3.8-3.12.

**A3.9** Show the details of how Eq. (3.78) is derived. If the resistors used in Ex. 3.13 match within 2% are there any concerns? What about matching within 5%? Use simulations to support your comments.

**A3.10** Can *Q* peaking occur in a switched-capacitor filter? Re-simulate the filter seen in Fig. 3.47, with the reduction in the capacitors described in Ex. 3.14 to keep the filter stable, using op-amps with finite gain-bandwidth products (say *fun* = 100 MHz) to support your answer.

**A3.11** Show the details of how the gains, *G*, are derived in Fig. 3.53.