Additional end-of-chapter problems for Chapter 19 – Digital Phase-Locked Loops

*CMOS: Circuit Design, Layout, and Simulation*

**A19.1** Is the source coupled VCO seen below a good design? Why or why not? Use SPICE to verify your answer and comments.

**Figure A19.1** Topology for a VCO. Good or bad?

*VDD*

*VDD*

*VinVCO*

*Output*

*Output*

**A19.2** Repeat Ex. 19.2 using a passive lag loop filter.

**A19.3** Verify that increasing the loop filter’s capacitance in Ex. 19.2 causes the PLL to become unstable.

**A19.4** Repeat Ex. 19.4 if the input signal frequency is 25 MHz. Show, using SPICE, how the 100 MHz output signal is locked to the 25 MHz input signal when a divide by 4 is added in the feedback path.

**A19.5** Repeat Ex. 19.5 if the input signal frequency is 25 MHz. Show, using SPICE, how the 100 MHz output signal is locked to the 25 MHz input signal.

**A19.6** Using the 50 nm process from the book design a VCO based upon the schematic seen in Fig. 18.8 that oscillates at 100 MHz when *VinVCO* = *VDD*/2 = 500 mV. Verify your design with simulations and plot the VCO’s output frequency against *VinVCO* as seen in Fig. 19.6.

**A19.7** Show using simulations and at least 10 simulation points, that the XOR PD transfer curves seen in Fig. 19.8 are correct. Ensure that the input of the XOR PD is varied from a phase shift of 0 to 2. To determine each of these points in a simulation the *data* and *dclock* signals should be fixed, with some phase difference, while the output of the XOR PD is RC lowpass filtered. Ensure you simulate long enough to reach steady-state.

**A19.8** Repeat A19.7 for the PFD with tri-state output, Fig. 19.11. Ensure the input to the PFD is varied from 2 to +2.

**A19.9** Repeat A19.7 for the PFD with charge pump output, Fig. 19.11. Ensure the input to the PFD is varied from 2 to +2.

**A19.10** Show how, in Ex. 19.4, reducing the loop’s damping factor, , to 0.2 can cause problems. Then show what happens if  is increased to 2.

**A19.11** Repeat problem 19.10 for Ex. 19.5.