Additional end-of-chapter problems for Chapter 11 – The Inverter

*CMOS: Circuit Design, Layout, and Simulation*

**Unless otherwise indicated use the 1 m process parameters from Table 6.2 on page 147.**

**A11.1** Estimate the switching point voltage, *VSP*, output low voltage, *VOL*, and output high voltage, *VOH*, for the following inverters using the square-law equations. Generate voltage transfer curves (VTCs) for these inverters using SPICE. Compare your hand calculations to the SPICE simulation results.

**A11.2** Estimate the delays, both *tPHL* and *tPLH*, when the inverters in problem A11.1 are driving 100 fF capacitors. Use a SPICE transient analysis to verify your hand calculations.

**Figure A11.1** Estimating the DC characteristics of resistor-load inverters.

10/1

*VDD*

10/1

*VDD*

In

Out

30k

In

Out

50k

**A11.3** Suppose the inverters in problem A11.1 are cascaded, as seen below. Estimate the *VSP* of the resulting cascade (remember *VSP* is defined as when the input and output voltages are equal). Which inverter dominates the *VSP* ? Why? Use SPICE to confirm your comments.

**A11.4** Repeat problem A11.1 using the following inverter configurations.

**Figure A11.3** Estimating the *VSP* of a cascade of inverters.

10/1

*VDD*

10/1

*VDD*

In

30k

Out

50k

10/1

*VDD*

Out

50k

10/1

*VDD*

In

30k

**A11.5** Repeat problem A11.2 using the inverters in Fig. 11.4.

**Figure A11.4** Estimating the DC characteristics of NMOS or PMOS inverters.

10/1

*VDD*

10/1

*VDD*

In

Out

In

Out

10/5

10/5

**A11.6** Show how, using square-law equations in symbolic form, you derive the switching point voltages for the inverters in Fig. 11.24 (no simulations and do not be specific to the C5 process).

**A11.7** Repeat Ex. 13.4 (with lengths of 2 keeping the same widths). Use a load capacitance of 500 fF.

**A11.8** Design, lay out, and simulate the operation of a 3-stage buffer made using 20/10, 160/80, 1280/640 inverters (of course all MOSFETs have lengths of 2) using the MOSIS design rules (do an LVS to compare the layout against the schematic). Note you should have 3 cells for the inverters (rank 2) and one cell for the buffer (rank 3). Plot the propagation delay, using hand calculations, of the buffer, against load capacitance. Compare your hand calculations, on the same plot, against simulation results.

**A11.9** Simulate, and comment on the operation of the tri-state inverter in Fig. 11.27, using 20/2 PMOS and 10/2 NMOS (MOSIS design rules where L = 2 is the minimum size). Compare your simulation results to hand calculations for the delay for various load capacitances.

**A11.10** Estimate the delay from point A to point B in the following circuit. All MOSFETs have lengths of 1.

**A11.11** Suppose an inverter is driving a 10 pF capacitive load at 100 MHz. Neglecting the power dissipated by the inverter because of cross-over current (the current that flows from VDD directly to ground when both MOSFETs are on) estimate the power dissipated by the circuit. How much power is dissipated by the NMOS? By the PMOS? Show your work.

**Figure A11.10** Estimating the delay in a cascade of inverters.

In

20/20

50/50

200/200

Out

A

B