Course Project

The Packaging and Design of a USB Flash Drive

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ECG 721 – Memory Circuit Design

Introduction

- The purpose of this power point is to provide the reader with information about the design and packaging of a USB flash drive. This will include the transistor level architecture along with reading, writing, and erasing from the memory cell. Several other components will also be discussed that form part of the printed circuit board (PCB) and packaging.

Main parts of a USB drive

Figure 1

Figure 2 [1]

Main components of a common USB drive [1]

- USB plug connector, such as Type-B, Mini-USB, Micro-USB and Type-C
- USB Mass storage controller
- **NAND flash memory chip**
- Crystal oscillator

Why NAND Flash Memory for USB Drive

Flash memory can be electrically programed and erased with ease which is a type of electrically erasable programmable ROM (EEROM). The reason for the term "flash" is because blocks of memory array can be easily erased [4]. NAND is used for mass storage due to several advantages over NOR which include, capacity, speed performance, erase cycles, life span, and type of applications used on [2]. The performance of NAND flash for erase, write and read is far better than NOR type flash, which is the reason is used in applications such as PC cards, compact Flash, MP3 players, digital cameras, etc. If a NOR type memory bank has a capacity of 1MB -32MB, it's NAND type counterpart would have 16 times more capacity, because a NAND size cell is about half of a NOR cell [2]. Also, considering the same capacity a NOR type would be much slower (5 sec) compared to NAND which would be about 3msec [2].

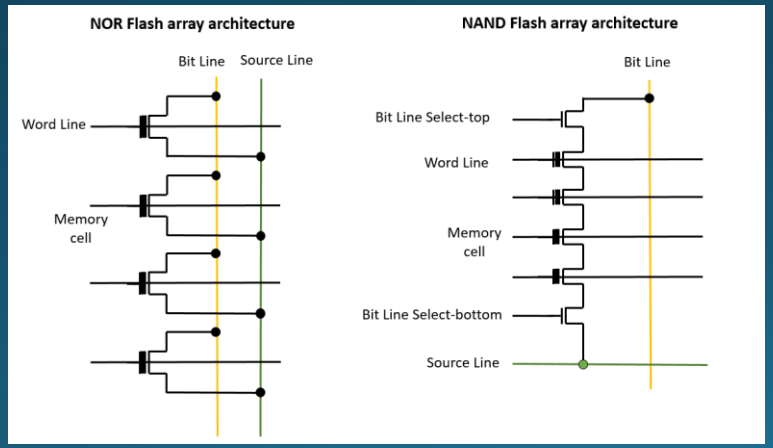
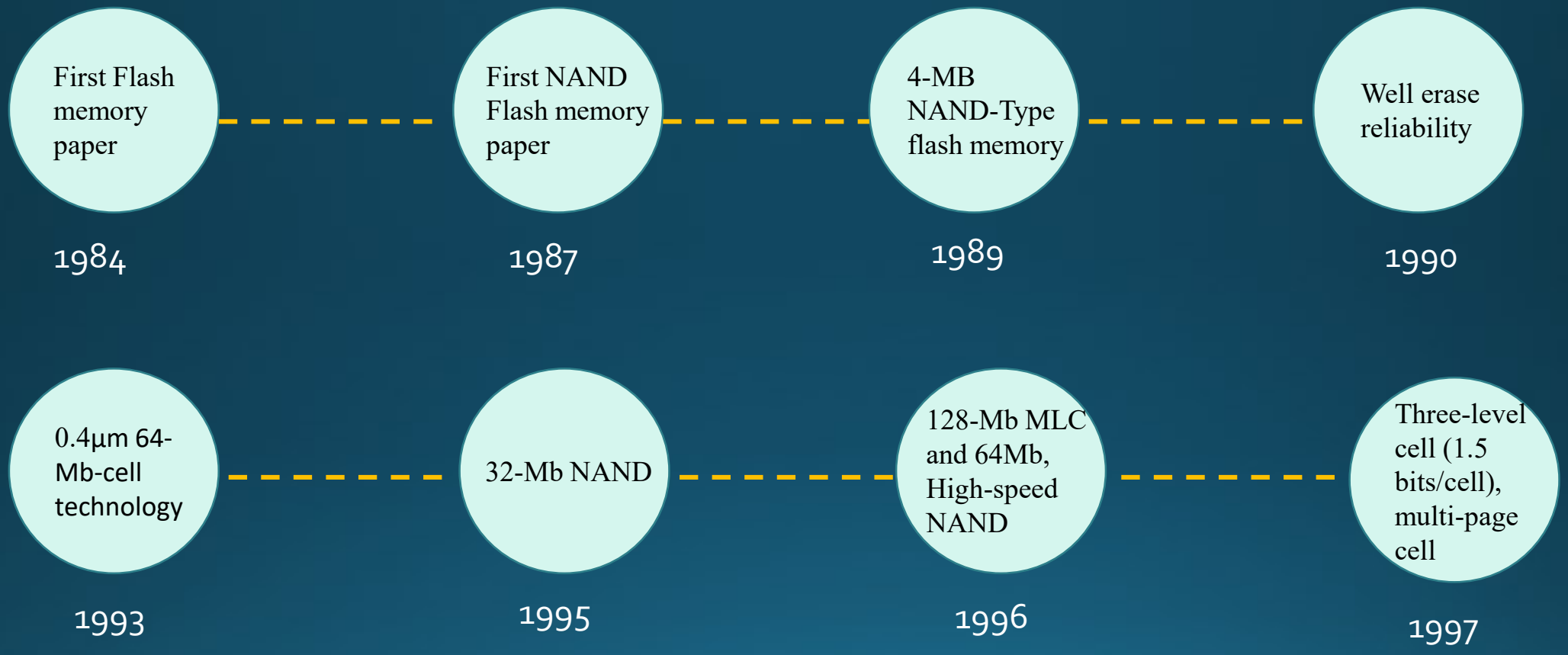


Figure 3: NOR and NAND Type Architectures

Some Historical Background of Flash Memory



The information above are only some significant breakthroughs, however there are many more discoveries within those years [3].

Single Cell Structure: Floating Gate

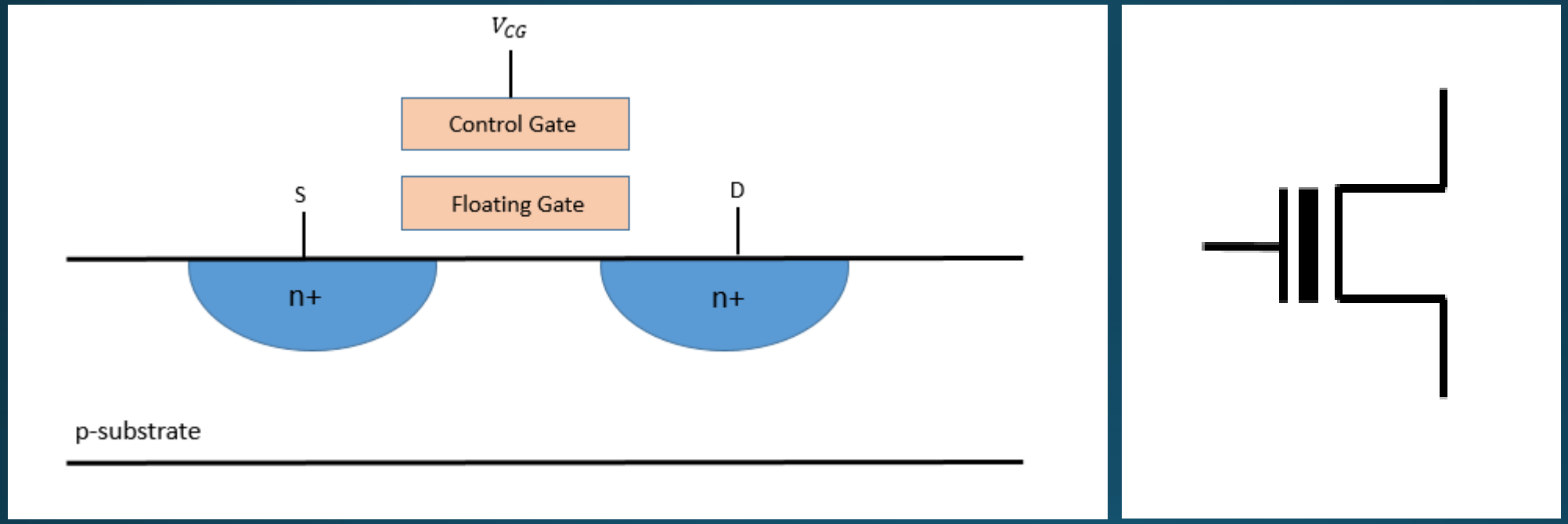


Figure 4

Figure 3 shows the floating gate structure and its symbol. This figure demonstrates the idea of controlling the threshold voltage of the MOSFET, which will be discussed in the next slides.

Programming and Erasing of a Cell

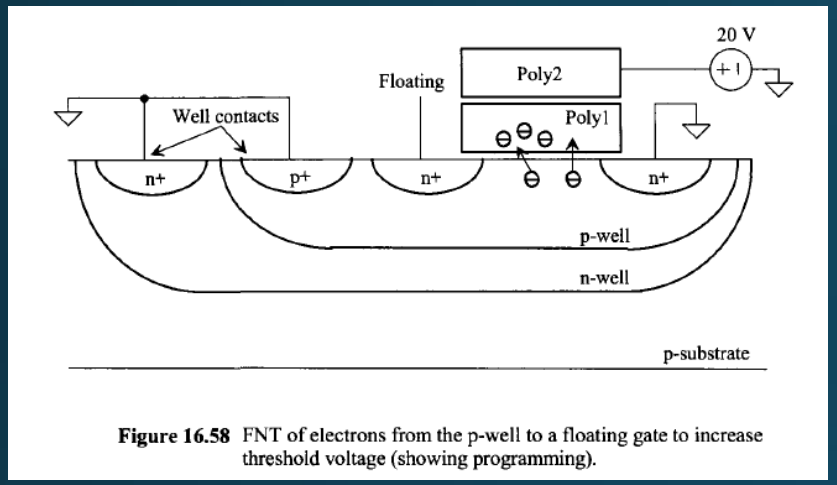


Figure 16.58 FNT of electrons from the p-well to a floating gate to increase threshold voltage (showing programming).

Figure 5 [4]

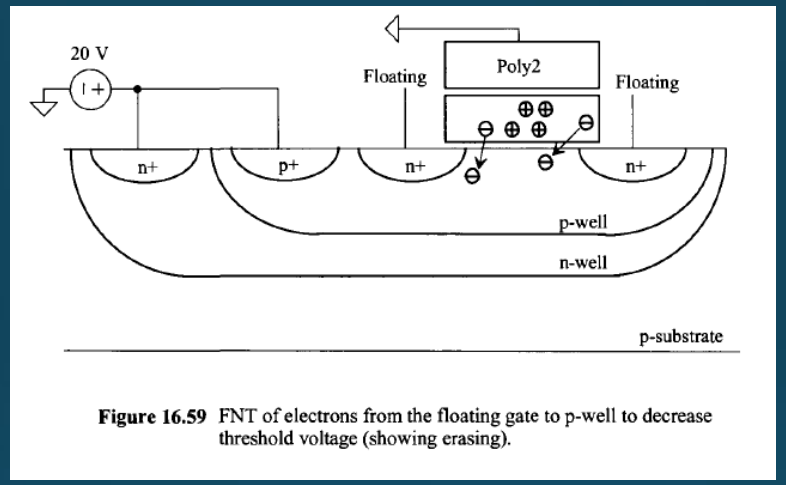


Figure 16.59 FNT of electrons from the floating gate to p-well to decrease threshold voltage (showing erasing).

Figure 6 [4]

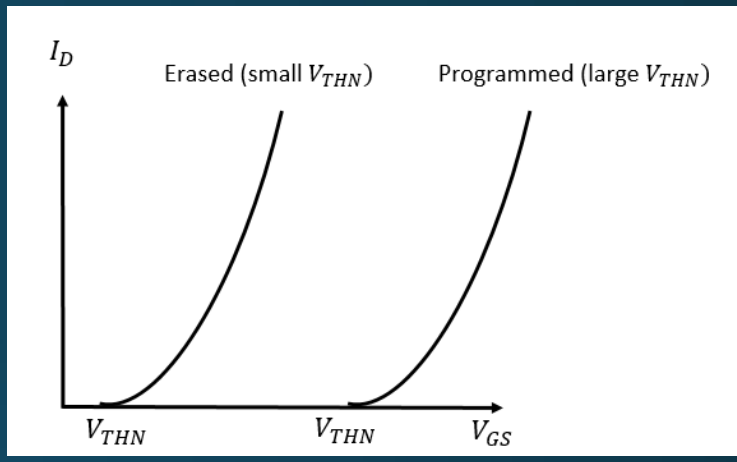


Figure 7 [4]

Figure 4 and 5 show the programming and erasing of a floating gate MOSFET by applying high voltage and using Fowler-Nordhein tunneling (FNT) [4]. Applying large voltage to the control gate push electrons into the floating gate (FG), programming, and applying large voltage to the double well pulls electrons from the FG, erasing. Figure 6 shows how this process increases and decreases the threshold voltage of the device. The double-well is used to prevent current flow through p-substrate because that would create irregular behavior of the overall memory.

Programming and Erasing in a String

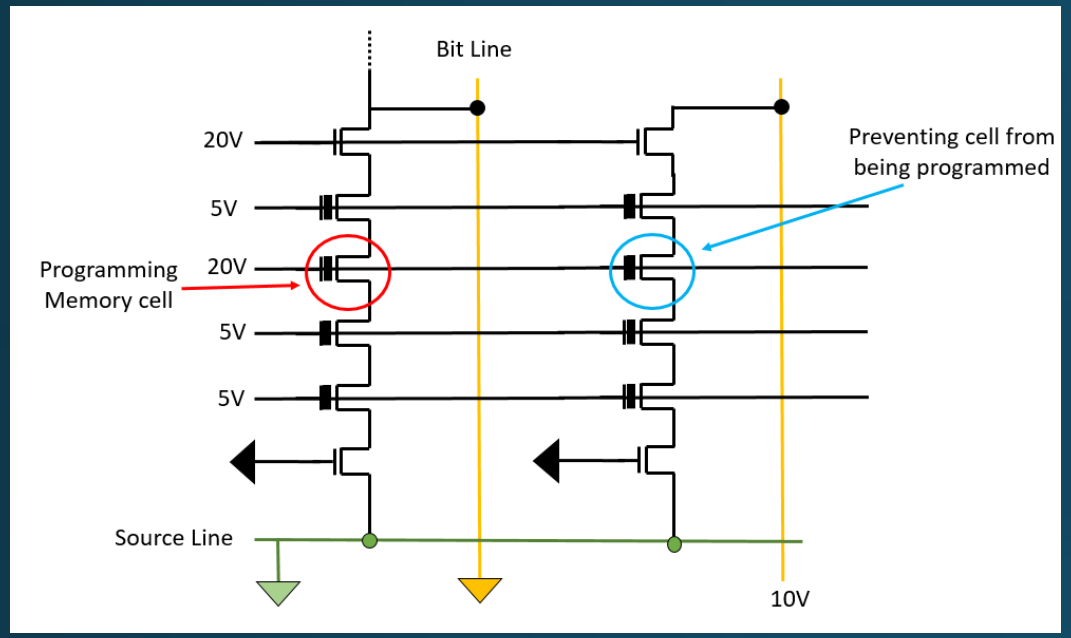


Figure 8

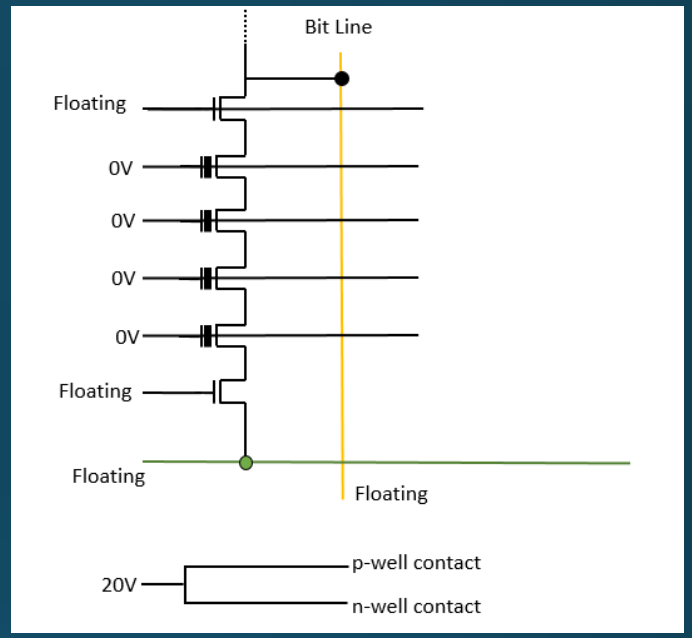


Figure 9

Figure 8 shows the programming of a memory cell in a string (let's say 4 bits). During the programming process the bit line, p-well and n-well contacts are connected to ground. The gate of the bottom select NMOS is grounded to have a floating gate in the string and all the other devices are set high. The memory cell being programmed is set to high voltage in order to increase the threshold voltage by using Fowler-Nordheim tunneling (FNT) [4]. Figure 9 shows the erasing operation; top and bottom select devices are floating, memory cell gates and bit lines are set low (0V), while the p-well and n-well contacts are set to high voltage (20V). This operation again takes advantage of FNT to remove electrons from the floating gates (erase) and change the threshold voltage as needed.

Programming and Erasing an Array

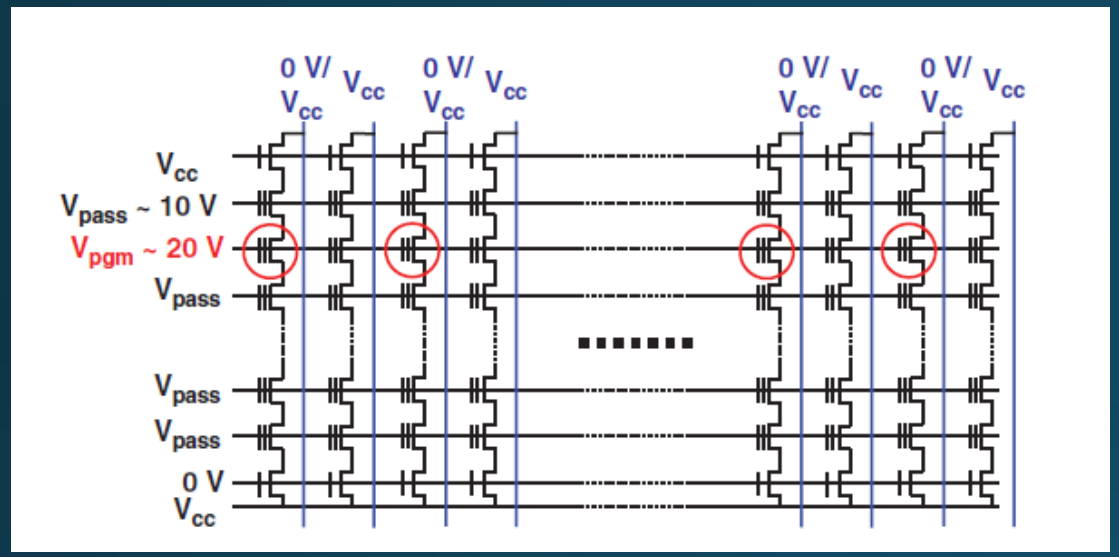


Figure 10: Programming an Array [4]

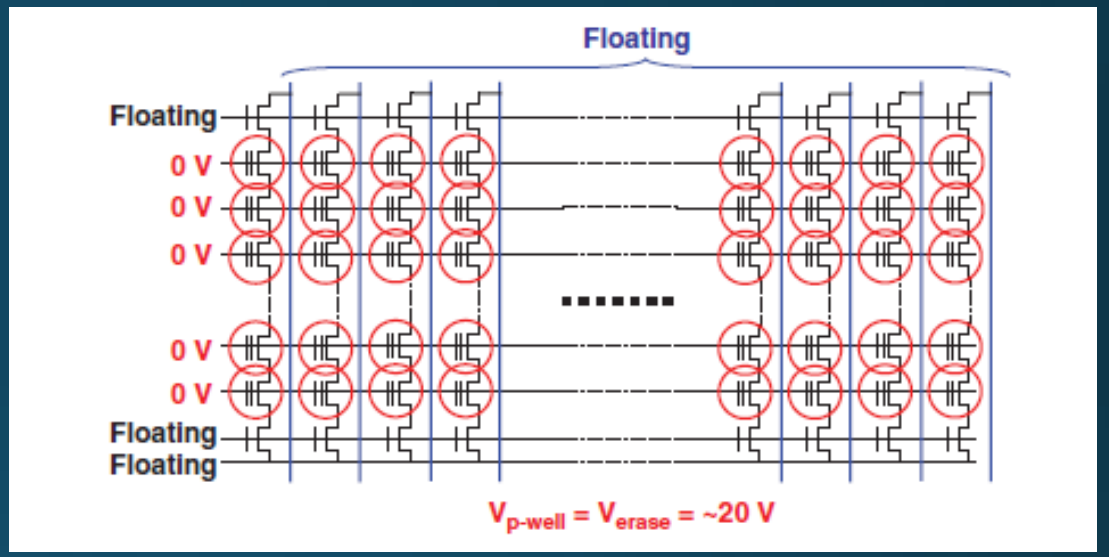


Figure 11: Erasing an Array [4]

Programming the device (USB drive) takes much longer than reading out the bits because programming takes an extra few steps to verify the voltage levels as is being programmed [4].

Reading Process

Let's say a 1 is 5V and 0 is 0V. Also, AR0-R2 is programmed and AR3 is erased.

Let's say we want to read the value in RA3.
If 5V is applied to RA0, RA1 and RA2, and 0V to RA3, then only RA3 is OFF, which means the charge on the bit line stays the same and does not discharge. Thus, the value when reading out the bit line is 1, meaning RA3 has a 0 stored.

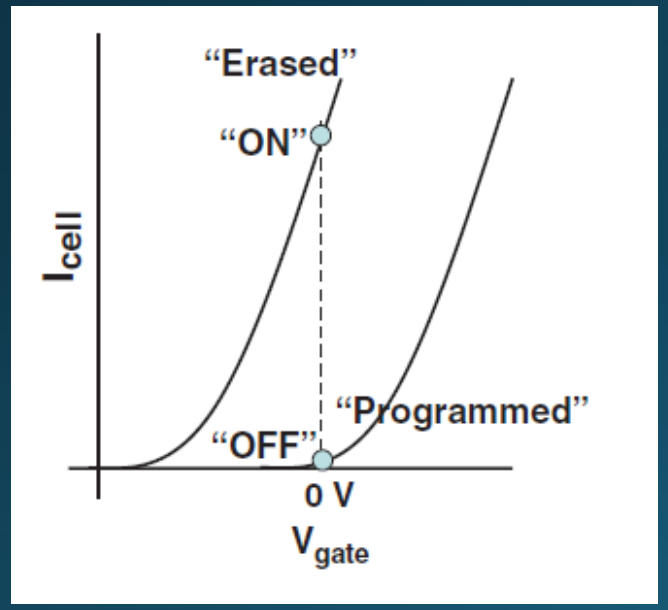


Figure 12 [3]

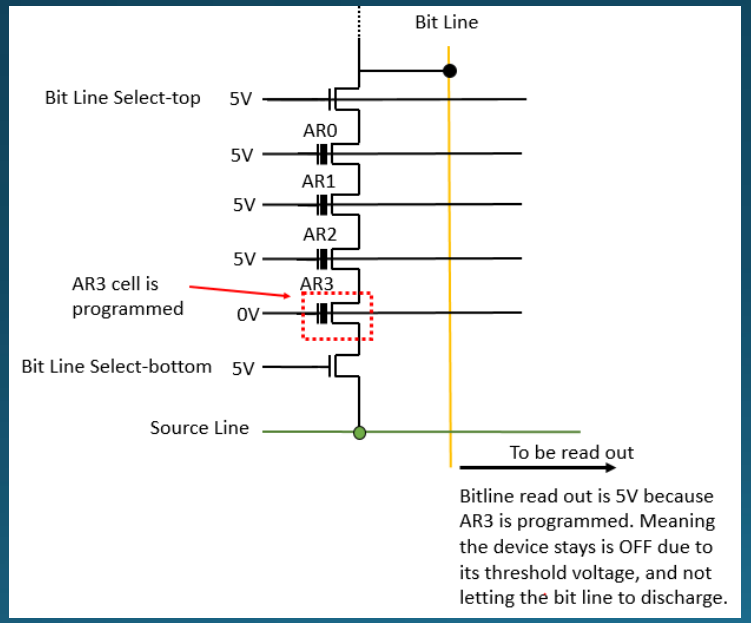


Figure 13 [4]

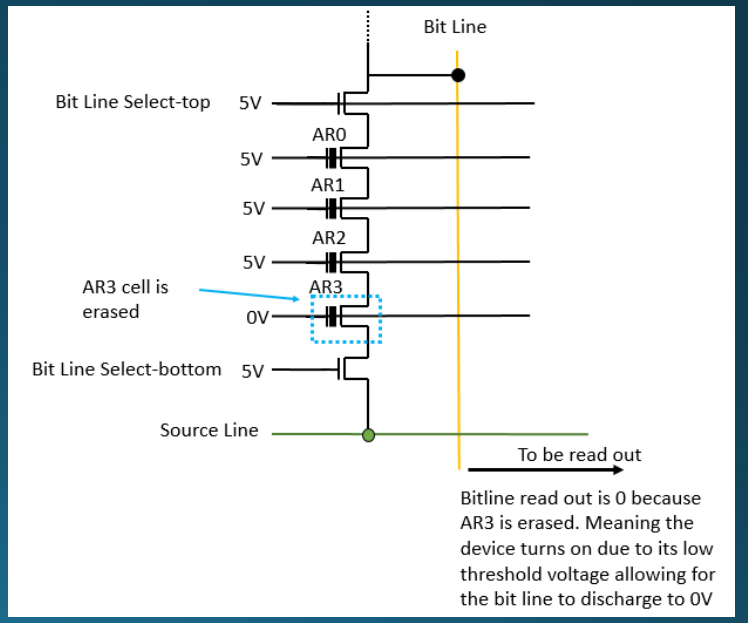


Figure 14 [4]

Let's expand the structure idea to 3D NAND Flash Memory

This 3D arrangement is a "Stack" process by using a cylindrical structure. There are several 3D NAND cell concepts; some of those concepts are BICS/P-BiCS, TCAT, Smart, SMArT, VG-NAND, and DC-SF [3]. However, here only the BiCS (bit cost scalable technology) will be discussed.

The main idea is to take the serial string of devices and stand it in a vertical position

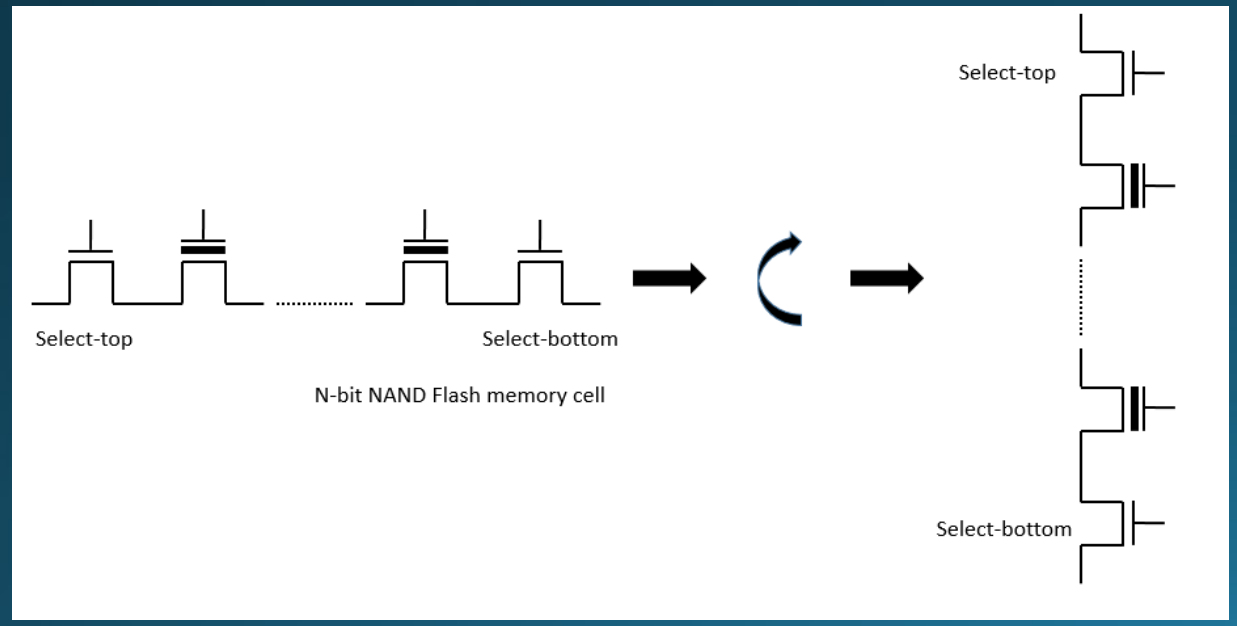


Figure 15

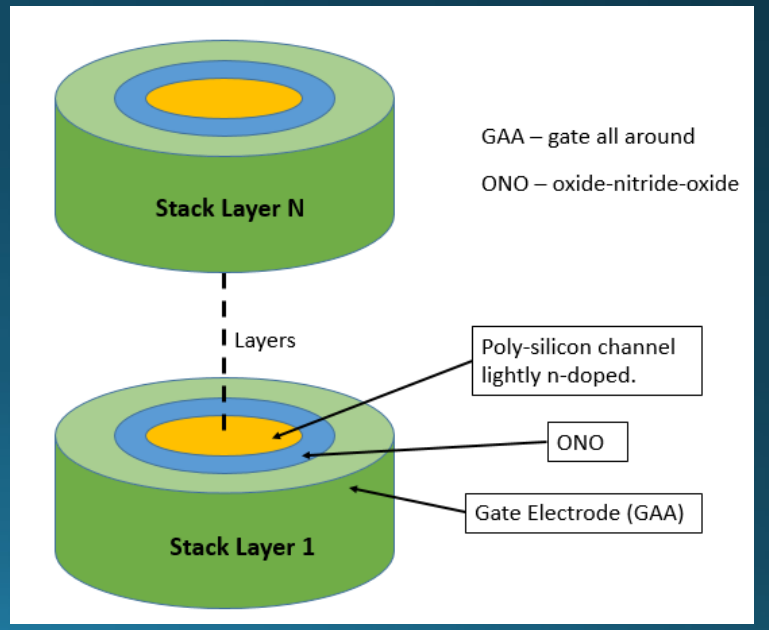


Figure 16

BiCS (bit cost scalable) Flash Memory

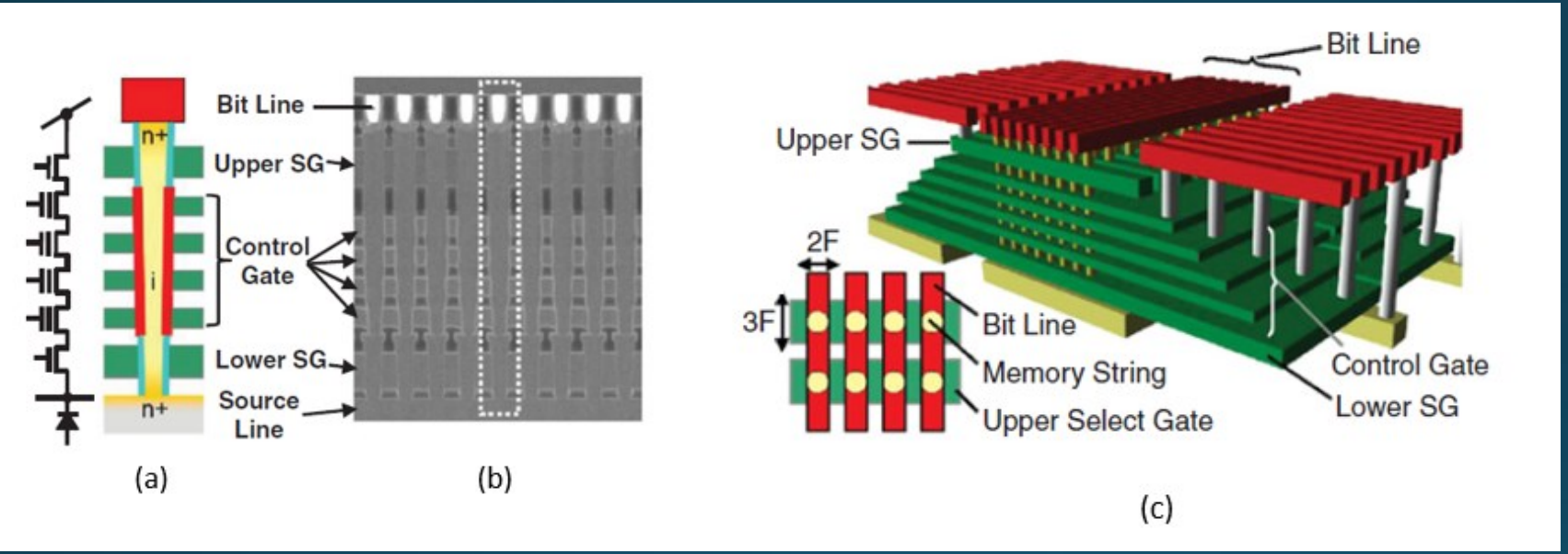


Figure 17

Figure 17 (a) Memory String. (b) Cross-sectional SEM image of BiCS flash memory array. (c) Bird's eye view and top-down view of BiCS flash memory array [3].

16-Gb BiCS Die with Peripheral Circuit

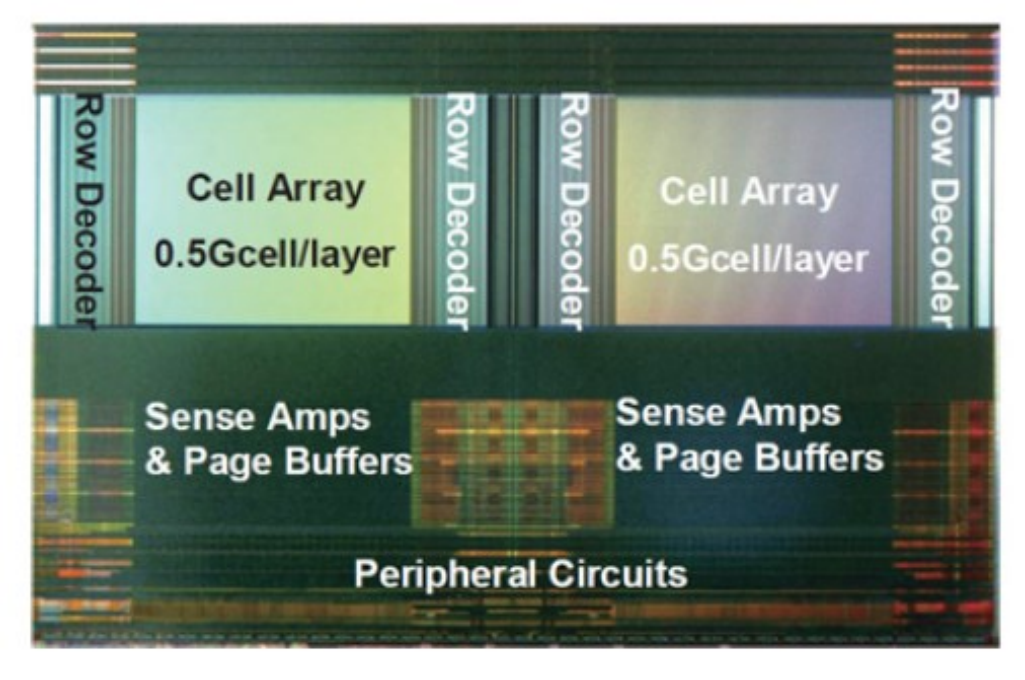


Figure 18

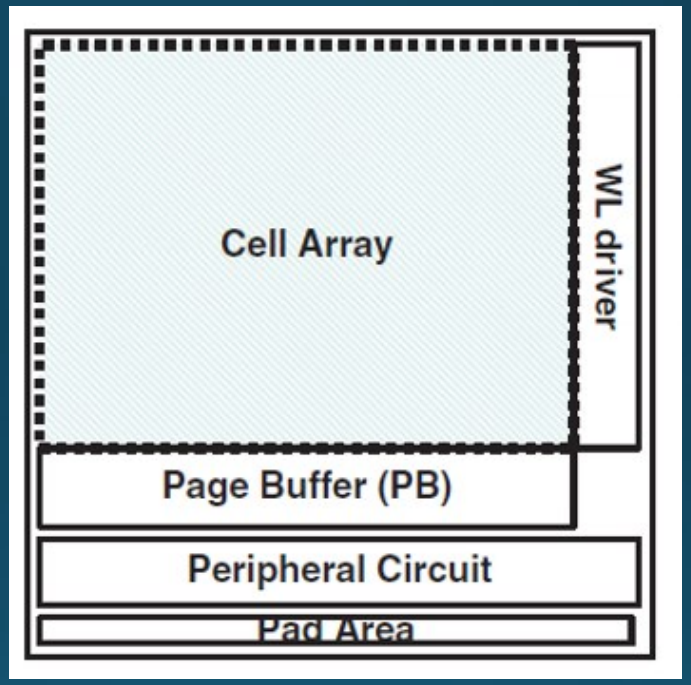


Figure 19

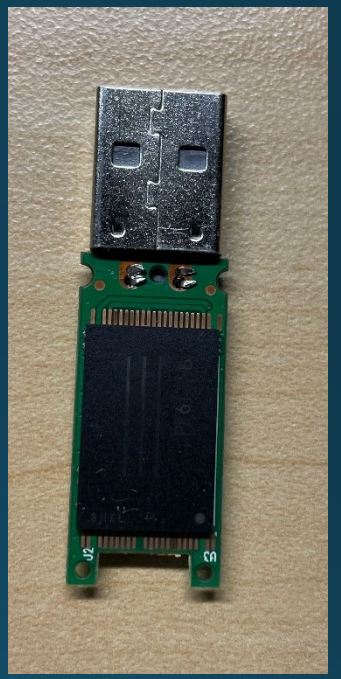


Figure 20

Figure 18 shows a micrograph of a 16-Gb test chip. The number of cells in one string is 32 in 16 stacked control gate layers [3]. Figure 19 shows the layout of a conventional chip layout and figure 20 is the actual memory chip solder to a PCB (figure 1 without the casing).

Main Peripherals of USB Flash Drive

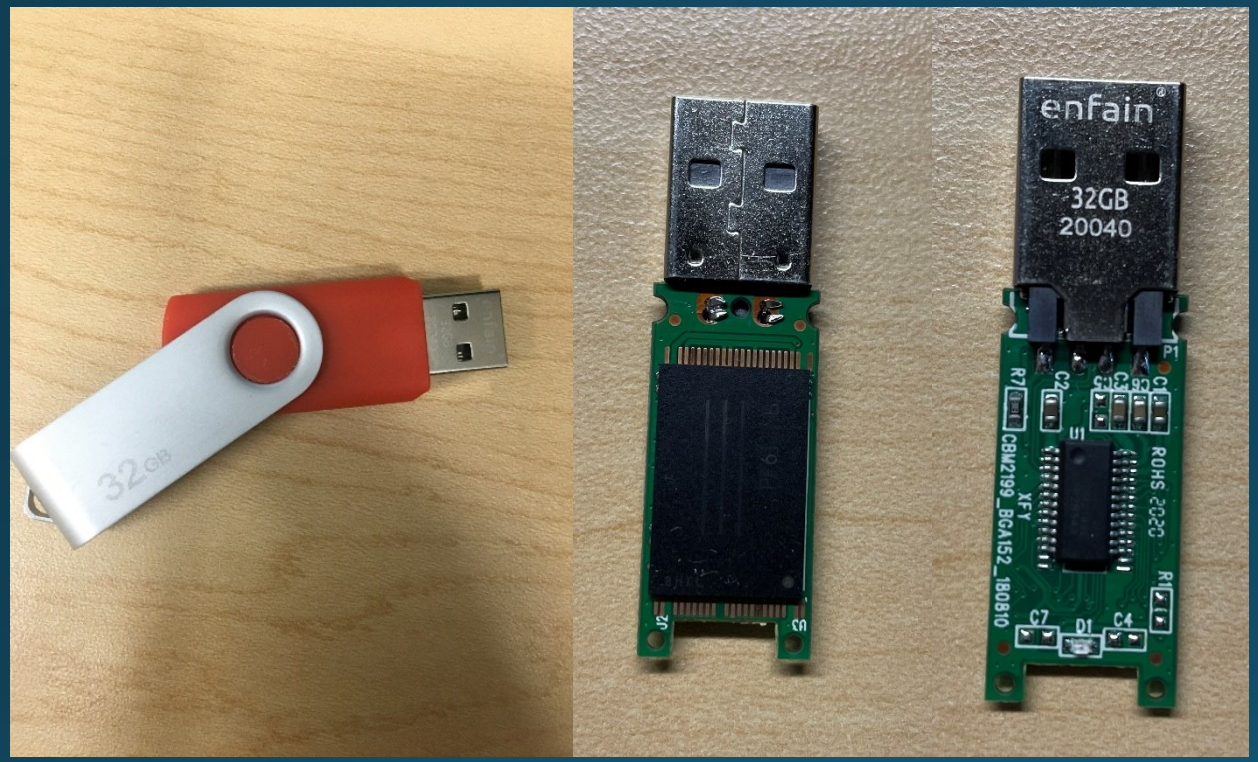


Figure 21

Figure 21 shows the casing, memory chip and memory controller. This USB drive contains 32GB of memory. This memory die is enclosed in a ball grid array (BGA) package. The controller chip package is the small-outline integrated circuit (SOIC) type.

Steps in the Fabrication of a Memory Chip

- Circuit Design
- Technology Development
- Fabrication (Fab)
- Wafer Probing
- Assembly
- Final Chip Test

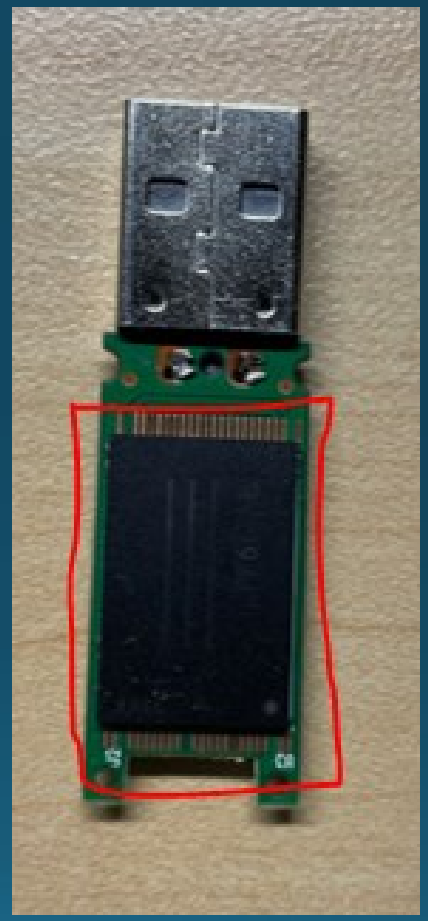


Figure 22

Fabrication of a Memory Chip: Circuit Design

- The first step is the design of the memory cell array blocks and memory peripherals.
  - A design software editor or an electronic design automation (EDA) system such as Cadence can be used in this step.

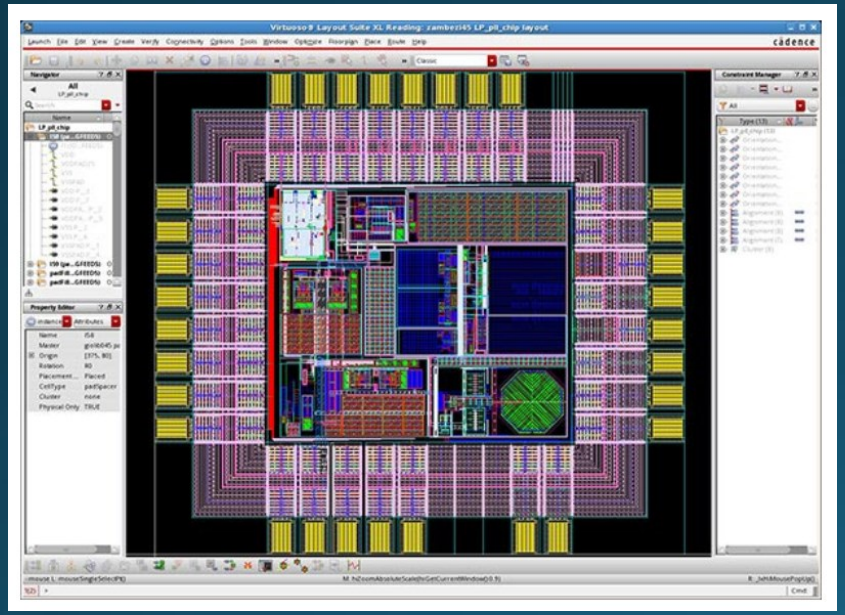


Figure 23

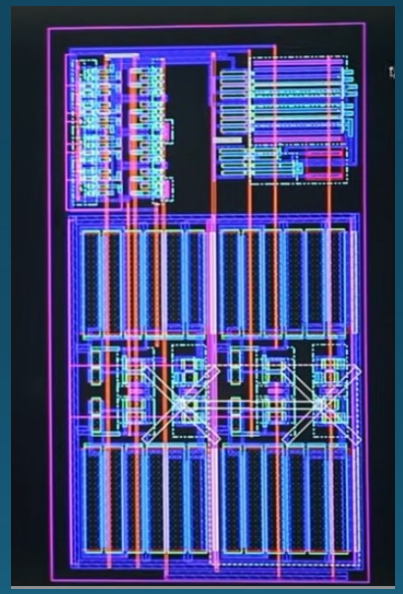


Figure 24

The figures above show a layout design of a memory chip using Cadence EDA [6]

Fabrication of a Memory Chip: Technology Development

- The second step describes the work flow that will be chosen to manufacture the die.
  - Timeline of fabrication process
  - Software to test certain parameter of the physical design
  - Test chip samples are made until final approval before mass production
  - Actual fabrication of large quantities of memory chips

Fabrication of a Memory Chip: Actual Fabrication (Fab)

- This step is the physical production of memory chips made from a silicon wafer
- A fabrication company (Fab) such as Taiwan semiconductor manufacturing company (TSMC) build chips from silicon wafers in huge clean rooms with state of the art technology.
- Photolithography
  - This practice uses extreme ultraviolet (EUV) along with a mask and photo-resistive material to basically print the design that was specified in the design step [8].
- Film Etching
  - The removal of thin material using techniques such as wet and dry etching [4].
- Film Deposition
  - The addition of different material to grow the circuit using procedures such as physical vapor deposition (PVD) and chemical vapor deposition (CVD) [4].

Fabrication of a Memory Chip: Wafer Probing

This step uses a probe card and computer software to test each die on a silicon wafer [7].

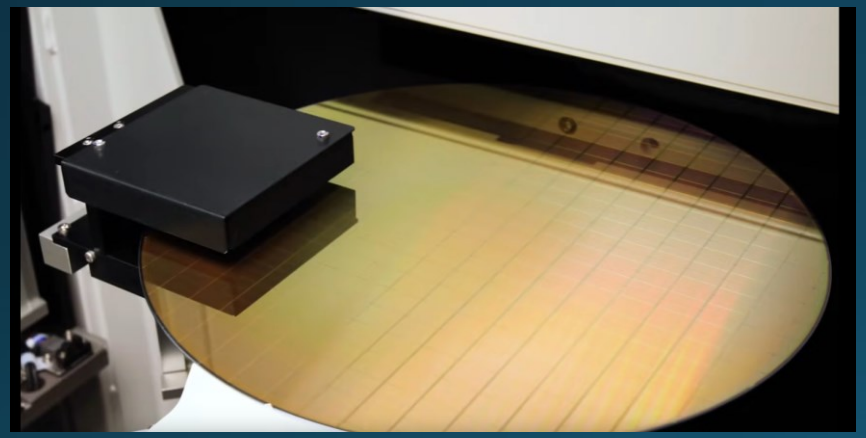


Figure 25

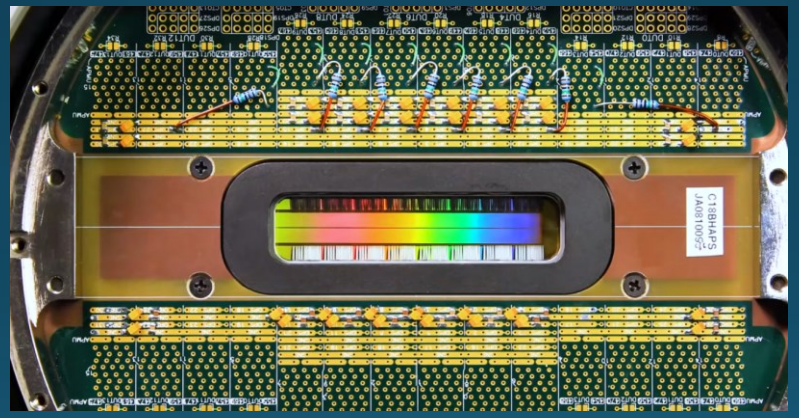


Figure 26

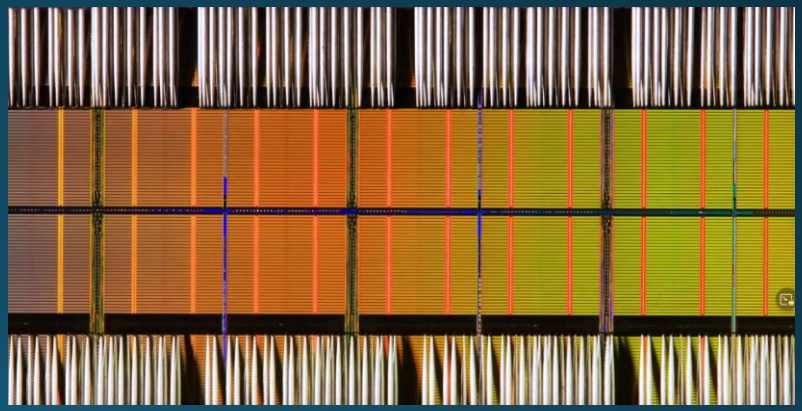


Figure 27

The figures above show the wafer, probe card, and probe needles [7].

Fabrication of a Memory Chip: Assembly

- First wafers are pack with a special thin adhesive and separated into individual die using a diamond edge saw [8].
- Each die is picked an placed on a printed circuit board (PCB).
- An automated wire bonder using solid gold wire makes all the connections from the die to the circuit board.
- Special epoxy mold compounds (EMC) are used to encapsulate and protect the die [8].

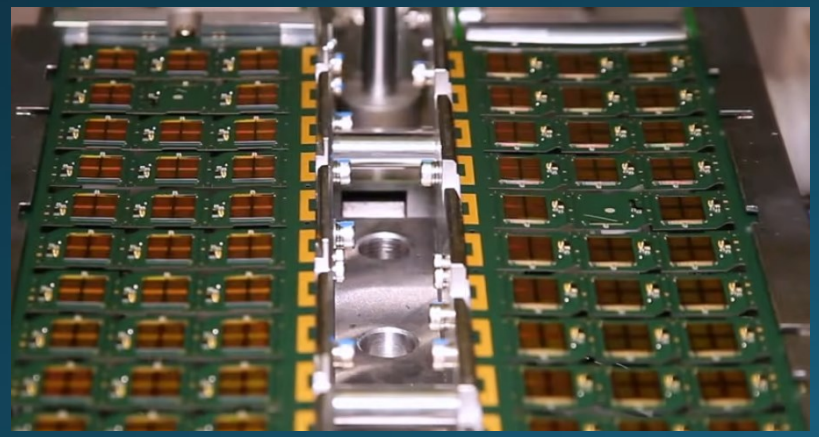


Figure 28

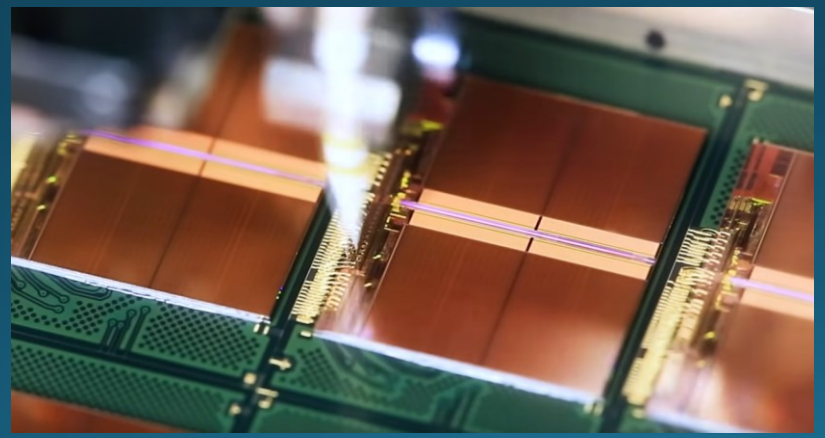


Figure 29

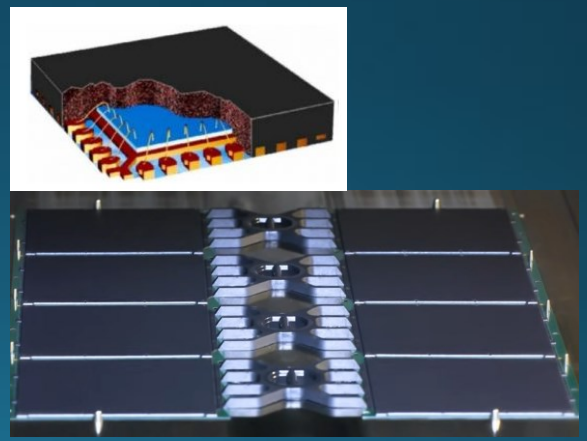


Figure 30

https://polymerinnovationblog.com/polymers-electronic-packaging-part-one-introduction-mold-compounds/

Fabrication of a Memory Chip: Final Chip Test

Memory chips follow many different test to make sure proper operation of device. Some of those are communication, stress, and temperature tests [7].

Figure 31

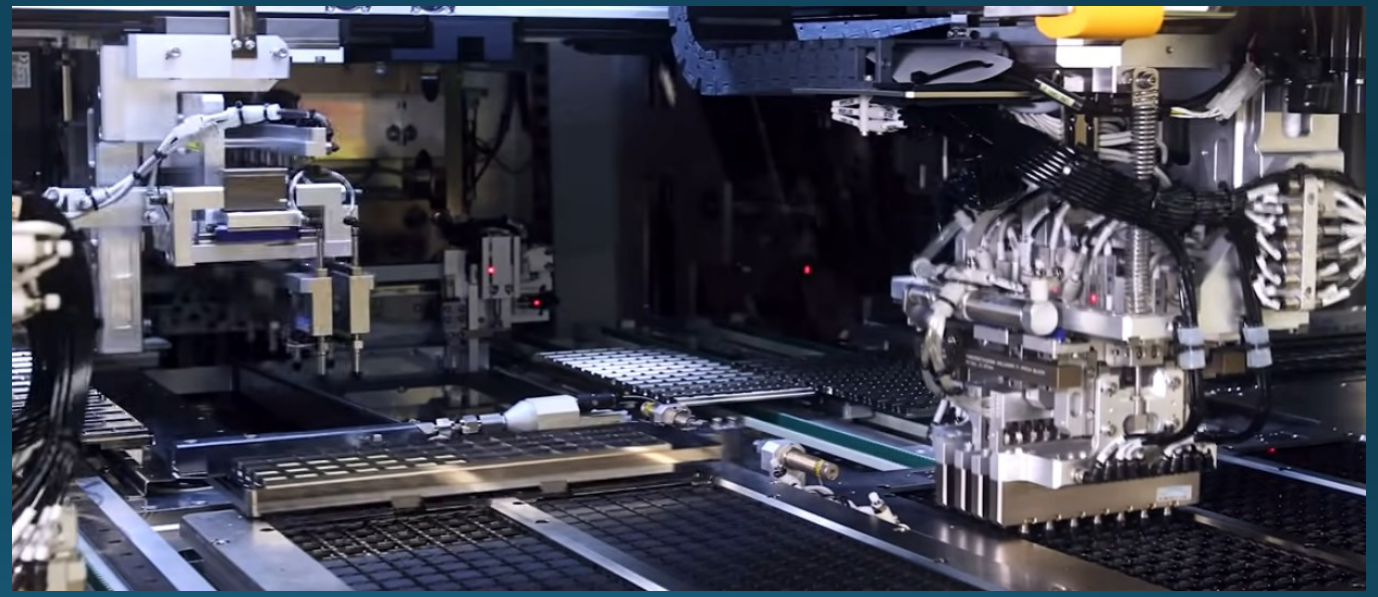


Figure 32

Figure above show several tests being done on chips before final packaging for distributors.

Fabrication of the Memory Chip Controller

The same steps are applied to the memory chip controller as the memory chip explained before, except the chip package and molding is different since this is a small-outline integrated circuit (SOIC) package.

Figure 33

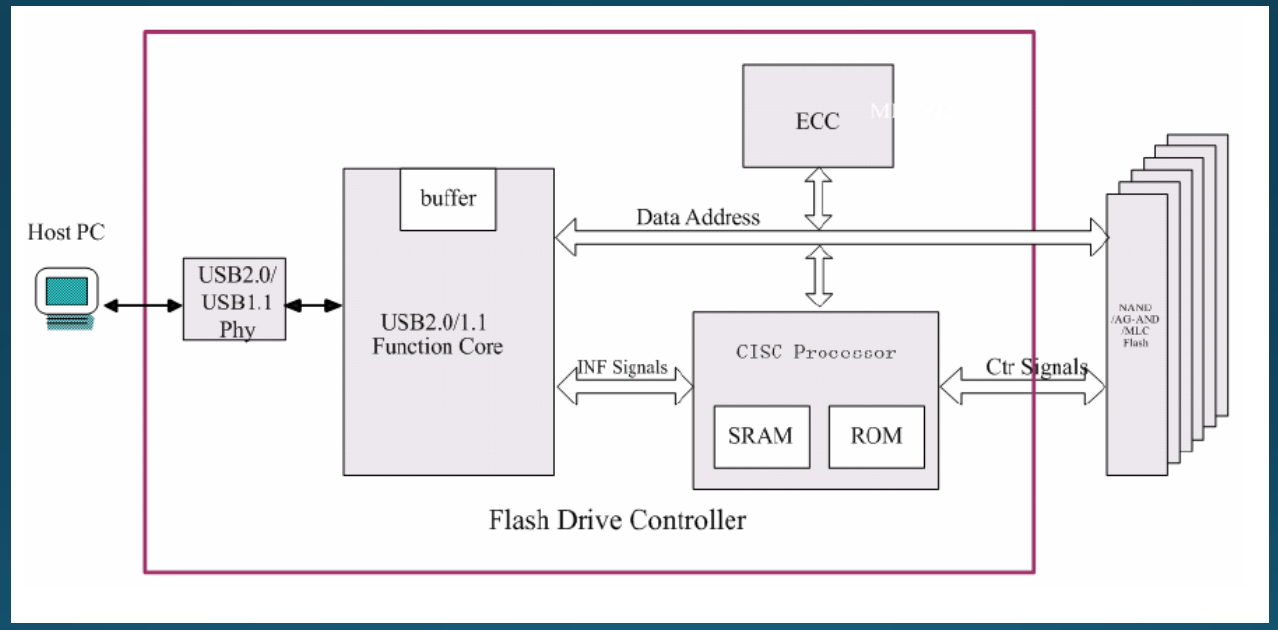


Figure 34 [9]

Figure 33 above show the memory chip controller and figure 34 shows its block diagram.

Fabrication of the Printed Circuit Board

Steps in the Fabrication of a printed circuit board (PCB) [10]

- Step 1 – Design Gerber files
  - Once the schematic and layout Gerber files have been received by the PCB factory, a raw FR-4 (fiberglass) copper clad PCB is cut and processed.
- Step 2 – Design Film
  - A photo resist film having the shape of the design is laser cut which will be used to attach it to a blank PCB and print the layout design on top of it.
- Step 3 – Printing Inner layers
  - The copper piece with the printed design goes through an alkaline solution to chemically remove extra copper and photo resist and leaving behind only the design to be processed according to each layer.
- Step 4
  - All the layers follow through an automated optical inspection (AOI) for alignment and etching errors [--].
- Step 5 - Layer-up and bond
  - All the PCB stackup layers from the design are bonded together using epoxy pre-impregnated (prepreg) process to sandwich into one single PCB board with several layers and fiber glass in between.

Fabrication of the Printed Circuit Board

Steps in the Fabrication of a printed circuit board (PCB) [10]

- Step 6 – Drill
  - During this step all the vias and mounting holes are drilled and each PCB fabricator charge a different amount per number of drilling and finished type.
- Step 7 – Copper Plating
  - A copper bath is added to the board after to cover and filled with copper the vias and holes that were drilled in the last processed.
- Step 8 – Outer Layer Imaging
  - This follows the same process as step 3 except an extra process is added here under a yellow room and UV light. A photo resist film of the design is attached to the outer blank copper layer and exposed to UV light to apply a print copy of the layout design on top and bottom of blank PCB.
- Step 9 – Outer Layer Plating
  - Here the outer layers are electroplated with a thin coat of copper
- Step 10 – Final Etching
- Step 11- Solder Mask Application
- Step 12 – Surface Finish
- Step 13 – Silkscreen
- Step 14 – Electrical Test

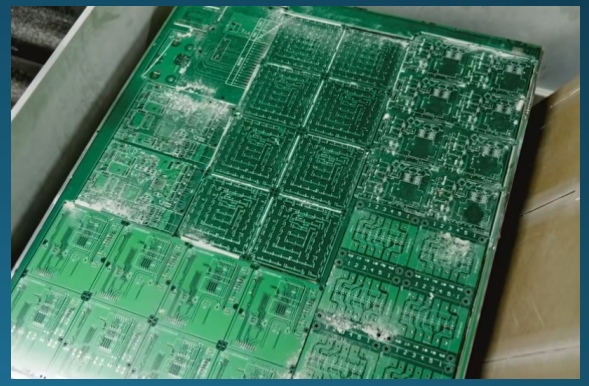


Figure 35: Finished PCB panel

PCB Assembly Process

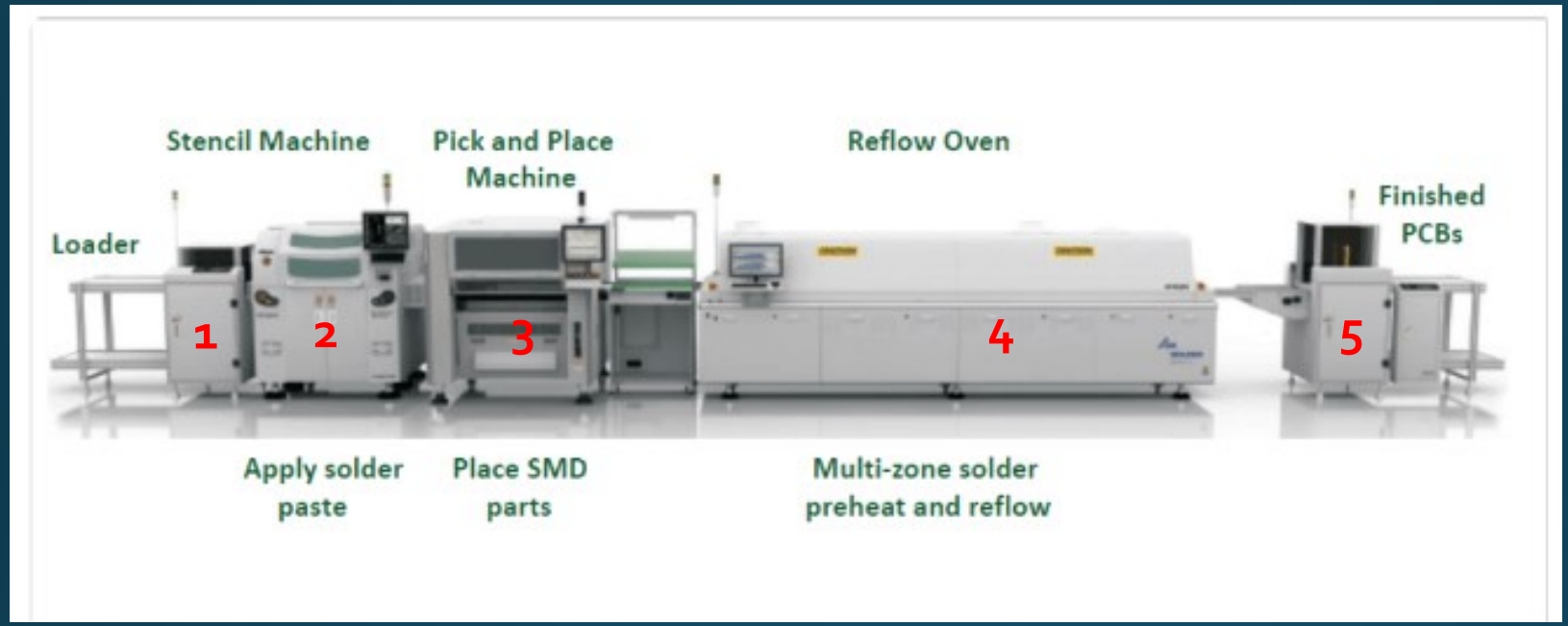
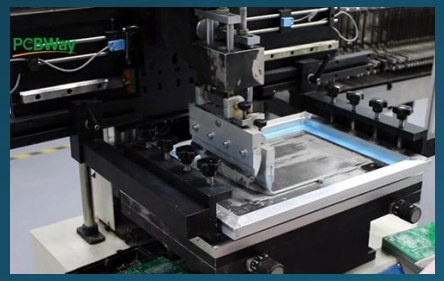


Figure 36: Basic PCB assembly line [11]

1) SMT PCB loader

2) Stencil Printing



3) SMT Yamaha M20

4) SMT Reflow oven

5) Finished loader

Output result

Conclusion

A discussion of the design and packaging of a USB drive was presented in this power point. Several design aspects were analyzed such as the basic structure of a cell and the reason for using NAND flash topology for mass memory devices. The single cell floating gate structure was discussed, as well as the programming, erasing and reading of a string and array of cells. Also, the basic structure of 3D NAND flash memory was considered. Other several topics were explained such as the fabrication of a memory chip (die) from a silicon wafer and the chip packaging assembly. Last, the fabrication of the printed circuit board (PCB) and the process to populate a board in the assembly line to have a complete USB flash drive were concluded.

References

[1] "What's Inside A USB Drive? - Premium USB". [Online]. Available: https://www.premiumusb.com/blog/whats-inside-a-usb-drive. [Accessed: NOV. 25, 2021].

[2] "Two Technologies Compared: NOR vs. NAND," M-Systems Flash Disk Pioneers, Israel, White Paper, 2003. [Online]. Available: http://www.maltiel-consulting.com/Nonvolatile_Memory_NOR_vs_NAND.pdf

[3] Aritome, Seiichi. *NAND Flash Memory Technologies*, John Wiley & Sons, Incorporated, 2015. *ProQuest Ebook Central*, https://ebookcentral.proquest.com/lib/unlv/detail.action?docID=4187185.

[4] R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation,* 4th ed. Hoboken, New Jersey: John Wiley & Sons, Inc., 2019.

[6] Cadence Design Systems, Inc., "Virtuoso Layout Suite," *Cadence.com*. [Online]. Available: https://www.cadence.com/en_US/home/tools/custom-ic-analog-rf-design/layout-design/virtuoso-layout-suite.html

[7] "Making Memory Chips – Process Step," *You Tube*. MicronTechnology, Jul. 28, 2017. [Video recording]. Available: https://www.youtube.com/watch?v=M-wNC3Z3ZX4

[8] "EUV: Lasers, plasma, and the sci-fi tech that will make chips faster | Upscaled," You Tube. Engadget, Jan. 1, 2020. [Video recording]. Available: https://www.youtube.com/watch?v=oIiqVrKDtLc

[9] Chipsbank Microelectronics, "Fastest & Secure USB 2.0/USB1.1 Flash Disk Controller with Dedicated 32-bit Microprocessor," CBM2080/CBM1180/CBM1183/CBM2075 datasheet, Mar. 2005.

[10] "PCB Manufacturing Process – A Step-by-Step Guide". [Online]. Available: https://www.pcbcart.com/article/content/PCB-manufacturing-process.html. [Accessed Dec. 1, 2021].

[11] "What machines are required for PCB assembly production," *PCB Assembly UETPCBA*. [Online]. Available: https://uetpcba.com/pcb-assembly-machine/. [Accessed Dec. 1, 2021].