Additional end-of-chapter problems for Chapter 17 – Sensing Using ΔΣ Modulation

*CMOS: Circuit Design, Layout, and Simulation*

**A17.1** Redesign the sensing circuit seen in Fig. 17.18 using the topology seen below.

a) Derive the equations governing the circuits’ operation.

b) Comment on the limitations on the amplitudes of the bitline voltage and the issues a practical circuit will face with variations in the bias current.

c) Show, using SPICE, how your design operates. Note that the Flash memory cells can be modeled with current sinks (you select reasonable values).

d) Under ideal conditions (M1 having infinite output resistance) is M4 needed? Verify your

answer with SPICE.

e) Suggest a modification to the design to keep M1 from shutting off. Verify your answer with SPICE.

f) Is the comparator's performance critical? Attempt to simplify the circuit and reduce power by using a very simple comparator. Simulate the operation of your design.

**Figure A17.1** An alternative DSM sensing circuit.

*Ibias*

*VDD*/2

*VDD*

*VDD*

*Q*

Fig. 17.16

*clock*

M1

M3

M4

*Cbit*

*Vbit*

*Row1*

*Row2*

*Row3*

*clock*

Flash memory

**A17.2** Derive the relationships governing the operation of the circuit seen in Fig. 17.8 including the voltage swing on the bitline.

**A17.3** Redesign the circuit seen above in Fig. A17.1 using a DFF in the place of the clocked comparator. Derive the equations governing your design’s operation. Verify your circuits operation using SPICE. Comment, and show, that your DFF design is tolerant to metastability.

**A17.4** Show, using equations, the details of how *VR* and *VI* are related to *M* and *N* for the circuit seen in Fig. 17.36.