Additional end-of-chapter problems for Chapter 16 – Memory Circuits

*CMOS: Circuit Design, Layout, and Simulation*

**A16.1** What would happen to the bitline capacitance if the column conductor in Fig. 16.2 is moved upwards away from the substrate?

**A16.2** Would you expect the capacitance of the metal bitline to substrate to be greater than or less than the capacitive loading from the isolation devices connected to the column line? Why?

**A16.3** The resistance associated with the metal line labeled *NLAT* in Fig. 16.17 can be significant. Why not add MOSFETs at the bottoms of every NSA to avoid this resistance? (hint: look at the ground conductor for these added MOSFETs.)

**A16.4** Why do the voltages on the bitlines in Fig. 16.8 dip below *VDD*/2 when *Eq* shuts off? Show, using SPICE, how the magnitude of this dip can be increased by reducing the bitline capacitance. Describe what is going on.

**A16.5** Describe in your own words and in detail what is happening at the various times in Fig. 16.14 (what are the signals, what do they do, and why when opening a row in a DRAM array).

**A16.6** Estimate, using hand-calculations, the minimum operating voltage of the sense amplifier in Fig. 16.72. Verify your estimate with simulations. How do input voltages affect the operation of the sense amplifier? What is the minimum voltage the sense amplifier can resolve if its outputs must switch to valid logic levels within 2 ns?

**A16.7** Repeat problems 16.10 and 16.11 if the size of the input/output word is increased to 4-bits. How many bits do we need for addressing?

**A16.8** Estimate the bitline capacitance if the length of the column line is 40 m, the depletion capacitance associated with an NMOS S/D to substrate is 100 aF, and the capacitance from a single column line to the 256 wordlines in the array is 200 aF. Sketch, on a cross-sectional view, these capacitances.

**A16.9** Using the 50 nm process estimate, using simulations with 10/2 devices, the maximum threshold voltage mismatch that can be tolerated in an NMOS sense-amp, Fig. 16.70, for correct sensing when the sensed signal is greater than or equal to 5% of VDD (50 mV). Comment on your simulation setups and your assumptions.

**A16.10** If an access device has 1 ohm resistance across its gate and a capacitance, to ground, of 5 fF estimate the delay to drive the word line high if there are 512 columns. Verify your answer in SPICE using an RC transmission line.

**A16.11** Lay out a DRAM mbit cell using the MOSIS design rules where the NMOS access device has a width of 10/2 and the capacitor is a 10/10 NMOSFET. Discuss the connections (how you connect the bitline, word line, and VDD/2) to the cell. Show that your cell LVSs okay.

**A16.12** This problem is concerned with simulating the operation of the DRAM sense (read) and write circuitry. Consider the section of a DRAM seen below. Make sure your simulation results are extremely clear (use pencil to label the plots to aid in clarity if needed). Turn in terse netlists AND CORRESPONDING COMPLETE SCHEMATICS without SPICE models for each simulation (with short discussions on what you did in the particular sim to answer the question). Use 20 fF for the Mbit capacitors, 100 fF for the bitline capacitance, and 200 fF for the I/O line capacitances.

**Figure A16.12** Simulating sensing and writing in a DRAM.

*ACT*

*EQ*

*VDD*/2

*NLAT*

*I*/*O*

*I*/*O*

*Row* 1

*Row* 2

*Col* 1

a) Suppose both DRAM cells contain logic zeroes. Starting with all decoder outputs at ground (that is, Row1, Row2, and Col1 are at 0 V), EQ high, NLAT floating (n\_sense at ground), ACT floating (p\_sense at VDD) use spice to show how you would read out the contents in the cell associated with Row2. Show how the cell is refreshed and how the I/O lines change values. Make sure your simulation output plots are labeled (e.g. EQ shuts off, row goes to VDDP, NSA fires, etc.) Use pulse sources for the signals Col1, Row1, Row2, EQ, n-sense, p-sense.

b) Show how you would write a logic one to the cell on Row 2. Use pulse sources to drive the I/O lines. Your outputs should show how the sense amplifiers help regenerate full logic levels on the digit lines (to compensate for the threshold drop through the I/O devices). Note that if your I/O transistors aren't wide enough you will not be able to switch the sense amplifiers when they are on (NLAT at ground and ACT at VDD).

c) Finally, design a sense amplifier for the I/O lines. When doing a read we know that the largest voltage we can pass through the I/O lines is *VDD* *VTHN*. Use a separate equilibrate signal for your sense amplifier. Precharge the I/O lines to VDD/2. Don't forget the 200 fF of parasitic capacitance hanging on the I/O lines. Make sure you comment on your choices (pros and cons).

**A16.13** Discuss, in your own words, the advantage of precharging the bit lines to *VDD* in a 6T SRAM high. What are the drawbacks? Is there any advantage if an SRAM cell using polysilicon pull-up resistors is used? Simulating the operation of reading an SRAM cell. Show your schematics and state all assumptions. Are n- or p-sense amplifiers needed? Why or why not? Use the simulations to support your comments.

**A16.14** Looking at Figs. 16.58 and 16.59 would it be possible to only have a single well for either erasing or programming a floating-gate memory? Why or why not? Use cross-sectional views to support your answers.

**A16.15** Problem 16.19 shows one method of sensing in a Flash memory. Do a literature search and document/discuss the operation of other sense amplifier topologies found in Flash memory (both NOR and NAND type cells).