Additional end-of-chapter problems for Chapter 10 – Models for Digital Design

*CMOS: Circuit Design, Layout, and Simulation*

**Unless otherwise indicated use the 1 m process parameters from Table 6.2 on page 147.**

**A10.1** Estimate the charge supplied by the input pulse in the following circuits. What is each circuits’ input capacitance? Add a 1k resistor in series with the input and use SPICE to verify your hand calculations (hint: integrate the current supplied by input pulse source to determine the charge supplied by the source.) Why do you need the resistor?

**Figure A10.1** Estimating input capacitance with an added Miller capacitance.

10/1

*VDD*

0

10 pF

1 pF

Initially charged to *VDD*

10/1

*VDD*

0

10 pF

1 pF

Initially at ground

*VDD*

**S**

**S**

**A10.2** Repeat problem A10.1 if the 1 pF capacitance is reconnected between the source and gate.

**A10.3** Estimate the voltage across each capacitor, in each of the following circuits, after the MOSFETs have turned on (the initial voltages are shown in the figure). Verify your answers with SPICE.

**A10.4** Repeat problem A10.3 if, for the NMOS device, the intitially voltage across the 1 pF capacitor is 4.5 V while the intitial voltage across the 10 pF capacitor is 5 V and for the PMOS the 1 pF capacitor is inititally at 500 mV and the 10 pF capacitor is at ground. Why aren’t the switches turning on and equalizing the charge across the capacitors?

**Figure A10.3** Charge sharing between two capacitors.

10/1

1 pF @ 1V

10 pF @ 2V

10/1

1 pF @ 4V

10 pF @ 3V

**A10.5** Estimate, and simulate with SPICE, the delay through the following circuits. Ensure you estimate and simulate both *tPHL* and *tPLH*. What are the maximum and minimum output voltages across the capacitor? Can the output of the NMOS charge all the way to *VDD* if you wait long enough?

**A10.6** Repeat problem A10.5 if 10 NMOS devices in series replace the single NMOS device and 10 PMOS devices connected in series replace the single PMOS device.

**Figure A10.5** Estimating the delay through two pass gates.

10/1

1 pF

10/1

1 pF

*VDD*

In

In

Out

Out

**A10.7** Derive an equation for the delay through the following circuit and verify with SPICE. What happens to the delay as we increase *R*1? What happens to the amplitude of the output signal? This circuit is ubiquitous when doing design or test. It’s an important circuit to understand.

**Figure A10.7** Estimating the delay through an RC circuit.

Out

In

*C*

*R*1

*R*2

**A10.8** Estimate the amount of charge the input supplies when transitioning from 0 to *VDD* in the following circuit. Assume that the device turns fully on (its drain voltage goes to zero) and neglect the MOSFET capacitances compared to the 1 pF capacitor.

**Figure A10.8** Estimating the charge supplied by the input source.

*VDD*

0

1 pF

3*VDD*

**A10.9** What is the voltage at point A in the following circuits? Verify your answers with SPICE. What happens in (h) if the PMOS is removed? Does the circuit work better or worse? Why?

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**Figure A10.9** Voltage drops across transmission gates and pass gates.