ECG 721 Memory Circuit Design, Final Exam

Spring 2024, University of Nevada, Las Vegas

Name: _____

- Show your work to get credit.
- Open book and notes.
- Worked exam, a single PDF, should be emailed to Dr. Baker at rjacobbaker@gmail.com by Monday, May 6 at 1 PM.

1. Explain how signal-to-noise ratio is determined by the memory-bit and bit-line capacitances in a DRAM. Make sure your explanation uses equations including Cmbit (memory bit capacitance) and Cbit (bitline capacitance) (5 points)
2. Sketch the schematics for an open bitline configuration DRAM architecture with the n-sense amp, p-sense amp, equilibration circuitry, and I/O devices. Sketch, and label what's going on, the voltage signals used during a read operation. (10 points)
3. What is the biggest concern with increasing the number of rows in a memory array? with increasing the number of columns? (5 points)
4. Why do we need to ensure that the parasitic bitline capacitances connected to a sense amplifier are balanced? (10 points)
5. Sketch the layouts of two DRAM cells used in both folded and open arrays. Comment on the pros and cons of each layout. (5 points)
6. From a circuit designer's point of view what is the difference between CHE and FNT? Which would you expect uses less power? (10 points)
7. Sketch a sense amplifier useful for regenerating logic levels outside of the array (on the side opposite the I/O devices) in a memory. Sometimes this sense amplifier is called a helper flip-flop. Using this topology discuss kickback noise, clock feedthrough, how the previous comparison's results (memory) is erased, and how power is minimized. (20 points)
8. Sketch the schematic of a 6T SRAM memory cell. Describe why you need to precharge the bitlines high. (5 points)
9. Sketch the IV curves for an erased and a programmed Flash memory cells and describe the state of charge on the floating gate in your own words. (5 points)
10. Explain, in your own words, why a VCO is represented as an integration when analyzing PLLs. (5 points)
11. Sketch the schematic of a delta-sigma sensing circuit useful for determining the value of a capacitor based upon the delta-sigma techniques from Ch. 17. Discuss the operation and derive equations governing the circuit's operation. (20 points).