Final for EE 421 Digital Electronics and ECG 621 Digital Integrated Circuit Design
Fall, University of Nevada, Las Vegas

NAME:_____

Show your work to get credit. Open book and closed notes.

Unless otherwise indicated use the following SPICE parameters for hand calculations with ***VDD* = 5 V**. Also, use R'n = 20k, R'p = 40k, and C'ox = 2.5 fF/um^2.

Note that by the book's definition the threshold voltage for the PMOS device is positive (so from the data below V_{THP} = 0.9 V using the book's labeling and equations).

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.MODEL NMOS NMOS LEVEL  = 3
+ TOX    = 150E-10          NSUB   = 1E17            GAMMA  = 0.5
+ PHI    = 0.7              VTO    = 0.8             DELTA  = 3.0
+ UO     = 650              ETA    = 3.0E-6          THETA  = 0.1
+ KP     = 100E-6           VMAX   = 1E5             KAPPA  = 0.3
+ RSH    = 0                NFS    = 1E12            TPG    = 1
+ XJ     = 500E-9           LD     = 100E-9
+ CGDO   = 200E-12          CGSO   = 200E-12         CGBO   = 1E-10
+ CJ     = 400E-6           PB     = 1               MJ     = 0.5
+ CJSW   = 300E-12          MJSW   = 0.5
*
.MODEL PMOS PMOS LEVEL  = 3
+ TOX    = 150E-10          NSUB   = 1E17            GAMMA  = 0.6
+ PHI    = 0.7              VTO    = -0.9            DELTA  = 0.1
+ UO     = 250              ETA    = 0               THETA  = 0.1
+ KP     = 50E-6            VMAX   = 5E4             KAPPA  = 1
+ RSH    = 0                NFS    = 1E12            TPG    = -1
+ XJ     = 500E-9           LD     = 100E-9
+ CGDO   = 200E-12          CGSO   = 200E-12         CGBO   = 1E-10
+ CJ     = 400E-6           PB     = 1               MJ     = 0.5
+ CJSW   = 300E-12          MJSW   = 0.5
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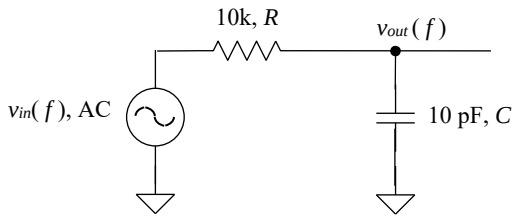
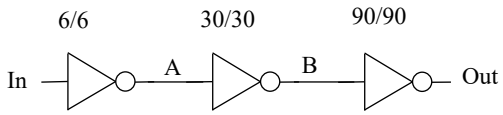
1. Suppose the input in the circuit seen below is a 1 V peak sinusoid with a frequency of 10 MHz. Sketch, by hand, the input and output waveforms in the circuit (in the time domain). What are the magnitude and phase relationships between the input and output? Show your hand calculations for credit (10 points).



2. Suppose an inverter drives a capacitive load from 0 to 5 V at a maximum frequency of 100 MHz with 100 ps edge transitions. If the peak amount of current pulled by the circuit is 100 mA what is the value of the capacitive load? (2 points) What is the average power consumed by the circuit? (4 points) How much power is delivered to the capacitive load? (2 points) What is the peak energy stored by the capacitive load? (2 points) How much power is dissipated by each MOSFET in the inverter? (5 points) Show your work for credit.

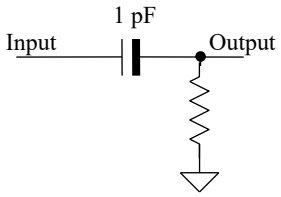
3. Estimate the delays, t_{PHL} and t_{PLH}, from point A to B in the following circuit. All MOSFETs have lengths of 600 nm. Widths of the PMOS and NMOS in each inverter are equal as shown in the figure below. Show your work and place your answers in boxes. (15 points)



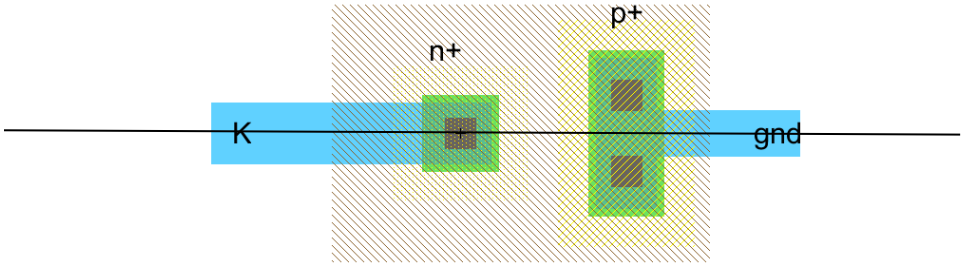
4. Sketch the layout of a poly2 resistor in the C5 process using the hi-res layer. Ensure you label the layers you are using including your connections to metal. (5 points).

5. Sketch the implementation of a logic gate that implements (A + B + C)D. (5 points)

6. Suppose the bottom plate parasitic in the poly1-poly2 capacitor seen below is 25% of the desired capacitance value (here 1 pF). If the resistor is large so its effects can be neglected estimate the output voltage change if the input voltage changes from 0 to *VDD*. Sketch the schematic of the equivalent circuit. Please place a box around your numerical answer (this means put a box around a number, you know *VDD* from the first page of this exam). (5 points)

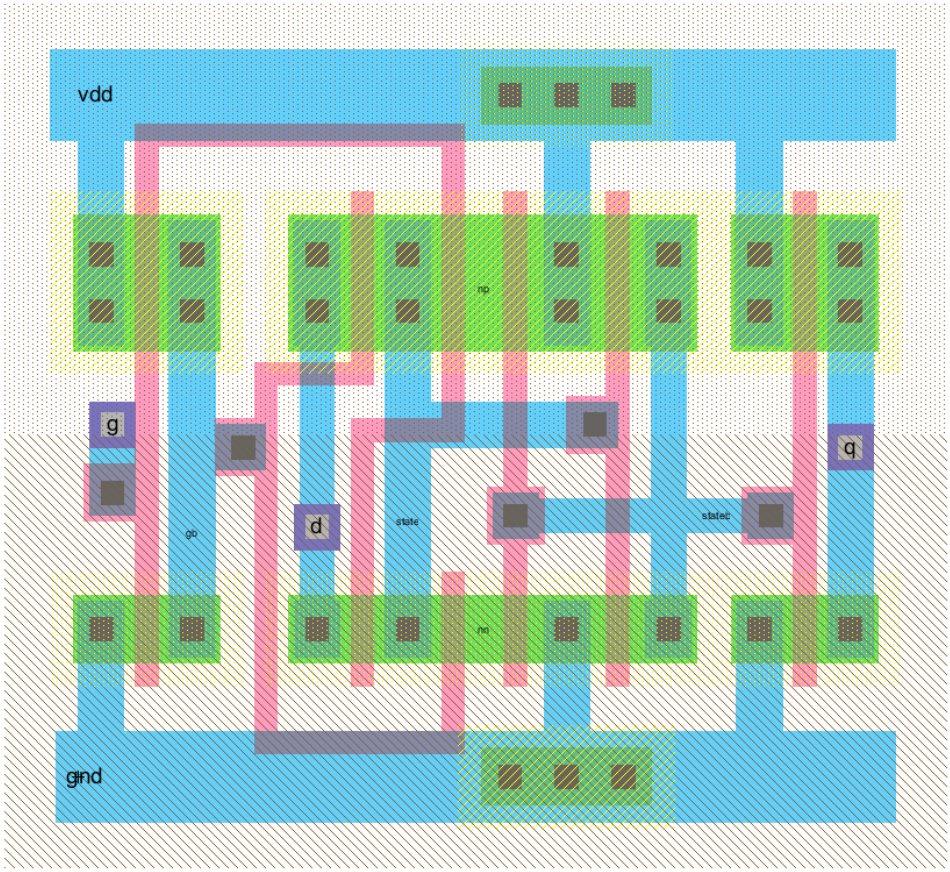


7. Consider the n+ to p-substrate diode seen below.



a. Sketch the cross-sectional view of the diode at the line indicated. (2 points)
b. If the n+ is 1.8 um by 1.8 um and the p+ (substrate) is grounded write an equation for the depletion capacitance of the pn junction in terms of the voltage on K, V_K using: CJ = 4.1E-4, PB = 0.84, MJ = 0.43, CJSW = 3.6E-10, PBSW = 0.8, MJSW = 0.2. (3 points)
c. Using the equation from part b sketch the capacitance seen on K to ground as V_K is increased from 0 to 5 V. (2 points)
d. How does the depletion layer width change as the voltage on K is increased in part c? Why? (3 points)

8. Sketch the corresponding schematic for the following layout. Make sure the body connections of the MOSFETs are clearly seen in your schematic. (10 points)



9. Show how to derive the equation for the V_{SP} of an inverter formed using a PMOS device and a resistor. (10 points)

10. Explain, in your own words, what happens to the current in an inductor when a constant voltage, as used in your projects, is applied to the inductor. (10 points)

11. Estimate the delay through the following circuit. Show your work for credit. (10 points)